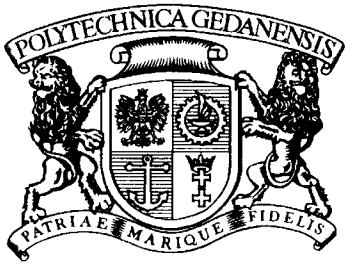

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COMPACT MODELLING AND PARAMETER EXTRACTION FOR CMOS TRANSISTORS

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Technical Report No.53/98

WYDZIAŁ ELEKTRONIKI

TELEKOMUNIKACJI I INFORMATYKI

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Streszczenie

Opracowano model analityczny tranzystorów CMOS w postaci jednej formuły matematycznej, w której parametry nie zależą ani od długości kanału tranzystora ani od napięć polaryzujących tranzystor. Opracowano także metodę ekstrakcji parametrów modelu opartą na zmodyfikowanym algorytmie genetycznym i metodzie gradientowej. Zarówno model, jak i metoda ekstrakcji zostały zweryfikowane eksperymentalnie; materiałem empirycznym były wyniki pomiarów tranzystorów o różnej długości kanału wykonanych w technologii MOSIS.

Compact Modelling and Parameter Extraction for CMOS Transistors

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Abstract

A new fully analytical single-equation dc model of non-uniformly doped CMOS transistors, parameter fitting method for the model and experimental verification are presented. The model is valid for short- and long-channel transistors. Its parameters are independent of channel length. A hybrid parameter extraction technique based on a modified genetic algorithm and gradient method has been developed and succesfully applied to fit parameters to the model.

1. Introduction

The Gradual Channel Approximation (GCA) which is commonly used in analytical modelling of the MOS transistor precludes derivation of any model of the transistor whose validity would be true for the entire range of the drain-source variation, which results from analytical and numerical analyses [1-4].

An unified, single-equation model of the uniformly doped MOSFET abandoning the GCA and analogous model for the non-uniformly doped transistor were presented in [3] and [4], respectively. However, some parameters of the models depend on channel length of the transistor, which is an obstacle to efficient designing and optimisation of electronic circuits.

In this work, we propose a closed system permitting us to model and efficiently fit parameters to measured CMOSFET characteristics. The fully analytical model we present is a generalization of the ones demonstrated in [3,4], is defined by one equation and its parameters are independent of the channel length. It is valid for short- and long-channel transistors. The differential conductance and transconductance derived from it are smooth functions of biasing voltages in the entire range of their variations. Of course, in this model, the threshold voltage depends on the channel length. For completeness, we have also developed an efficient parameter extraction method for the model. The method is based on a genetic algorithm

and supplemented by a gradient method. All the results presented here have been succesfully examined experimentally.

2. The channel-length independent model

In this model, the MOS transistor is treated as a two-dimensional object (the gradual channel approximation is abandoned), in which the channel has also two-dimensional nature. The physics of the model is based on the following phenomena: (i) field effect, (ii) modulation of a channel charge by means of the physical channel-substrate junction, (iii) creation of an "additional" channel charge resulting from variations in the longitudinal electric field component in the channel, (iv) influence of the gate voltage on the carrier mobility, (v) carrier velocity saturation effect, and (vi) nonlinear dependence of the inversion layer charge on the gate voltage, especially for small values of V_{GS}. The model is free from such non-realistic terms as: "pinch-off" and "shortening channel effect".

The basic equation for the drain current of the enhancement-mode, non-uniformly doped MOSFET takes the form:

$$I_D = \frac{\mu E_C B M W C_{ox}(|V_{GS}|-|V_T|)^2 V_{DS}}{(V_C+|V_{GS}|-|V_T|)(LE_{Cef}+B|V_{DS}|)} \qquad (1)$$

in which

$$E_{Cef} = E_C(\beta+\alpha C_{ox}|V_{GS}|),$$

$$M = 1+\frac{a|V_{DS}|\exp(b|V_{GS}|^{-1})}{1+c|V_{DS}|},$$

$$B = \frac{\exp(H|V_{DS}|)}{1+fH|V_{DS}|},$$

$$H = \frac{h}{|V_{GS}|-k}+\frac{1}{m+r|V_{DS}|V_{GS}^2},$$

and

$$\mu = \mu_1\exp(-\mu_2 L),$$

$$\alpha = (\alpha_1+\alpha_2 L)/\ln(\alpha_3 L),$$

$$E_c = E_1\exp(E_2 L),$$

$$V_c = (V_1+V_2 L)\exp(-V_3 L),$$

$$V_T = \sqrt{t_1+t_2 L},$$

$$a = a_1\exp(-a_2 L),$$

$$b = b_1+b_2 L,$$

$$k = k_1\ln(k_2 L),$$

where: W and L are the channel length and width, respectively, μ is the effective low-field bulk mobility, C_{ox} - the gate oxide capacitance per unit area, E_C - a characteristic field, V_C - a characteristic voltage, V_T - the threshold voltage, and the others are parameters which do not depend on the channel length; V_{DS} and V_{GS} are, respectively, the drain-source voltage and the gate-source voltage.

The equation (1) is valid for both n- and p-channel MOSFET and the sign of I_D is defined by the sign of V_{DS} occurring in the numerator of the equation.

3. Parameter extraction

The extraction of model parameters has been performed using a hybrid optimisation system which contains a genetic algorithm (GA) as a global optimisation tool and local search procedures (based on gradient methods) for final tuning of parameter values.

The goal was to minimize an error function defined as an average relative

difference between the measured and the theoretical MOSFET characteristics. The differences were determined in 24 points of each curve of output characteristics of each transistor (the characteristics of eight transistors were taken into account simultaneously).

The genetic algorithm used in our system is based on binary coding (12 bits per variable), and incorporated proportional selection (no elitism), function scaling, flip mutation and one-point crossover [5]. The non-uniform and performance-dependent mutation probability has been introduced to improve the convergence of the algorithm in the late stages of the optimisation process [6].

The optimisation procedure consists of two steps: the search for the basic solution using GA and the improving of this solution using the local search procedure (a gradient method). The employing of global optimisation method (i.e. GA) is necessary because the error function is intractable (it comprises many local extrema) and it is impossible to find a satisfactory solution using local search methods only.

4. Experimental verification

Results of the modelling and the parameter extraction method have been verified experimentally on the basis of data of CMOS transistor measurements. The transistors were fabricated in the p-well MOSIS technology. Each of them was of W=50μm and T_{ox}=42nm (the gate oxide thickness) but the channel lengths were of L=2,3,4,5,6,7,8,10,15,20μm. The results of the parameter fitting are presented in Table 1 and depicted in Figures 1 and 2 (the solid lines and the points represent the measured and theoretical characteristics, respectively); $|V_{GS}|$=1.5V to 5.0V in 0.5V step for the curves in the figures. It should be emphasized that the values of extracted parameters are independent of L and that the equally close accuracy has been attained for all the measured transistors.

Table 1. Extracted Parameters for NMOS's and PMOS's

Parameter	NMOS's	PMOS's
μ_1 [$cm^2V^{-1}s^{-1}$]	1051.35	351.82
μ_2 [cm^{-1}]	689.0	357.75
α_1 [$cm^2A^{-1}s^{-1}$]	2261914	2122516
α_2 [$cmA^{-1}s^{-1}$]	$-8197\cdot10^5$	$6472\cdot10^5$
α_3 [cm^{-1}]	$1.371\cdot10^4$	$1.425\cdot10^4$
E_1 [Vcm^{-1}]	5497.5	11604.7
E_2 [cm^{-1}]	293.6	-744.1
V_1 [V]	-2.357	-6.238
V_2 [Vcm^{-1}]	25121.6	57704.8
V_3 [cm^{-1}]	384.4	1351.4
a_1 [V^{-1}]	0.140	0.1067
a_2 [cm^{-1}]	2863.0	2878.2
b_1 [V]	0.875	3.154
b_2 [Vcm^{-1}]	-375	-1572
k_1 [V]	-0.0469	0.0869
k_2 [cm^{-1}]	$18\cdot10^{-6}$	15811.4
t_1 [V^2]	0.7983	0.6344
t_2 [V^2cm^{-1}]	4.47	28.1
c [V^{-1}]	0.1	0.1
f [-]	0.75	0.75
h [-]	6	4
m [V]	0.1	0.1
r [V^{-2}]	0.5	0.1
β [-]	-0.0001	-0.0001

5. Conclusion

We have demonstrated a new fully analytical single-equation dc model of the non-uniformly doped CMOS transistor and the efficient algorithm for parameter fitting to the model. The parameters of the model are independent of the channel length.

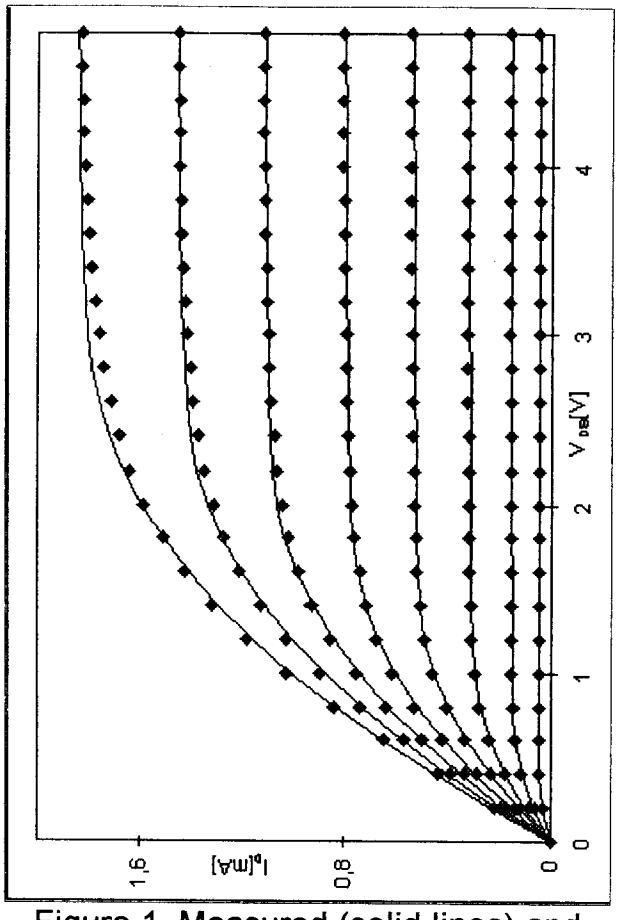

Figure 1. Measured (solid lines) and calculated (points) NMOS characteristics; L=8μm

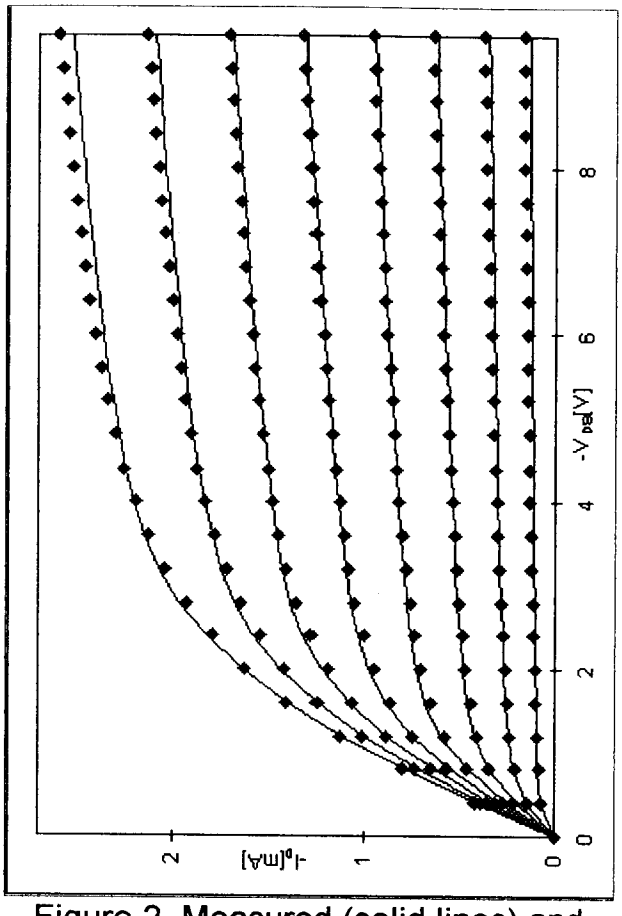

Figure 2. Measured (solid lines) and calculated (points) PMOS characteristics; L=3μm

Both validity of the model and the efficiency of the parameter fitting method have been experimentally confirmed. Unlike the known models, there are no physical inconsistencies in this model. Moreover, the transconductance degradation effect is reflected by the model for any value of V_{DS}. The model is very useful for circuit analysis, simulation and optimisation purposes.

6. References

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