C H A P T E R 6

Models of Semiconductor Devices

Integrated circuits, in contrary to discrete circuits, can be designed only with computer-aided simulation tools. A design can be successful only if those computer simulators satisfactorily imitate real circuits. The results of simulations are only as good as the accuracy of the models used. To match characteristics of basic semiconductor devices, relatively complex mathematical models with about thirty to fifty different parameters are used. It is not possible to obtain correct results, even with a perfect model, if inaccurate parameters are used. For a successful design it is very important to understand the meaning of each model parameter and how this parameter is used in mathematical formulas used by SPICE programs.

This chapter presents equations and formulas which are used for modeling semiconductor devices in SPICE programs. Depending on the implementations various mathematical models are used. For example, the MOS transistor is described by more than 20 different models. It is not possible to cover all the models implemented in various SPICE programs in this book. Only the most basic and commonly used models are described in this Chapter.

The following table describes common symbols which are used throughout Chapter 6.

Common symbols used in equations	
T	Absolute temperature in K
T_{nom}	Nominal temperature in K at which all parameters were measured
k	Boltzmann constant $k = 8.62 \cdot 10^{-5}$ eV/K
q	Electron charge $q = 1.6 \cdot 10^{-19}$ C
V_T	Thermal potential $V_T = kT/q \approx 25.8$ mV at 300 °K
ε_o	Permittivity of free space $\varepsilon_o = 8.85 \cdot 10^{-12}$ F/m
ε_{si}	Relative permittivity of Si (silicon)
ε_{ox}	Relative permittivity of SiO_2 (silicon oxide)

B - GaAs FET PSPICE only

GaAs FET Model

.MODEL *Model_name* **GASFET** [*Model parameters*]

1. Model parameters

In PSPICE, four different models are implemented: level1 through level4.

Parameters for All Levels				
Name	*Parameter*	*Units*	*Default*	*Typical*
LEVEL	Model index	-	1	2
VTO	Pinch-off voltage	V	-2.5	-2.0
BETA	Transconductance coefficient	A/V^2	0.1	0.1
LAMBDA	Channel-length modulation parameter	1/V	0	10^3
RD	Drain ohmic resistance	Ω	0	100
RS	Source ohmic resistance	Ω	0	100
RG	Gate ohmic resistance	Ω	0	10
IS	Gate p-n saturation current	A	10^{-14}	10^{-14}
N	Gate p-n emission coefficient	–	1	1.2
VBI	Gate p-n potential	V	1.0	0.9
CGS	Zero-bias G-S junction capacitance	F	0	5 pF
CGD	Zero-bias G-D junction capacitance	F	0	5 pF
CDS	Zero-bias D-S capacitance	F	0	1 pF
FC	Coefficient for forward-bias depletion capacitance formula	-	0.5	0.5
EG	Bandgap voltage	eV	1.1	1.4
XTI	**IS** temperature exponent	-	0	
VTOTC	**VTO** temperature coefficient	V/°C	0	
BETATCE	**BETA** exponential temperature coefficient	%/°C	0	
TRG1	**RG** temperature coefficient (linear)	1/°C	0	0.001
TRD1	**RD** temperature coefficient (linear)	1/°C	0	0.001

TRS1	**RS** temperature coefficient (linear)	1/°C	0	0.001
KF	Flicker noise coefficient	-	0	-
AF	Flicker noise exponent	-	1	-

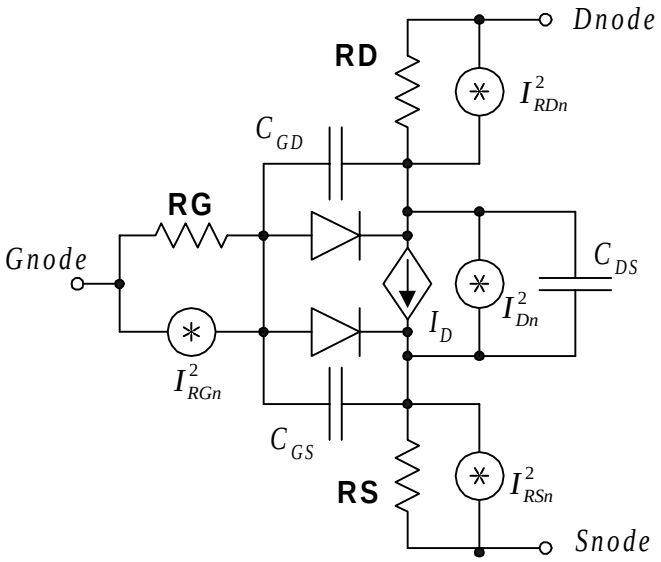
Parameters for Level 1				
Name	*Parameter*	*Units*	*Default*	*Typical*
ALPHA	Saturation voltage parameter	1/V	2.0	2.0
TAU	Conduction current delay time	s	0	
M	Gate *pn* grading coefficient	-	0.5	0.5

Parameters for Level 2				
Name	*Parameter*	*Units*	*Default*	*Typical*
ALPHA	Saturation voltage parameter	1/V	2.0	2.0
B	Doping tail extending parameter	1/V	0.3	0.3
TAU	Conduction current delay time	s	0	
M	Gate p-n grading coefficient	-	0.5	0.5
VDELTA	Capacitance transition voltage	V	0.2	0.2
VMAX	Capacitance limiting voltage	V	0.5	0.5

Parameters for Level3				
Name	*Parameter*	*Units*	*Default*	*Typical*
ALPHA	Saturation voltage parameter	1/V	2.0	2.0
GAMMA	Static feedback parameter	-	0	
DELTA	Output feedback parameter	1/AV	0	
Q	Power-law parameter	-	2	2
TAU	Conduction current delay time	s	0	
M	Gate *pn* grading coefficient	-	0.5	0.5
VDELTA	Capacitance transition voltage	V	0.2	0.2
VMAX	Capacitance limiting voltage	V	0.5	0.5

Parameters for Level 4				
Name	*Parameter*	*Units*	*Default*	*Typical*
ACGAM	Capacitance modulation	-	0	
DELTA	Output feedback parameter	1/AV	0	
Q	Power-law parameter	-	2	2
HFGAM	High-frequency V_{GD} feedback parameter	-	0	
HFG1	**HFGAM** modulation by V_{SG}	1/V	0	
HFG2	**HFGAM** modulation by V_{DG}	1/V	0	
HFETA	High-frequency V_{GS} feedback parameter	-	0	
HFE1	**HFETA** modulation by V_{GD}	1/V	0	
HFE2	**HFETA** modulation by V_{GS}	1/V	0	
LFGAM	Low-frequency feedback parameter	-	0	
LFG1	**LFGAM** modulation by V_{SG}	1/V	0	
LFG2	**LFGAM** modulation by V_{DG}	1/V	0	
MXI	Saturation knee-potential modulation	-	0	
MVST	Subthreshold modulation	1/V	0	
P	Linear-region power law exponent	-	2	2
TAUD	Relaxation time for thermal reduction	s	0	
TAUG	Relaxation time for GAM feedback	s	0	
VBD	Gate junction breakdown potential	V	1	5
VST	Subthreshold potential	V	0	0
XC	Capacitance pinch-off reduction factor	-	0	
XI	Saturation knee potential factor	-	1000	
Z	Knee transition parameter	-	0.5	
VMAX	Capacitance limiting voltage	V	0.5	0.5

2. Equivalent diagram



Terminal voltage used in equations	
V_{DS}	intrinsic drain-source voltage
V_{GS}	intrinsic gate-source voltage
V_{GD}	intrinsic gate-drain voltage
Other parameters such as V_T, T, and T_{nom} are defined in the introductory section	

3. Model equations

dc Currents for Level 1

For $V_{DS} \geq 0$ (normal mode) and V_{GS} - **VTO** < 0 (cutoff region):

$$I_D = 0 \qquad \textbf{(B-1)}$$

For $V_{DS} \geq 0$ (normal mode) and V_{GS} - **VTO** > 0 (linear and saturation region):

$$I_D = \textbf{BETA}\left(1+\textbf{LAMBDA}\,V_{DS}\right)\left(V_{GS}-\textbf{VTO}\right)^2 \tanh\left(\textbf{ALPHA}\,V_{DS}\right) \qquad \textbf{(B-2)}$$

For $V_{DS} < 0$ (inverted mode) source and drain terminals are switched.

dc Currents for Level 2

For $V_{DS} \geq 0$ (normal mode) and V_{GS} - **VTO** < 0 (cutoff region):

$$I_D = 0 \qquad \textbf{(B-3)}$$

For $V_{DS} \geq 0$ (normal mode) and V_{GS} - **VTO** > 0 (linear and saturation region):

$$I_D = \textbf{BETA}\left(1+\textbf{LAMBDA}\,V_{DS}\right)\left(V_{GS}-\textbf{VTO}\right)^2 \frac{K_t}{1+\textbf{B}\left(V_{GS}-\textbf{VTO}\right)} \qquad \textbf{(B-4)}$$

where K_t is a polynomial approximation of hyperbolic tangent:

$$K_t = \begin{cases} 1-\left(1-\dfrac{V_{DS}\textbf{ALPHA}}{3}\right)^3 & \text{for } 0 < V_{DS} < 3/\textbf{ALPHA} \\ 1 & \text{for } V_{DS} \geq 3/\textbf{ALPHA} \end{cases} \qquad \textbf{(B-5)}$$

For $V_{DS} < 0$ (inverted mode) source and drain terminals are switched.

dc Currents for Level 3

For $V_{DS} \geq 0$ normal mode) and V_{GS} - $V_{TO} < 0$ (cutoff region)

$$I_D = 0 \qquad \textbf{(B-6)}$$

For $V_{DS} \geq 0$ (normal mode) and V_{GS} - $V_{TO} > 0$ (linear and saturation region)

$$I_D = \frac{I_{DSO}}{1+\textbf{DELTA}\,V_{DS}\,I_{DSO}} \qquad \textbf{(B-7)}$$

$$I_{DSO} = \textbf{BETA}\left(V_{GS}-V_{TO}\right)^2 K_t \qquad \textbf{(B-8)}$$

$$V_{TO} = \textbf{VTO} - \mathit{GAMMA}\,V_{DS} \qquad \textbf{(B-9)}$$

$$K_t = \begin{cases} 1-\left(1-\dfrac{V_{DS}\textbf{ALPHA}}{3}\right)^3 & \text{for } 0 < V_{DS} < 3/\textbf{ALPHA} \\ 1 & \text{for } V_{DS} \geq 3/\textbf{ALPHA} \end{cases} \qquad \textbf{(B-10)}$$

For $V_{DS} < 0$ (inverted mode) source and drain terminals are switched.

For the Level 4 model see the PSPICE Reference Manual and A. E. Parker and D. J. Skellern, "Improved MESFET Characterization for Analog Circuit Design and Analysis," *1992 IEEE GaAs IC Symposium Technical Digest*, pp. 225-228, Miami Beach, October 4-7, 1992.

Capacitances for Level 1

$$C_{GS} = \begin{cases} \mathit{Rarea}\ \mathbf{CGS}\left(1-\dfrac{V_{GS}}{\mathbf{VBI}}\right)^{-\mathbf{M}} & \text{for } V_{GS} \le \mathbf{FC}\ \mathbf{VBI} \\ \mathit{Rarea}\ \mathbf{CGS}\left(1-\mathbf{FC}\right)^{-(1+\mathbf{M})}\left[1-\mathbf{FC}\left(1+\mathbf{M}\right)+\dfrac{\mathbf{M}\,V_{GS}}{\mathbf{VBI}}\right] & \text{for } V_{GS} > \mathbf{FC}\ \mathbf{VBI} \end{cases} \quad \textbf{(B-11)}$$

$$C_{GD} = \begin{cases} \mathit{Rarea}\ \mathbf{CGD}\left(1-\dfrac{V_{GD}}{\mathbf{VBI}}\right)^{-\mathbf{M}} & \text{for } V_{GD} \le \mathbf{FC}\ \mathbf{VBI} \\ \mathit{Rarea}\ \mathbf{CGD}\left(1-\mathbf{FC}\right)^{-(1+\mathbf{M})}\left[1-\mathbf{FC}\left(1+\mathbf{M}\right)+\dfrac{\mathbf{M}\,V_{GD}}{\mathbf{VBI}}\right] & \text{for } V_{GD} > \mathbf{FC}\ \mathbf{VBI} \end{cases} \quad \textbf{(B-12)}$$

Capacitances for Level 2 and Level 3

$$C_{GS} = \mathit{Rarea}\left(\mathbf{CGS}\,\frac{K_1\,K_2}{\sqrt{1-\dfrac{V_n}{\mathbf{VBI}}}}+\mathbf{CGD}\,K_3\right) \quad \textbf{(B-13)}$$

$$C_{GD} = \mathit{Rarea}\left(\mathbf{CGS}\,\frac{K_1\,K_3}{\sqrt{1-\dfrac{V_n}{\mathbf{VBI}}}}+\mathbf{CGD}\,K_2\right) \quad \textbf{(B-14)}$$

$$K_1 = 0.5\left[1+\frac{V_e-\mathbf{VTO}}{\sqrt{\left(V_e-\mathbf{VTO}\right)^2+\mathbf{VDELTA}^2}}\right] \quad \textbf{(B-15)}$$

$$K_2 = 0.5\left[1+\frac{V_{GS}-V_{GD}}{\sqrt{\left(V_{GS}-V_{GD}\right)^2+\dfrac{1}{\mathbf{ALPHA}^2}}}\right] \quad \textbf{(B-16)}$$

$$K_3 = 0.5\left[1-\frac{V_{GS}-V_{GD}}{\sqrt{\left(V_{GS}-V_{GD}\right)^2+\dfrac{1}{\mathbf{ALPHA}^2}}}\right] \quad \textbf{(B-17)}$$

$$V_n = \begin{cases} 0.5\left[V_e+\mathbf{VTO}+\sqrt{\left(V_e-\mathbf{VTO}\right)^2+\mathbf{VDELTA}^2}\right] & \text{for } V_O < \mathbf{VMAX} \\ \mathbf{VMAX} & \text{for } V_O \ge \mathbf{VMAX} \end{cases} \quad \textbf{(B-18)}$$

$$V_e = 0.5\left[V_{GS} + V_{GD} + \sqrt{\left(V_{GS} - V_{GD}\right)^2 + \frac{1}{\mathbf{ALPHA}^2}}\right] \quad \textbf{(B-19)}$$

$$V_O = 0.5\left[V_e + \mathbf{VTO} + \sqrt{\left(V_e - \mathbf{VTO}\right)^2 + \mathbf{VDELTA}^2}\right] \quad \textbf{(B-20)}$$

Noise for All Levels

$$I_{RSn}^2 = Rarea\frac{4kT}{\mathbf{RS}}\,BW \quad \textbf{(B-21)}$$

$$I_{RDn}^2 = Rarea\frac{4\,k\,T}{\mathbf{RD}}\,BW \quad \textbf{(B-22)}$$

$$I_{Dn}^2 = \left(I_{shot}^2 + I_{flicker}^2\right) BW \quad \textbf{(B-23)}$$

$$I_{shot}^2 = 2\,q\,I_D \quad \textbf{(B-24)}$$

$$I_{flicker}^2 = \frac{\mathbf{KF}\,I_D^{\mathbf{AF}}}{Freq} \quad \textbf{(B-25)}$$

Both bandwidth *BW* and frequency *Freq* are expressed in Hz. Thermal noise is generated by the series resistance. The parameter *Rarea* indicates that for diodes with large relative area, the actual resistance is smaller. Shot noise is proportional to the drain current as shown by Eq. (B-24). Flicker noise dominates at low frequencies. It increases with the current level and is inversely proportional to the frequency, as shown by Eq. (B-25). The flicker noise source is described by two parameters, **KF** and **AF**. Description of MESFET models can be found in PSPICE Reference Manual and in more detail in:

Level 1 W. R. Curtice, "A MESFET Model for Use in the Design of GaAs Integrated Circuits," *IEEE Trans. On Microwave Theory and Techniques* **MTT-28**, pp. 448-456, 1980.

Level 2 H. Statz, P. Newman, I. W. Smith, R. A. Pucel, and H. A. Haus, "GaAs FET Device and Circuit Simulation in SPICE," *IEEE Transactions on Electron Devices* **ED-34**, pp. 160-169, February 1987. This is the same model as implemented in SPICE3 using the names starting with the letter **Z**.

Level 3 A. J. McCamant, G. D. McCormack, and D. H. Smith, "An Improved GaAs MESFET Model for SPICE," *IEEE Trans. on Microwave Theory and Techniques* **MTT-38**, June 1990.

Level 4 A. E. Parker and D. J. Skellern, "Improved MESFET Characterization for Analog Circuit Design and Analysis," *1992 IEEE GaAs IC Symposium Technical Digest*, pp. 225-228, Miami Beach, October 4-7, 1992.

D - Diode

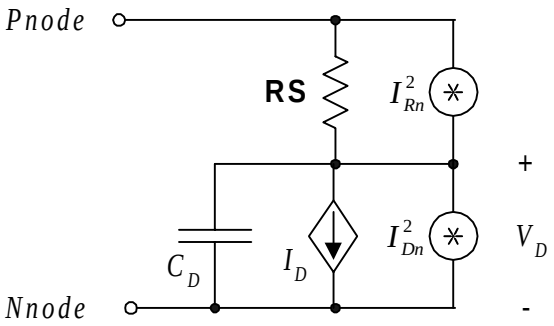
Diode Model

.MODEL *Model_name* **D** [*Model parameters*]

1. Model parameters

Name	*Parameter*	*Units*	*Default*	*Typical*
IS	Saturation current for *Rarea* = 1	A	10^{-14}	10^{-14}
RS	Ohmic series resistance for *Rarea* = 1	Ω	0	3
N	Emission coefficient	-	1	1
TT	Transit time	s	0	10^{-9}
CJO	Zero-bias junction capacitance for *Rarea* = 1	F	0	$3{\cdot}10^{-12}$
VJ	Junction potential	V	1	0.8
M	Grading coefficient	-	0.5	0.5
EG	Energy gap	eV	1.11	1.11
XTI	Saturation current temperature exponent	-	3.0	3.0
KF	Flicker noise coefficient	-	0	-
AF	Flicker noise exponent	-	1	-
FC	Coefficient for forward-bias depletion capacitance formula	-	0.5	-
BV	Reverse breakdown voltage	V	∞	80
IBV	Current at breakdown voltage	A	10^{-3}	$2{\cdot}10^{-3}$
TNOM	Temperature at which parameters were measured	°C	27	27
	PSPICE extensions			
IKF	Corner for high injection current roll-off for *Rarea* = 1	A	∞	0.1
TIKF	IKF temperature coefficient (linear)	1/°C	0	0
ISR	Recombination saturation current for *Rarea* = 1	A	0	10^{-8}
NR	Recombination emission coefficient	-	2	2
NBV	Reverse breakdown ideality factor	-	1	1
IBVL	Low-level reverse breakdown “knee” current for *Rarea* = 1	A	0	0
NBVL	Low-level reverse breakdown ideality factor	-	1	10^{-8}
TBV1	BV temperature coefficient (linear)	1/°C	0	0.003
TBV2	BV temperature coefficient (quadratic)	$1/°C^2$	0	0
TRS1	RS temperature coefficient (linear)	1/°C	0	0.002
TRS2	RS temperature coefficient (quadratic)	$1/°C^2$	0	0

2. Equivalent diagram



Terminal voltage used in equations	
V_D	intrinsic diode voltage
Other parameters such as V_T, T, and T_{nom} are defined in the introductory section	

3. Model equations

dc Currents

$$I_D = Rarea\left(I_{Forward} - I_{Reverse}\right) \quad \textbf{(D-1)}$$

$$I_{Forward} = I_{Normal} + I_{Recombination} \quad \textbf{(D-2)}$$

$$I_{Normal} = \mathbf{IS}\sqrt{\frac{\mathbf{IKF}}{\mathbf{IKF} + I_{Normal}}}\left[\exp\left(\frac{V_D}{\mathbf{N}V_T}\right) - 1\right] \quad \textbf{(D-3)}$$

$$I_{Recombination} = \mathbf{ISR}\left[\left(1 - \frac{V_D}{\mathbf{VJ}}\right)^2 + 0.005\right]^{\frac{\mathbf{M}}{2}}\left[\exp\left(\frac{V_D}{\mathbf{NR}V_T}\right) - 1\right] \quad \textbf{(D-4)}$$

$$I_{Reverse} = \mathbf{IBV}\exp\left(-\frac{V_D + \mathbf{VB}}{\mathbf{NBV}\,V_T}\right) + \mathbf{IBVL}\exp\left(-\frac{V_D + \mathbf{VB}}{\mathbf{NBVL}\,V_T}\right) \quad \textbf{(D-5)}$$

The diode is really modeled as two virtual diodes connected in parallel: one for diffusion-based phenomena (**IS**, **N**), and a second for recombination phenomena (**ISR**, **NR**). Both

diodes are described by the "diode equation," where **IS** and **ISR** are modified by middle terms of Eq. (D-3) and (D-4). For very high injection levels, the diode characteristics are flatted using the **IKF** parameter in Eq. (D-3). The recombination current is a function of the depletion-layer width (see the term of Eq. (D-4) with **VJ** and **M** parameters). Typically, **NR** ≈ 2, and the diffusion phenomena dominate in the normal and high current range. Generation phenomena dominate in the low forward current range and for reverse bias. Note that **ISR** is usually 3 to 4 orders of magnitude larger than **IS**. The reverse diode characteristic in the vicinity of the breakdown voltage is modeled using Eq. (D-5) with **IBV**, **VB**, **NBV**, **NBVL**, and **IBVL** as parameters.

Capacitances

$$C_D = C_{transit-time} + Rarea\ C_{depletion} \tag{D-6}$$

$$C_{transit-time} = \mathbf{TT}\frac{\partial}{\partial V_D}\left(I_{Forward}\right) \approx \mathbf{TT}\frac{I_D}{\mathbf{N}_{eff} V_T} \approx \frac{\mathbf{TT}}{r_D} \tag{D-7}$$

$$C_{depletion} = \begin{cases} \mathbf{CJO}\left(1-\dfrac{V_D}{\mathbf{VJ}}\right)^{-\mathbf{M}} & \text{for } V_D \le \mathbf{FC}\ \ \mathbf{VJ} \\ \mathbf{CJO}\left(1-\mathbf{FC}\right)^{-(1+\mathbf{M})}\left[1-\mathbf{FC}\left(1+\mathbf{M}\right)+\mathbf{M}\dfrac{V_D}{\mathbf{VJ}}\right] & \text{for } V_D > \mathbf{FC}\ \mathbf{VJ} \end{cases} \tag{D-8}$$

The junction capacitance always has two components: $C_{transit\text{-}time}$ which is proportional to the diode current, Eq. (D-6); and $C_{depletion}$ which changes with voltage in the same manner as the depletion-layer thickness changes, Eq. (D-7).

Temperature Effects

$$\mathbf{IS}(T) = \mathbf{IS}\left(\frac{T}{T_{nom}}\right)^{\frac{\mathbf{XTI}}{\mathbf{N}}} \exp\left[\left(\frac{T}{T_{nom}}-1\right)\frac{\mathbf{EG}}{\mathbf{N}\ V_T}\right] \tag{D-9}$$

$$\mathbf{ISR}(T) = \mathbf{ISR}\left(\frac{T}{T_{nom}}\right)^{\frac{\mathbf{XTI}}{\mathbf{NR}}} \exp\left[\left(\frac{T}{T_{nom}}-1\right)\frac{\mathbf{EG}}{\mathbf{NR}\ V_T}\right] \tag{D-10}$$

$$\mathbf{IKF}(T) = \mathbf{IKF}\left[1+\mathbf{TIKF}\left(T-T_{nom}\right)\right] \tag{D-11}$$

$$\mathbf{BV}(T) = \mathbf{BV}\left[1+\mathbf{TBV1}\left(T-T_{nom}\right)+\mathbf{TBV2}\left(T-T_{nom}\right)^2\right] \tag{D-12}$$

$$\mathbf{RS}(T) = \mathbf{RS}\left[1+\mathbf{TRS1}\left(T-T_{nom}\right)+\mathbf{TRS2}\left(T-T_{nom}\right)^2\right] \tag{D-13}$$

$$\mathbf{CJO}(T) = \mathbf{CJO}\left\{1 + \mathbf{M}\left[0.0004\left(T - T_{nom}\right) + \left(1 - \frac{\mathbf{VJ}(T)}{\mathbf{VJ}}\right)\right]\right\} \quad \textbf{(D-14)}$$

$$\mathbf{VJ}(T) = \mathbf{VJ}\frac{T}{T_{non}} - 3V_T \ln\left(\frac{T}{T_{non}}\right) - \mathbf{EG}\frac{T}{T_{non}} + 1.16 - 0.000702\frac{T^2}{T + 1108} \quad \textbf{(D-15)}$$

Equation (D-15) is valid only for silicon, since it approximates the silicon energy bandgap variation with temperature.

Noise

$$I_{Rn}^2 = Rarea\frac{4\,k\,T}{\mathbf{RS}}\,BW \quad \textbf{(D-16)}$$

$$I_{Dn}^2 = \left(I_{shot}^2 + I_{flicker}^2\right) BW \quad \textbf{(D-17)}$$

$$I_{shot}^2 = 2\,q\,I_D \quad \textbf{(D-18)}$$

$$I_{flicker}^2 = \frac{\mathbf{KF}\,I_D^{\mathbf{AF}}}{Freq} \quad \textbf{(D-19)}$$

Both bandwidth *BW* and frequency *Freq* are expressed in Hz. Thermal noise is generated by the series resistance. The parameter *Rarea* indicates that for diodes with large relative area, the actual resistance is smaller. Shot noise is proportional to the diode current, as shown by Eq. (D-18). Flicker noise dominates at low frequencies. It increases with the current level and is inversely proportional to the frequency, as shown by Eq. **(**D-19). The flicker noise source is described by two parameters, **KF** and **AF**.

Equations (D-1) through (D-19) are implemented in PSPICE. The Berkeley SPICE2 and SPICE3 programs use a simpler diode model. Equations for SPICE2/SPICE3 can be obtained by setting the additional PSPICE parameters to their default values.

J - JFET

JFET Models

.MODEL *Model_name* **NJF** [*Model parameters*]
.MODEL *Model_name* **PJF** [*Model parameters*]

1. Model parameters

Name	*Parameter*	*Units*	*Default*	*Typical*
VTO	Threshold voltage	V	-2.0	-2.0
BETA	Transconductance parameter	A/V^2	10^{-4}	10^{-4}
LAMBDA	Channel-length modulation parameter	1/V	0	0
RD	Drain resistance	Ω	0	20
RS	Source resistance	Ω	0	20
CGS	Zero-bias *G-S* junction capacitance	F	0	5 pF
CGD	Zero-bias *G-D* junction capacitance	F	0	5 pF
PB	Gate junction potential	V	1	0.8
IS	Gate junction saturation current	A	1.0^{-14}	1.0^{-15}
KF	Flicker noise coefficient	-	0	
AF	Flicker noise exponent	-	1	1
FC	Coefficient for forward-bias depletion capacitance formula	-	0.5	0.5
TNOM	Parameter measurement temperature	°C	27	27
PSPICE extensions				
N	Gate *pn* emission coefficient	-	1	1
ISR	Gate *pn* recombination current parameter	A	0	
NR	Emission coefficient for **ISR**	-	2	2
ALPHA	Ionization coefficient	1/V	0	
VK	Ionization “knee” voltage	V	0	
M	Grading p-n coefficient	-	0.5	0.5
VTOTC	**VTO** temperature coefficient	V/°C	0	
BETACE	**BETA** exponential temperature coefficient	%/°C	0	
XTI	**IS** temperature coefficient	-	3	3

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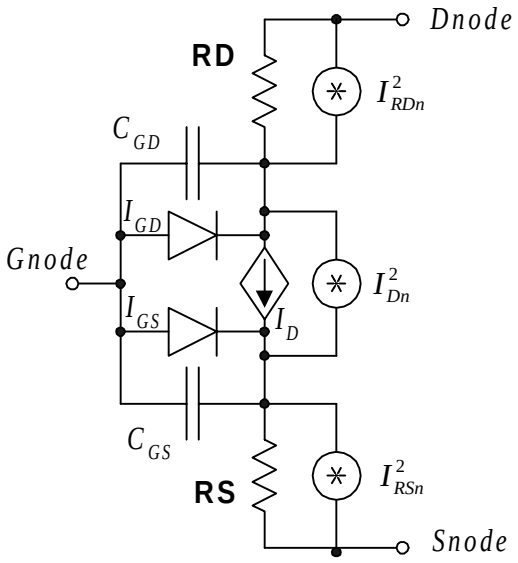
2. Equivalent diagram



Terminal voltage used in equations	
V_{DS}	intrinsic drain-source voltage
V_{GS}	intrinsic gate-source voltage
Other parameters such as V_T, T, and T_{nom} are defined in the introductory section	

3. Model equations

dc Currents

$$I_{Gate} = Rarea\ \left(I_{GS} + I_{GD}\right) \quad \textbf{(J-1)}$$

$$I_{GS} = \mathbf{IS}\left[\exp\left(\frac{V_{GS}}{\mathbf{N}V_T}\right)-1\right] + K_{GS}\mathbf{ISR}\left[\exp\left(\frac{V_{GS}}{\mathbf{NR}\ V_T}\right)-1\right] \quad \textbf{(J-2)}$$

$$K_{GS} = \left[\left(1-\frac{V_{GS}}{\mathbf{PB}}\right)^2 + 0.005\right]^{\frac{\mathbf{M}}{2}} \quad \textbf{(J-3)}$$

$$I_{GD} = \mathbf{IS}\left[\exp\left(\frac{V_{GD}}{\mathbf{N}V_T}\right)-1\right] + K_{GD}\mathbf{ISR}\left[\exp\left(\frac{V_{GD}}{\mathbf{NR}\ V_T}\right)-1\right] + I_I \quad \textbf{(J-4)}$$

$$K_{GD} = \left[\left(1 - \frac{V_{GD}}{\mathbf{PB}}\right)^2 + 0.005\right]^{\frac{\mathbf{M}}{2}} \quad \textbf{(J-5)}$$

$$I_I = \begin{cases} I_D\ \mathbf{ALPHA}\ V_{dif}\ \exp\left(-\dfrac{V_{DG}}{V_{dif}}\right) & \text{for} \quad 0 < V_{GS} - \mathbf{VTO} < V_{DS} \\ 0 & \text{otherwise} \end{cases} \quad \textbf{(J-6)}$$

$$I_{Drain} = Rarea\ \left(I_D - I_{GD}\right) \quad \textbf{(J-7)}$$

$$I_{Source} = Rarea\ \left(-I_D - I_{GS}\right) \quad \textbf{(J-8)}$$

For $V_{DS} \geq 0$ (normal mode) and V_{GS} - **VTO** <0 (cutoff region)

$$I_D = 0 \quad \textbf{(J-9)}$$

For $V_{DS} \geq 0$ (normal mode) and $V_{DS} < V_{GS}$ - **VTO** (linear region)

$$I_D = \mathbf{BETA}\left(1 + \mathbf{LAMBDA}\ V_{DS}\right)V_{DS}\left[2\left(V_{GS} - \mathbf{VTO}\right) - V_{DS}\right] \quad \textbf{(J-10)}$$

For $V_{DS} \geq 0$ (normal mode) and $V_{DS} > V_{GS}$ - **VTO** (saturation region)

$$I_D = \mathbf{BETA}\left(1 + \mathbf{LAMBDA}\ V_{DS}\right)\left(V_{GS} - \mathbf{VTO}\right)^2 \quad \textbf{(J-11)}$$

For $V_{DS} < 0$ (inverted mode) source and drain terminals are switched and Eqs. (J-1) through (J-11) are used.

Equations for drain current in the JFET model are derived from the MOS FET level-1 model of Shichman and Hodges. The above formulas are for the model implemented in PSPICE. SPICE2 and SPICE3 models are simple and can be obtained by setting the default value for additional PSPICE parameters.

Capacitances

In the JFET model only depletion capacitances are used.

$$C_{GS} = \begin{cases} Rarea\ \mathbf{CGS}\left(1 - \dfrac{V_{GS}}{\mathbf{PB}}\right)^{-\mathbf{M}} & \text{for } V_{GS} \leq \mathbf{FC}\ \mathbf{PB} \\ Rarea\ \mathbf{CGS}\left(1 - \mathbf{FC}\right)^{-(1+\mathbf{M})}\left[1 - \mathbf{FC}\left(1 + \mathbf{M}\right) + \dfrac{\mathbf{M}\ V_{GS}}{\mathbf{PB}}\right] & \text{for } V_{GS} > \mathbf{FC}\ \mathbf{PB} \end{cases} \quad \textbf{(J-12)}$$

$$C_{GD} = \begin{cases} Rarea\ \mathbf{CGD}\left(1 - \dfrac{V_{GD}}{\mathbf{PB}}\right)^{-\mathbf{M}} & \text{for } V_{GD} \leq \mathbf{FC}\ \mathbf{PB} \\ Rarea\ \mathbf{CGD}\left(1 - \mathbf{FC}\right)^{-(1+\mathbf{M})}\left[1 - \mathbf{FC}\left(1 + \mathbf{M}\right) + \dfrac{\mathbf{M}\ V_{GD}}{\mathbf{PB}}\right] & \text{for } V_{GD} > \mathbf{FC}\ \mathbf{PB} \end{cases} \quad \textbf{(J-13)}$$

Temperature effects

$$\mathbf{VTO}(T) = \mathbf{VTO} + \mathbf{VTOTC}\left(T - T_{nom}\right) \quad \textbf{(J-14)}$$

$$\mathbf{BETA}(T) = \mathbf{BETA}\, 1.01^{\mathbf{BETATC}\left(T - T_{nom}\right)} \quad \textbf{(J-15)}$$

$$\mathbf{IS}(T) = \mathbf{IS}\left(\frac{T}{T_{nom}}\right)^{\frac{\mathbf{XTI}}{\mathbf{N}}} \exp\left(\frac{\left(\frac{T}{T_{nom}} - 1\right) 1.11}{\mathbf{N}\, V_T}\right) \quad \textbf{(J-16)}$$

$$\mathbf{ISR}(T) = \mathbf{ISR}\left(\frac{T}{T_{nom}}\right)^{\frac{\mathbf{XTI}}{\mathbf{NR}}} \exp\left(\frac{\left(\frac{T}{T_{nom}} - 1\right) 1.11}{\mathbf{NR}\, V_T}\right) \quad \textbf{(J-17)}$$

$$\mathbf{PB}(T) = \mathbf{PB}\frac{T}{T_{non}} - 3V_T \ln\left(\frac{T}{T_{non}}\right) - 1.11\frac{T}{T_{non}} + 1.16 - 0.000702\,\frac{T^2}{T + 1108} \quad \textbf{(J-18)}$$

$$\mathbf{CGS}(T) = \mathbf{CGS}\left\{1 + \mathbf{M}\left[0.0004\left(T - T_{nom}\right) + \left(1 - \frac{\mathbf{PB}(T)}{\mathbf{PB}}\right)\right]\right\} \quad \textbf{(J-19)}$$

$$\mathbf{CGD}(T) = \mathbf{CGD}\left\{1 + \mathbf{M}\left[0.0004\left(T - T_{nom}\right) + \left(1 - \frac{\mathbf{PB}(T)}{\mathbf{PB}}\right)\right]\right\} \quad \textbf{(J-20)}$$

In the JFET model, series ohmic resistances RS and RD are not temperature-dependent.

Thermal Noise

$$I_{RSn}^2 = Rarea\,\frac{4kT}{\mathbf{RS}}\,BW \quad \textbf{(J-21)}$$

$$I_{RDn}^2 = Rarea\,\frac{4kT}{\mathbf{RD}}\,BW \quad \textbf{(J-22)}$$

Shot and flicker noise

$$I_{Dn}^2 = \left(I_{shot}^2 + I_{flicker}^2\right) BW \quad \textbf{(J-23)}$$

$$I_{shot}^2 = 2\,q\,I_D \quad \textbf{(J-24)}$$

$$I_{flicker}^2 = \frac{\mathbf{KF}\, I_D^{\mathbf{AF}}}{Freq} \quad \textbf{(J-25)}$$

Both bandwidth *BW* and frequency *Freq* are expressed in Hz. Thermal noise is generated by the series resistance. The parameter *Rarea* indicates that for a transistor with large relative area, the actual resistance is smaller. Shot noise is proportional to the drain current, as shown by Eq. (J-24). Flicker noise dominates at low frequencies. It increases with the current level and is inversely proportional to the frequency, as shown by Eq. (J-25). The flicker noise source is described by two parameters, **KF** and **AF**.

M - MOS Transistor

MOS Transistor Models

.MODEL *Model_name* **NMOS** [*Model parameters*]
.MODEL *Model_name* **PMOS** [*Model parameters*]

A large number of MOS transistor models are used. These models are distinguished by the keyword LEVEL and a number. Some SPICE implementations (i.e. AIM-SPICE) have up to 20 different levels of MOS models. In this section three basic levels (1, 2, and 3), which are implemented in all SPICE versions, and the newer BSIM models, which are also becoming a standard, are described.

LEVEL=1	Shichman-Hodges model [1] [8]	All SPICE implementations
LEVEL=2	Geometric based analytical Meyer model [2] [8]	All SPICE implementations
LEVEL=3	Semi-empirical short channel Dang model [3] [8]	All SPICE implementations
LEVEL=4	BSIM1 (Berkeley Short Channel Igfet Model) [4] [9]	SPICE3 and new PSPICE
LEVEL=5	BSIM2 Jeng model [5] [9]	SPICE3
LEVEL=5	BSIM3 (version 1) [6] [9]	New PSPICE
LEVEL=6	BSIM3 (version 2) [6] [9]	new PSPICE
LEVEL=6	MOS6 Sakurai-Newton model [7]	SPICE3

1. Parameters of MOS transistor models

Common for all Levels				
Name	*Parameter description*	*Unit*	*Default*	*Typical*
LEVEL	Model index	-	1	
L	Default channel length (PSPICE only)	m	DEFL	100µ
W	Default channel width (PSPICE only)	m	DEFL	100µ
RD	Drain ohmic resistance	Ω	0	5
RS	Source ohmic resistance	Ω	0	5
RG	Gate ohmic resistance (PSPICE only)	Ω	0	5
RB	Bulk/substrate ohmic resistance (PSPICE only)	Ω	0	5
CBD	Zero-bias bulk-drain junction capacitance	F	0	20 fF
CBS	Zero-bias bulk-source junction capacitance	F	0	20 fF
IS	Bulk junction saturation current	A	10^{-14}	$3 \cdot 10^{-15}$
JS	Bulk junction saturation current per sq-meter of junction area	A/m^2	0	10^{-8}

JSSW	Bulk junction saturation current per length of sidewall area (PSPICE only)	A/m	0	10^{-12}
N	Bulk junction emission coefficient (PSPICE only)	-	1	1
PB	Bulk junction potential	V	0.8	0.85
PBSW	Bulk junction sidewall potential (PSPICE only)	V	**PB**	0.85
CGSO	Gate-source overlap capacitance per meter channel width	F/m	0	$3{\cdot}10^{-11}$
CGDO	Gate-drain overlap capacitance per meter channel width	F/m	0	$3{\cdot}10^{-11}$
CGBO	Gate-bulk overlap capacitance per meter channel length	F/m	0	$3{\cdot}10^{-10}$
RSH	Drain and source diffusion sheet resistance	Ω/	0	10
CJ	Zero-bias bulk junction bottom capacitance per square meter of junction area	F/m^2	0	$2{\cdot}10^{-4}$
CJSW	Zero-bias bulk junction sidewall capacitance per length of sidewall	F/m	0	10^{-8}
MJ	Bulk junction bottom grading coefficient	-	0.5	0.5
CJSW	Zero-bias bulk junction sidewall capacitance per meter of junction perimeter (PSPICE only)	F/m	0	10^{-9}
MJSW	Bulk junction sidewall grading coefficient (PSPICE only)	-	0.50 (Level 1) 0.33 (Level 2, 3)	
TT	Bulk junction transit time (PSPICE only)	s	0	10^{-8}
KF	Flicker noise coefficient	-	0	10^{-26}
AF	Flicker noise exponent	-	1.0	1.2
FC	Coefficient for forward-bias depletion capacitance formula	-	0.5	0.5
TNOM	Nominal temperature which overwrites the value specified in **.OPTION** statement (SPICE3 only)	K	300	300

Level 1, 2, 3, and 6 (Sakurai-Newton)				
Name	*Parameter description*	*Unit*	*Default*	*Typical*
VTO	Zero-bias threshold voltage	V	0	1.0
KP	Transconductance parameter	A/V^2	$2 \cdot 10^{-5}$	$3 \cdot 10^{-5}$
GAMMA	Bulk threshold parameter	$V^{0.5}$	0	0.35
PHI	Surface potential	V	0.6	0.65
LAMBDA	Channel-length modulation parameter (level 1 and level 2 only)	1/V	0	0.02
TOX	Oxide thickness	m	10^{-7}	10^{-7}
NSUB	Substrate doping	cm^{-3}	0	$5 \cdot 10^{15}$
NSS	Surface state density	$cm-^{2}$	0	$2 \cdot 10^{10}$
NFS	Fast surface state density	$cm-^{2}$	0	10^{10}
TPG	Type of gate material (+1 for opposite to substrate, -1 for same as substrate, and 0 for Al gate)	-	1	1
XJ	Metallurgical junction depth	m		1u
LD	Lateral diffusion	m	0	0.7u
WD	Lateral diffusion width (PSPICE only)	m	0	0.5u
UO	Surface mobility	$cm^2/V\text{-}s$	600	700
UCRIT	Critical field for mobility degradation (level 2 only)	V/cm	10^4	10^4
UEXP	Critical field exponent in mobility degradation (level 2 only)	-	0	0.1
UTRA	Transverse field coefficient (mobility) (deleted for level 2)	-	0	0.3
VMAX	Maximum drift velocity of carriers	m/s	0	$3 \cdot 10^4$
NEFF	Total channel charge (fixed and mobile) coefficient (level 2 only)	-	1.0	3.0
XQC	Thin-oxide capacitance model flag and a fraction of channel charge attributed to drain (0-0.5)	-	1	0.4
DELTA	Width effect on threshold voltage	-	0	1.0
THETA	Mobility modulation (level 3 only)	1/V	0	0.1
ETA	Static feedback (level 3 only)	-	0	1.0
KAPP	Saturation field factor (level 3 only)	-	0.2	0.5

Transistor parameters may often be specified in different ways. For example, the reverse current can be specified either with the **IS** parameter ([in A) or with **JS** (in A/m^2). The first choice is an absolute value, while the second choice is multiplied by **AD** and **AS** to give the reverse current at the drain and source junctions, respectively. The latter approach is preferred. The same is also true for the parameters **CBD**, **CBS.** and **CJ**. Parasitic resistances can be given with **RD** and **RS** (in Ω) or with **RSH** [in Ω/]. **RSH** is multiplied by number of squares **NRD** and **NRS**.

In the case of BSIM parameters for **LEVEL**=4 there are no default values, and all parameters must be specified. Also, some parameters, marked with an asterisk "*" in the following Table, have channel length/width dependencies. For each of these parameters, two additional parameters should be specified. For example, if a parameter has name **PNAM** then two additional parameters **LPNAM** and **WPNAM** should be specified. The actual parameter value is calculated using

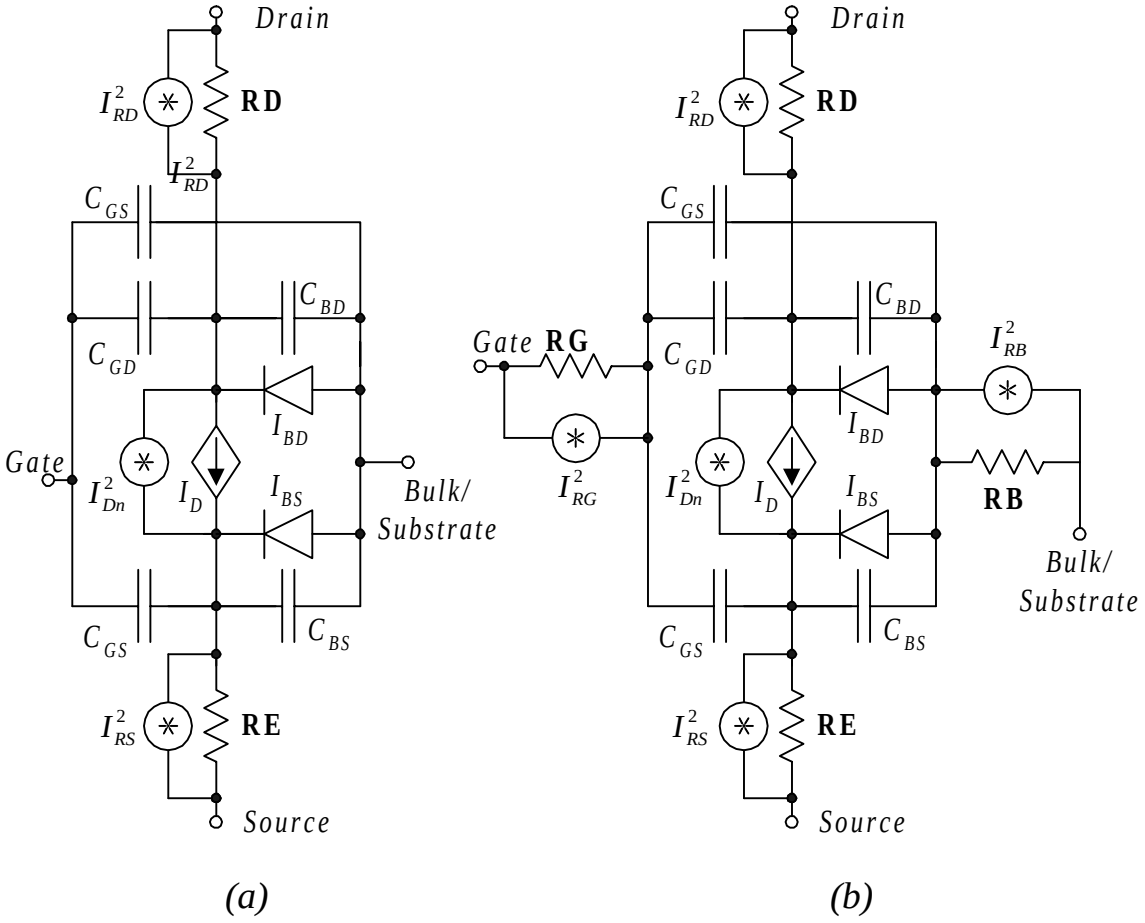
$$\mathbf{PNAM} = \mathbf{PNAM} + \frac{\mathbf{LPNAM}}{\mathbf{L} - \mathbf{DL}} + \frac{\mathbf{WPNAM}}{\mathbf{W} - \mathbf{DW}}$$

where **L** and **W** are channel length and width specified in the device line. Level 4 parameters were designed for automatic parameter extraction, and all model parameters should be copied from the device extractor rather than entered manually.

Level 4 - BSIM1			
Name	*Parameter description*	*Unit*	*L/W*
TOX	Gate oxide thickness	μm	
VFB	Flat-band voltage	V	*
PHI	Surface inversion potential	V	*
K1	Body effect coefficient		*
K2	Drain/source depletion charge sharing coefficient	-	*
DL	Shortening of channel	μm	
DW	Narrowing of channel	μm	
N0	Zero-bias subthreshold slope coefficient	-	*
NB	Sensitivity of subthreshold slope to substrate bias	-	*
ND	Sensitivity of subthreshold slope to drain bias	-	*
VDD	Measurement bias range	V	
MUS	Mobility at zero substrate bias and at V_{DS} = **VDD**	cm^2/V·s	
X2MS	Sensitivity of mobility to substrate bias at V_{DS} = **VDD**	cm^2/V^2·s	*
X3MS	Sensitivity of mobility to drain bias at V_{DS} = **VDD**	cm^2/V^2·s	*

MUZ	Zero-bias mobility	$cm^2/V{\cdot}s$	
X2MZ	Sensitivity of mobility to substrate bias at V_{DS}=0	$cm^2/V^2{\cdot}s$	*
U0	Zero-bias transverse-field mobility degradation coefficient	$1/V$	*
X2U0	Sensitivity of transverse field mobility degradation effect to substrate bias	$1/V^2$	*
U1	Zero-bias velocity saturation coefficient	$\mu m/V$	*
X2U1	Sensitivity of velocity saturation effect to substrate bias	$\mu m/V^2$	*
X3U1	Sensitivity of velocity saturation effect on drain bias at V_{DS} = **VDD**	$\mu m/V^2$	*
WDF	Source-drain junction default width	m	
DELL	Source-drain junction length reduction	m	
TEMP	Temperature at which parameters are measured	^oC	
ETA	Zero-bias drain-induced barrier-lowering coefficient	-	*
X2E	Sensitivity of drain-induced barrier-lowering effect to substrate bias	1/V	*
X3E	Sensitivity of drain-induced barrier-lowering effect to drain bias at V_{DS} = **VDD**	1/V	*
XPART	Gate-oxide capacitance charge model flag. **XPART** = 0 selects a 40/60 drain/source partition of the gate charge in saturation, while **XPART** = 1 selects a 0/100 drain/source charge partition.	-	

2. Equivalent diagrams



The model diagrams for a MOS transistor in *(a)* SPICE2/3 and *(b)* PSPICE

Terminal voltages used in equations	
V_{GS}	Intrinsic gate-source voltage
V_{GD}	Intrinsic base-drain voltage
V_{DS}	Intrinsic drain-source voltage
V_{BS}	Intrinsic bulk-source voltage
V_{BD}	Intrinsic bulk-drain voltage
Other parameters such as V_T, q, ε_o, ε_{ox}, ε_{si}, T, and T_{nom} are defined in the introductory section of Chapter 6.	

3. Model equations for level 1 (Shichman-Hodges)

dc Currents for Level-1

$$I_{Gate} = 0 \qquad \textbf{(M-1)}$$

$$I_{Bulk} = I_{BS} + I_{BD} \qquad \textbf{(M-2)}$$

$$I_{BS} = I_{SS}\left[\exp\left(\frac{V_{BS}}{N V_T}\right) - 1\right] \qquad \textbf{(M-3)}$$

$$I_{BD} = I_{DS}\left[\exp\left(\frac{V_{BD}}{N V_T}\right) - 1\right] \qquad \textbf{(M-4)}$$

if **JS** = 0 or **AS** = 0 or **AD** = 0 then: $I_{SS} = 0$ and $I_{DS} = 0$ **(M-5)**
otherwise:

$$I_{SS} = \textbf{AS JS} + \textbf{PS JSSW} \qquad \textbf{(M-6)}$$

$$I_{DS} = \textbf{AD JS} + \textbf{PD JSSW} \qquad \textbf{(M-7)}$$

$$I_{Drain} = I_D - I_{BG} \qquad \textbf{(M-8)}$$

$$I_{Source} = -I_D - I_{BS} \qquad \textbf{(M-9)}$$

For $V_{DS} \geq 0$ (normal mode) and V_{GS}-$V_{TO} < 0$ (cutoff region):

$$I_D = 0 \qquad \textbf{(M-10)}$$

For $V_{DS} \geq 0$ (normal mode) and $V_{DS} < V_{GS}$- V_{TO} (linear region):

$$I_D = \frac{\textbf{W}}{L_{eff}}\frac{\textbf{KP}}{2}\left(1 + \textbf{LAMBDA}\, V_{DS}\right)V_{DS}\left[2\left(V_{GS} - V_{TO}\right) - V_{DS}\right] \qquad \textbf{(M-11)}$$

For $V_{DS} \geq 0$ (normal mode) and $V_{DS} > V_{GS}$- V_{TO} (saturation region):

$$I_D = \frac{\textbf{W}}{L_{eff}}\frac{\textbf{KP}}{2}\left(1 + \textbf{LAMBDA}\, V_{DS}\right)\left(V_{GS} - V_{TO}\right)^2 \qquad \textbf{(M-12)}$$

$$V_{TO} = \textbf{VTO} + \textbf{GAMMA}\left(\sqrt{\textbf{PHI} - V_{BS}} - \sqrt{\textbf{PHI}}\right) \qquad \textbf{(M-13)}$$

$$L_{eff} = \textbf{L} - 2\,\textbf{LD} \qquad \textbf{(M-14)}$$

For $V_{DS} < 0$ (inverted mode), the source and drain terminals are switched and Eqs. **(M-1)** through **(M-13)** are used.

If technological parameters (**TOX** - oxide thickness, **UO** - carrier mobility, **NSUB** - substrate impurity concentration) are specified instead of implicit values of **KP**, **GAMMA**, and **PHI**, then **KP**, **GAMMA**, and **PHI** are calculated using the following equations:

$$\mathbf{KP} = \mathbf{UP}\, C_{OX} \qquad \textbf{(M-15)}$$

$$\mathbf{GAMMA} = \frac{\sqrt{2\, q\, \varepsilon_o\, \varepsilon_{si}\, \mathbf{NSUB}}}{C_{OX}} \qquad \textbf{(M-16)}$$

$$\mathbf{PHI} = \max\left[2V_T \ln\left(\frac{\mathbf{NSUB}}{n_i}\right), 0.1\right] \qquad \textbf{(M-17)}$$

$$C_{OX} = \frac{\varepsilon_o\, \varepsilon_{ox}}{\mathbf{TOX}} \qquad \textbf{(M-18)}$$

$$n_i(T) = 1.4510^{10}\left(\frac{T}{300}\right)^{1.5} \exp\left[\frac{1.16\left(\frac{T}{300}\right) - E_G(T)}{V_T}\right] \quad \left[\mathrm{cm}^{-3}\right] \qquad \textbf{(M-19)}$$

$$E_G(T) = 1.16 - \frac{0.000702\, T^2}{T + 1108} \qquad \textbf{(M-20)}$$

Capacitances for level 1

All capacitances are defined between the intrinsic terminals of the MOS transistor:

For **CBS**=0 $\quad C_{BS} = X_{BSJ}\mathbf{AS}\,\mathbf{CJ} + X_{BSS}\mathbf{PS}\,\mathbf{CJSW} + \mathbf{TT}\, G_{BS}$ **(M-21)**

otherwise $\quad C_{BS} = X_{BSJ}\mathbf{CBS} + X_{BSS}\mathbf{PS}\,\mathbf{CJSW} + \mathbf{TT}\, G_{BS}$ **(M-22)**

For **CBD**=0 $\quad C_{BD} = X_{BDJ}\mathbf{AD}\,\mathbf{CJ} + X_{BDS}\mathbf{PD}\,\mathbf{CJSW} + \mathbf{TT}\, G_{DS}$ **(M-23)**

otherwise $\quad C_{BD} = X_{BDJ}\mathbf{CBD} + \mathbf{PD}\,\mathbf{CJSW}\, C_{BDS} + \mathbf{TT}\, G_{DS}$ **(M-24)**

$$G_{BS} = \frac{I_{BS}}{\mathbf{N}\, V_T} \quad \text{for } V_{BS} > 0 \quad \text{and} \quad G_{BS} = 0 \quad \text{otherwise} \qquad \textbf{(M-25)}$$

$$G_{BD} = \frac{I_{BD}}{\mathbf{N}\, V_T} \quad \text{for } V_{BD} > 0 \quad \text{and} \quad G_{BD} = 0 \quad \text{otherwise} \qquad \textbf{(M-26)}$$

For $V_{BS} \leq$ **FC PB**:

$$X_{BSJ} = \left(1 - \frac{V_{BS}}{\mathbf{PB}}\right)^{-\mathbf{MJ}} \quad \textbf{(M-27)}$$

$$X_{BSS} = \left(1 - \frac{V_{BS}}{\mathbf{PBSW}}\right)^{-\mathbf{MJSW}} \quad \textbf{(M-28)}$$

otherwise

$$X_{BSJ} = (1 - \mathbf{FC})^{-(1+\mathbf{MJ})}\left[1 - \mathbf{FC}\,(1+\mathbf{MJ}) + \mathbf{MJ}\,\frac{V_{BS}}{\mathbf{PB}}\right] \quad \textbf{(M-29)}$$

$$X_{BSS} = (1 - \mathbf{FC})^{-(1+\mathbf{MJSW})}\left[1 - \mathbf{FC}\,(1+\mathbf{MJSW}) + \mathbf{MJSW}\,\frac{V_{BS}}{\mathbf{PBSW}}\right] \quad \textbf{(M-30)}$$

For $V_{BD} \leq$ **FC PB**:

$$X_{BDJ} = \left(1 - \frac{V_{BD}}{\mathbf{PB}}\right)^{-\mathbf{MJ}} \quad \textbf{(M-31)}$$

$$X_{BDS} = \left(1 - \frac{V_{BD}}{\mathbf{PBSW}}\right)^{-\mathbf{MJSW}} \quad \textbf{(M-32)}$$

otherwise

$$X_{BDJ} = (1 - \mathbf{FC})^{-(1+\mathbf{MJ})}\left[1 - \mathbf{FC}\,(1+\mathbf{MJ}) + \mathbf{MJ}\,\frac{V_{BD}}{\mathbf{PB}}\right] \quad \textbf{(M-33)}$$

$$X_{BDS} = (1 - \mathbf{FC})^{-(1+\mathbf{MJSW})}\left[1 - \mathbf{FC}\,(1+\mathbf{MJSW}) + \mathbf{MJSW}\,\frac{V_{BD}}{\mathbf{PBSW}}\right] \quad \textbf{(M-34)}$$

$$C_{GS} = \mathbf{CGSO\ W} \quad \textbf{(M-35)}$$

$$C_{GD} = \mathbf{CGDO\ W} \quad \textbf{(M-36)}$$

$$C_{GB} = \mathbf{CGBO\ L} \quad \textbf{(M-37)}$$

Temperature Effects

$$\mathbf{IS}(T) = \mathbf{IS}\,\exp\left[\frac{\mathbf{EG}\,\dfrac{T}{T_{nom}} - E_G(T)}{V_T}\right] \quad \textbf{(M-38)}$$

$$\mathbf{JS}(T) = \mathbf{JS}\exp\left[\frac{\mathbf{EG}\dfrac{T}{T_{nom}} - E_G(T)}{V_T}\right] \quad \textbf{(M-39)}$$

$$\mathbf{JSSW}(T) = \mathbf{JSSW}\exp\left[\frac{\mathbf{EG}\dfrac{T}{T_{nom}} - E_G(T)}{V_T}\right] \quad \textbf{(M-40)}$$

$$\mathbf{PB}(T) = \mathbf{PB}\frac{T}{T_{nom}} - 3V_T\ln\left(\frac{T}{T_{nom}}\right) - \mathbf{EG}\frac{T}{T_{nom}} + E_G(T) \quad \textbf{(M-41)}$$

$$\mathbf{PBSW}(T) = \mathbf{PBSW}\frac{T}{T_{nom}} - 3V_T\ln\left(\frac{T}{T_{nom}}\right) - \mathbf{EG}\frac{T}{T_{nom}} + E_G(T) \quad \textbf{(M-42)}$$

$$\mathbf{PHI}(T) = \mathbf{PHI}\frac{T}{T_{nom}} - 3V_T\ln\left(\frac{T}{T_{nom}}\right) - \mathbf{EG}\frac{T}{T_{nom}} + E_G(T) \quad \textbf{(M-43)}$$

$$\mathbf{CBD}(T) = \mathbf{CBD}\left\{1 + \mathbf{MJ}\left[0.0004\left(T - T_{nom}\right) + \left(1 - \frac{\mathbf{PB}(T)}{\mathbf{PB}}\right)\right]\right\} \quad \textbf{(M-44)}$$

$$\mathbf{CBS}(T) = \mathbf{CBS}\left\{1 + \mathbf{MJ}\left[0.0004\left(T - T_{nom}\right) + \left(1 - \frac{\mathbf{PB}(T)}{\mathbf{PB}}\right)\right]\right\} \quad \textbf{(M-45)}$$

$$\mathbf{CJ}(T) = \mathbf{CJ}\left\{1 + \mathbf{MJ}\left[0.0004\left(T - T_{nom}\right) + \left(1 - \frac{\mathbf{PB}(T)}{\mathbf{PB}}\right)\right]\right\} \quad \textbf{(M-46)}$$

$$\mathbf{CJSW}(T) = \mathbf{CJSW}\left\{1 + \mathbf{MJSW}\left[0.0004\left(T - T_{nom}\right) + \left(1 - \frac{\mathbf{PB}(T)}{\mathbf{PB}}\right)\right]\right\} \quad \textbf{(M-47)}$$

$$\mathbf{KP}(T) = \mathbf{KP}\left(\frac{T}{T_{nom}}\right)^{-\frac{3}{2}} \quad \textbf{(M-48)}$$

$$\mathbf{UO}(T) = \mathbf{UO}\left(\frac{T}{T_{nom}}\right)^{-\frac{3}{2}} \quad \textbf{(M-49)}$$

$$\mathbf{MUS}(T) = \mathbf{MUS}\left(\frac{T}{T_{nom}}\right)^{-\frac{3}{2}} \quad \textbf{(M-50)}$$

$$\mathbf{MUZ}(T) = \mathbf{MUZ}\left(\frac{T}{T_{nom}}\right)^{-\frac{3}{2}} \quad \textbf{(M-51)}$$

$$\mathbf{X3MS}(T) = \mathbf{X3MS}\left(\frac{T}{T_{nom}}\right)^{-\frac{3}{2}} \quad \textbf{(M-52)}$$

The temperature dependencies of the saturation currents **IS**, **JS**, and **JSSW** are determined by the energy-gap, **EG**. The temperature dependencies of the saturation currents are given by Eqs. (M-38) through (M-40). Ohmic resistances are assumed to be temperature independent. The temperature dependence of depletion capacitances incorporates the changes of built-in potentials and changes of the silicon energy gap, as it is shown in equations (M-41) through (M-47).

Thermal Noise

$$I_{RD}^2 = \frac{4kT}{\mathbf{RD}}\,BW \quad \textbf{(M-53)}$$

$$I_{RS}^2 = \frac{4kT}{\mathbf{RS}}\,BW \quad \textbf{(M-54)}$$

$$I_{RG}^2 = \frac{4kT}{\mathbf{RG}}\,BW \quad \textbf{(M-55)}$$

$$I_{RB}^2 = \frac{4kT}{\mathbf{RB}}\,BW \quad \textbf{(M-56)}$$

Thermal noise is generated by series resistances. Only PSPICE uses gate **RG** and bulk **RB** resistances.

Shot and Flicker Noise

$$I_{Dn}^2 = \left(I_{D\_shot}^2 + I_{D\_flicker}^2\right) BW \quad \textbf{(M-57)}$$

$$I_{D\_shot}^2 = \frac{8\,k\,T}{3}\,g_m \quad \textbf{(M-58)}$$

$$g_m = \frac{d\,I_D}{d\,V_{GS}} \quad \textbf{(M-59)}$$

$$I_{D\_flicker}^2 = \frac{\mathbf{KF}\ I_D^{\mathbf{AF}}}{K_{CHAN} Freq} \qquad \textbf{(M-60)}$$

$$K_{CHAN} = \frac{\varepsilon_{ox}\ \mathbf{L}_{eff}^2}{\mathbf{TOX}} \approx \frac{4.0\,\mathbf{L}_{eff}^2}{\mathbf{TOX}} \qquad \textbf{(M-61)}$$

Both *BW* (bandwidth) and *Freq* (frequency) are expressed in Hz. Shot and flicker noises are a function of the device current. The shot noise is proportional to the junction current, as shown by Eq. (M-57) and (M-58). Flicker noise dominates at low frequency. It increases with the current level and is inversely proportional to the frequency, as shown by Eq. (M-60). Flicker noise is described by the two parameters **KF** and **AF**.

4. Model equations for level 2 (Meyer)

The level 2 model is much more accurate than the Shichman-Hodges model used in level 1. The following additional phenomena are taken into consideration in the Level 2 model:

- A nonuniform charge distribution in the depletion layer between channel and substrate is used. Equations for level 1 were derived with an assumption of constant voltage between the channel and substrate, which is never valid (unless the source is shorted in drain).
- The subthreshold conduction phenomenon is introduced in which a small drain current may exist even for gate-source voltages smaller than the threshold voltage.
- Carrier mobility variation with the electrical field is used. In particular, the effect of carrier velocity saturation is modeled.
- The narrow channel effect is incorporated into the model.
- The nonlinear character of capacitances between gate and source, and drain and substrate, is included in the model.

dc Currents for Level 2

For $V_{GS} < V_{ON}$ (subthreshold conduction) :

$$I_D = I_{ON}\ \exp\left(\frac{V_{GS} - V_{ON}}{n\,V_T}\right) \qquad \textbf{(M-62)}$$

$$V_{ON} = V_{TO} + n\,V_T \qquad \textbf{(M-63)}$$

$$n = 1 + \frac{q\,\mathbf{NFS}}{V_{GS} C_{OX}} + \frac{\mathbf{GAMMA}}{2\sqrt{\mathbf{PHI} - V_{BS}}} \qquad \textbf{(M-64)}$$

If **VTO** and GAMMA are not defined, the threshold voltage can be calculated from technological parameters:

$$V_{TO} = V_{MS} - \frac{q\,\mathbf{NSS}}{C_{OX}} + \mathbf{PHI} + \mathbf{GAMMA}\ \sqrt{\mathbf{PHI}} \qquad \textbf{(M-65)}$$

$$V_{MS} = -\mathbf{TPG}\frac{E_G(T)}{2} - V_T \ln\left(\frac{\mathbf{NSUB}}{n_i(T)}\right) \quad \textbf{(M-66)}$$

For $V_{GS} > V_{ON}$ and $0 < V_{DS} < V_{SAT}$ (linear region):

$$I_D = \frac{\mathbf{KP}\ \mathbf{W}}{L_{eff} - \Delta L}\left\{\left(V_{GS} - V_{fb} - \mathbf{PHI} - \frac{V_{DS}}{2}\right)V_{DS} - \right.$$
$$\left. - \frac{2}{3}\mathbf{GAMMA}\left[\left(V_{DS} - V_{BS} + \mathbf{PHI}\right)^{1.5} - \left(\mathbf{PHI} - V_{BS}\right)^{1.5}\right]\right\} \quad \textbf{(M-67)}$$

$$V_{fb} = V_{MS} + \frac{q\,\mathbf{NSS}}{C_{OX}} \quad \textbf{(M-68)}$$

$$L_{eff} = \left(\mathbf{L} - 2\,\mathbf{LD}\right) \quad \textbf{(M-69)}$$

$$\Delta L = L_{eff}\left(1 - \mathbf{LAMBDA}\,V_{DS}\right) \quad \textbf{(M-70)}$$

$$V_{SAT} = V_{GS} - V_{fb} - \mathbf{PHI} + \frac{\mathbf{GAMMA}^2}{2}\left[1 - \sqrt{1 + \frac{4\left(V_{GS} - V_{fb} - V_{BS}\right)}{\mathbf{GAMMA}^2}}\right] \quad \textbf{(M-71)}$$

For $V_{GS} > V_{ON}$ and $V_{DS} > V_{SAT}$ (saturation region):

$$I_D = \frac{I_{SAT}}{1 - \mathbf{LAMBDA}\,V_{DS}} \quad \textbf{(M-72)}$$

where I_{SAT} is computed using the linear region equation (M-67) by setting $V_{DS} = V_{SAT}$.

The effect of mobility degradation is modeled using **UCRIT**, **ULTRA**, **UEXP**, and **TOX** parameters:

$$\mathbf{KP} = \mathbf{KP}\left(\frac{\varepsilon_{si}}{\varepsilon_{ox}}\frac{\mathbf{UCRIT}\ \ \mathbf{TOX}}{V_{GS} - V_{TO} - \mathbf{ULTRA}\,V_{DS}}\right)^{\mathbf{UEXP}} \quad \textbf{(M-73)}$$

When LAMBDA is not specified, its value can be calculated using technological parameters with the formula:

$$\Delta L = L_{eff}\,\mathbf{LAMBDA}\,V_{DS} = H_D\sqrt{\frac{V_{DS} - V_{SAT}}{4} + \sqrt{\left(\frac{V_{DS} - V_{SAT}}{4}\right)^2 + 1}} \quad \textbf{(M-74)}$$

$$H_D = \sqrt{\frac{2\,\varepsilon_o\,\varepsilon_{si}}{\mathbf{NEFF}\;q\;\mathbf{NSUB}}} \qquad \textbf{(M-75)}$$

The above equation is not accurate and usually results in a larger value of **LAMBDA** than the actual one. When the **VMAX** parameter is specified, better results can be obtained using the Baum-Beneking model, especially for transistors with channel length longer than 4 to 5 μm:

$$\Delta L = L_{eff}\,\mathbf{LAMBDA}\,V_{DS} = H_D\sqrt{\sqrt{\left(\frac{X_D\;\mathbf{VMAX}}{2\;\mathbf{UO}}\right)^2 + \left(V_{DS} - V_{SAT}\right)^2} - \frac{X_D\;\mathbf{VMAX}}{2\;\mathbf{UO}}} \qquad \textbf{(M-76)}$$

Although the Baum-Beneking model is more accurate, it has noncontinuous derivatives and often leads to numerical instability. For small transistor geometries, with **L** or **W** below 5 μm, both **L** and **W** affect the transistor threshold voltage. This effect is modeled by calculating **GAMMA** as a function of **L** and **W**:

$$\mathbf{GAMMA} = \mathbf{GAMMA}\left[1 - \frac{\mathbf{XJ}}{2\;L_{eff}}\left(\sqrt{1 + \frac{2\;W_D}{\mathbf{XJ}}} + \sqrt{1 + \frac{2\;W_S}{\mathbf{XJ}}} - 2\right)\right] \qquad \textbf{(M-77)}$$

$$W_S = \sqrt{\frac{2\,\varepsilon_o\,\varepsilon_{si}}{q\;\mathbf{NSUB}}}\;\sqrt{\mathbf{PHI} - V_{BS}} \qquad \textbf{(M-78)}$$

$$W_D = \sqrt{\frac{2\,\varepsilon_o\,\varepsilon_{si}}{q\;\mathbf{NSUB}}}\;\sqrt{\mathbf{PHI} - V_{BS} + V_{DS}} \qquad \textbf{(M-79)}$$

Equation (M-78) usually results in a larger than actual value of the **GAMMA** parameter. Therefore an additional experimentally chosen parameter **DELTA** is introduced, and the threshold voltage is calculated using

$$V_{TO} = \mathbf{VTO} + \mathbf{GAMMA}\left(\sqrt{\mathbf{PHI} - V_{BS}} - \sqrt{\mathbf{PHI}}\right) + \\ + \frac{\pi\,\varepsilon_o\,\varepsilon_{Si}\;\mathbf{DELTA}}{4\;C_{OX}\;\mathbf{W}}\left(\mathbf{PHI} - V_{BS}\right) \qquad \textbf{(M-80)}$$

Capacitances for Level 2

For the level 2 model, junction capacitances are calculated the same way as in the level 1 model Eqs. (M-21) through (M-37). Only capacitances associated with the gate are calculated differently.

For $V_{GS} < V_{ON}$ - **PHI** (accumulation region):

$$C_{GB} = C_{GOX} + \mathbf{CGBO}\,L_{eff} \qquad \textbf{(M-81)}$$

$$C_{GS} = C_{GOX} + \mathbf{CGSO}\;\mathbf{W} \qquad \textbf{(M-82)}$$

$$C_{GD} = C_{GOX} + \mathbf{CGDO}\ \mathbf{W} \quad \textbf{(M-83)}$$

$$C_{GOX} = C_{OX}\ \mathbf{W}\ L_{eff} \quad \textbf{(M-84)}$$

For V_{ON} **- PHI** $< V_{GS} < V_{ON}$ (depletion region):

$$C_{GB} = C_{GOX}\frac{V_{ON} - V_{GS}}{\mathbf{PHI}} + \mathbf{CGBO}\, L_{eff} \quad \textbf{(M-85)}$$

$$C_{GS} = \frac{2}{3}C_{GOX}\left(\frac{V_{ON} - V_{GS}}{\mathbf{PHI}} + 1\right) + \mathbf{CGSO\ W} \quad \textbf{(M-86)}$$

$$C_{GD} = C_{GOX} + \mathbf{CGDO}\ \mathbf{W} \quad \textbf{(M-87)}$$

For $V_{ON} < V_{GS} < V_{ON} + V_{DS}$ (saturation region):

$$C_{GB} = \mathbf{CGBO}\, L_{eff} \quad \textbf{(M-88)}$$

$$C_{GS} = \frac{2}{3}C_{GOX} + \mathbf{CGSO\ W} \quad \textbf{(M-89)}$$

$$C_{GD} = \mathbf{CGDO}\ \mathbf{W} \quad \textbf{(M-90)}$$

For $V_{GS} > V_{ON} + V_{DS}$ (linear region):

$$C_{GB} = \mathbf{CGBO}\, L_{eff} \quad \textbf{(M-91)}$$

$$C_{GS} = C_{GOX}\left\{1 - \left[\frac{V_{GS} - V_{DS} - V_{ON}}{2\left(V_{GS} - V_{ON}\right) - V_{DS}}\right]^2\right\} + \mathbf{CGSO\ W} \quad \textbf{(M-92)}$$

$$C_{GD} = C_{GOX}\left\{1 - \left[\frac{V_{GS} - V_{ON}}{2\left(V_{GS} - V_{ON}\right) - V_{DS}}\right]^2\right\} + \mathbf{CGDO\ W} \quad \textbf{(M-93)}$$

5. Model equations for level 3 (Dang model)

dc Currents for Level 3

$$I_D = \beta\left(V_{GS} - V_{TO} - \frac{1 + F_B}{2}V_{DS}\right)V_{DS} \quad \textbf{(M-94)}$$

Transistor current in the saturation region is obtained by substituting $V_{DS} = V_{SAT}$ in Eq. (M-94).

$$F_B = \frac{\mathbf{GAMMA}\ F_s}{1\sqrt{\mathbf{PHI} - V_{BS}}} + F_n \qquad \textbf{(M-95)}$$

$$F_s = 1 - \left[\frac{\mathbf{LD} + W_c}{L_{eff}} \sqrt{1 - \left(\frac{W_p}{\mathbf{XJ} + W_p} \right)^2} - \frac{\mathbf{LD}}{L_{eff}} \right] \qquad \textbf{(M-96)}$$

$$W_p = \sqrt{\frac{2\ \varepsilon_o\ \varepsilon_{si}}{q\ \mathbf{NSUB}\ \ \mathbf{NEFF}}}\ \sqrt{\mathbf{PHI} - V_{BS}} \qquad \textbf{(M-97)}$$

$$W_c = 0.0831353\,\mathbf{XJ} + 0.8013929\,W_p - 0.0111077\frac{W_p^2}{\mathbf{XJ}} \qquad \textbf{(M-98)}$$

$$\beta = \frac{\mathbf{W}}{L_{eff} - \Delta L}\ \frac{\mu_{eff}}{\mathbf{UO}}\mathbf{KP} \qquad \textbf{(M-99)}$$

The level 3 model includes mobility degradation due to both transverse (source-drain) and perpendicular (gate-substrate) electrical fields:

$$\mu_{eff} = \frac{\mu_s}{1 + \dfrac{\mu_s\ V_{DS}}{\mathbf{VMAX}\ L_{eff}}} \qquad \textbf{(M-100)}$$

Surface mobility μ_s degradation due to the perpendicular electrical field is modeled by

$$\mu_s = \frac{\mathbf{UO}}{1 + \mathbf{THETA}\left(V_{GS} - V_{TO}\right)} \qquad \textbf{(M-101)}$$

$$V_{SAT} = V_a + V_b - \sqrt{V_a^2 + V_b^2} \qquad \textbf{(M-102)}$$

$$V_a = \frac{V_{GS} - V_{TO}}{1 + F_B} \qquad \textbf{(M-103)}$$

$$V_b = \frac{\mathbf{VMAX}\ L_{eff}}{\mu_{eff}} \qquad \textbf{(M-104)}$$

where μ_{eff} represents the effective carrier mobility which is reduced by both the perpendicular electrical field (gate-substrate) and the carrier velocity limitation.

The threshold voltage formula includes the additional effect of electrostatic interaction drain potential which effectively lowers the threshold voltage. This effect becomes especially visible for short-channel transistors.

$$V_{TO} = V_{fb} + \mathbf{PHI} - \sigma\,V_{DS} + \mathbf{GAMMA}\ F_s\sqrt{\mathbf{PHI} - V_{BS}} + F_n\left(\mathbf{PHI} - V_{BS}\right) \qquad \textbf{(M-105)}$$

$$V_{MS} = -\mathbf{TPG}\frac{E_G(T)}{2} - V_T \ln\left(\frac{\mathbf{NSUB}}{n_i(T)}\right) \quad \textbf{(M-106)}$$

$$\sigma = \mathbf{ETA}\frac{8.15\ 10^{-22}}{C_{OX} L_{eff}^3} \quad \textbf{(M-107)}$$

$$F_n = \frac{\pi\ \varepsilon_o\ \varepsilon_{Si}\ \mathbf{DELTA}}{4\ C_{OX}\ \mathbf{W}} \quad \textbf{(M-108)}$$

Channel-length modulation is computed only in the saturation region, $V_{DS} > V_{SAT.}$

$$\Delta L = \sqrt{\left(\frac{E_p\ H_D^2}{2}\right)^2 + \mathbf{KAPPA}\ H_D^2\left(V_{DS} - V_{SAT}\right)} - \frac{E_p\ H_D^2}{2} \quad \textbf{(M-109)}$$

$$E_p = \frac{I_{SAT}}{G_{SAT}\ L(V_{DS})} \quad \textbf{(M-110)}$$

where I_{SAT} and G_{SAT} are the drain current and drain conductance at $V_{DS} = V_{SAT}$.

6. Model equations for level 4 (BISIM1 model)

dc Currents for Level 4

For $V_{GS} > V_{TO}$ and $0 < V_{DS} < V_{SAT}$ (linear region):

$$I_D = \frac{\mu_o}{1 + U_0\left(V_{GS} - V_{TO}\right)}\frac{C_{OX}\ W_{eff}}{L_{eff} + U_1\ V_{DS}}\left[\left(V_{GS} - V_{TO}\right)V_{DS} - \frac{a\ V_{DS}^2}{2}\right] \quad \textbf{(M-111)}$$

$$V_{TO} = V_{fb} + \mathbf{PHI} - \sigma\ V_{DS} + \mathbf{K1}\ F_s\sqrt{\mathbf{PHI} - V_{BS}} + \mathbf{K2}\left(\mathbf{PHI} - V_{BS}\right) - \eta V_{DS} \quad \textbf{(M-112)}$$

$$\eta = \mathbf{N0} + \mathbf{NB}\ V_{BS} + \mathbf{ND}\left(V_{DS} - \mathbf{VDD}\right) \quad \textbf{(M-113)}$$

$$a = 1 + \frac{g\ \mathbf{K1}}{2\sqrt{\mathbf{PHI} - V_{BS}}} \quad \textbf{(M-114)}$$

$$g = 1 - \frac{1}{1.744 + 0.8364\left(\mathbf{PHI} - V_{BS}\right)} \quad \textbf{(M-115)}$$

$$U_0 = \mathbf{U0} + \mathbf{X2U0}\ V_{BS} \quad \textbf{(M-116)}$$

$$U_1 = \mathbf{U1} + \mathbf{X2U1}V_{BS} + \mathbf{X3U1}\left(V_{DS} - \mathbf{VDD}\right) \quad \textbf{(M-117)}$$

Mobility μ_o is approximated by a quadratic polynomial between points

$$\mu_o(V_{DS} = 0) = \mathbf{MUZ} + \mathbf{X2MZ}\,V_{BS} \quad \textbf{(M-118)}$$

and

$$\mu_o(V_{DS} = \mathbf{VDD}) = \mathbf{MUS} + \mathbf{X2MS}\,V_{BS} \quad \textbf{(M-119)}$$

using the sensitivity of μ_o to the drain bias **X3MS** at (V_{DS} = **VDD**) to set the proper second derivative. Therefore

$$\begin{aligned}\mu_o = &\left(\frac{\mathbf{X3MS}}{\mathbf{VDD}} - \frac{\mathbf{MUS} + \mathbf{X2MS}\,V_{BS}}{\mathbf{VDD}^2}\right)V_{DS}^2 + \\ &+\left(\frac{2\,\mathbf{MUS} + \mathbf{X2MS}\,V_{BS}}{\mathbf{VDD}} - \mathbf{X3MS}\right)V_{DS} + \mathbf{MUZ} + \mathbf{X2MZ}\,V_{BS}\end{aligned} \quad \textbf{(M-120)}$$

For $V_{GS} > V_{TO}$ and $V_{DS} \geq V_{SAT}$ (saturation region):

$$I_D = \frac{\mu_o}{1 + U_0\left(V_{GS} - V_{TO}\right)}\frac{C_{OX}\,W_{eff}}{2\,a\,L_{eff}\,K}\left(V_{GS} - V_{TO}\right)^2 \quad \textbf{(M-121)}$$

$$K = \frac{1 + v_c + \sqrt{1 + 2v_c}}{2} \quad \textbf{(M-122)}$$

$$v_c = \frac{U_1}{L_{eff}}\frac{\left(V_{GS} - V_{TO}\right)}{a} \quad \textbf{(M-123)}$$

For $V_{GS} \leq V_{TO}$ (subthreshold conduction - weak inversion region), the total drain current for all gate biasing is calculated as a sum of current for the strong inversion case [Eqs. (M-111) and (M-121)] and an additional component I_{DW} due to the subthreshold conduction in the weak inversion region.

$$I_D = I_D + I_{DW} \quad \textbf{(M-124)}$$

$$I_{DW} = \frac{I_{\exp}\,I_{limit}}{I_{\exp} + I_{limit}} \quad \textbf{(M-125)}$$

$$I_{\exp} = \mu_o C_{OX}\,\frac{W_{eff}}{L_{eff}}V_T^2\exp\left(1.8 + \frac{V_{GS} - V_{TO}}{n\,V_T}\right)\left[1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right] \quad \textbf{(M-126)}$$

$$I_{limit} = \frac{\mu_o C_{OX}}{2} \frac{W_{eff}}{L_{eff}} \left(3V_T\right)^2 \quad \textbf{(M-127)}$$

$$n = \mathbf{NO} + \mathbf{NB}\, V_{BS} + \mathbf{ND}\, V_{DS} \quad \textbf{(M-128)}$$

The BSIM1 model works well for devices with channel length larger than 1 μm. For modern transistors with submicrometer channel length, the BSIM1 model does not work well. Problems are mainly with subthreshold conduction. The BSIM2 model developed by Jeng [5] is a modification of the BSIM1 model. The BSIM2 model is useful for MOS transistors with channel length as short as 0.2 μm. For the BSIM2 and BISIM3 models, see references [5-6] and [9-11].

A simplified transistor model as described by Sakurai and Newton [7] is implemented as level 6 in SPICE3.

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Q - Bipolar Transistor

Bipolar Transistor Models

.MODEL *Model_name* **NPN** [*Model parameters*]
.MODEL *Model_name* **PNP** [*Model parameters*]
.MODEL *Model_name* **LPNP** [*Model parameters*] PSPICE only

The **LPNP** keyword indicates a special model for the lateral *pnp* transistor implemented in PSPICE only.

1. Parameters of bipolar transistor model

Name	*Parameter description*	*Unit*	*Default*	*Typical*
IS	Saturation current for *Rarea*=1	A	10^{-16}	10^{-15}
ISE	*B-E* leakage saturation current for *Rarea*=1	A	0	10^{-12}
ICS	*B-C* leakage saturation current for *Rarea*=1	A	0	10^{-12}
BF	Forward current gain	-	100	100
BR	Reverse current gain	-	1	0.1
NF	Forward current emission coefficient	-	1.0	1.2
NR	Reverse current emission coefficient	-	1.0	1.3
NE	B-E leakage emission coefficient	-	1.5	1.4
NC	B-C leakage emission coefficient	-	1.5	1.4
VAF	Forward Early voltage	V	∞	100
VAR	Reverse Early voltage	V	∞	50
IKF	$ß_F$ high current roll-off corner	A	∞	0.05
IKR	$ß_R$ high current roll-off corner	A	∞	0.01
IRB	Current where base resistance falls by half for *Rarea*=1	A	∞	0.1
RB	Zero-bias base resistance	Ω	0	100
RBM	Minimum base resistance	Ω	**RB**	10
RE	Emitter series resistance for *Rarea*=1	Ω	0	1
RC	Collector series resistance for *Rarea*=1	Ω	0	50
CJE	*B-E* zero-bias depletion capacitance	F	0	10^{-12}
CJC	*B-C* zero-bias depletion capacitance	F	0	10^{-12}

CJS	Zero-bias collector-substrate capacitance	F	0	10^{-12}
VJE	*B-E* built-in potential	V	0.75	0.8
VJC	*B-C* built-in potential	V	0.75	0.7
VJS	Substrate junction built-in potential	V	0.75	0.7
MJE	*B-E* junction exponential factor	-	0.33	0.33
MJC	*B-C* junction exponential factor	-	0.33	0.5
MJS	Substrate junction exponential factor	-	0	0.5
XCJC	Fraction of *B-C* capacitance connected to internal base node (see Fig. 6)	-	0	0.5
TF	Forward transit time	s	0	10^{-10}
TR	Reverse transit time	s	0	10^{-8}
XTF	Coefficient for bias dependence of τ_F	-	0	-
VTF	Voltage for t_F dependence on V_{BC}	V	∞	-
ITF	Current where $t_F = f(I_C,V_{BC})$ starts	A	0	-
PTF	Excess phase at $freq = 1/(2pt_F)$ Hz	deg	0	-
XTB	Forward and reverse beta temperature exponent		0	-
EG	Energy gap	eV	1.11	1.1
XTI	Temperature exponent for effect on I_s	-	3	3.5
KF	Flicker noise coefficient	-	0	
AF	Flicker noise exponent	-	1	
FC	Coefficient for the forward biased depletion capacitance formula	-	0.5	0.5
SPICE3 extension				
TNOM	Nominal temperature which overrides the value specified in **.OPTION** statement	K	300	300
PSPICE extensions				
NK	High-current roll-off coefficient	-	0.5	0.5
ISS	Substrate saturation current for *Rarea*=1	A	0	10^{-15}
NS	Substrate emission coefficient	-	1	1
QCO	Epitaxial layer charge factor for *Rarea*=1	C	0	
RCO	Epitaxial region resistance for *Rarea*=1	Ω	0	100
VO	Carrier mobility knee voltage	V	10	20
GAMMA	Epitaxial layer doping factor		10^{-11}	10^{-11}

TRE1	**RE** temperature coefficient (linear)	1/°C	0	0.001
TRE2	**RE** temperature coefficient (quadratic)	1/°C^2	0	0
TRB1	**RB** temperature coefficient (linear)	1/°C	0	0.002
TRB2	**RB** temperature coefficient (quadratic)	1/°C^2	0	0
TRM1	**RBM** temperature coefficient (linear)	1/°C	0	0.002
TRM2	**RBM** temperature coefficient (quadratic)	1/°C^2	0	0
TRC1	**RC** temperature coefficient (linear)	1/°C	0	0.003
TRC2	**RC** temperature coefficient (quadratic)	1/°C^2	0	0

2. Equivalent diagram

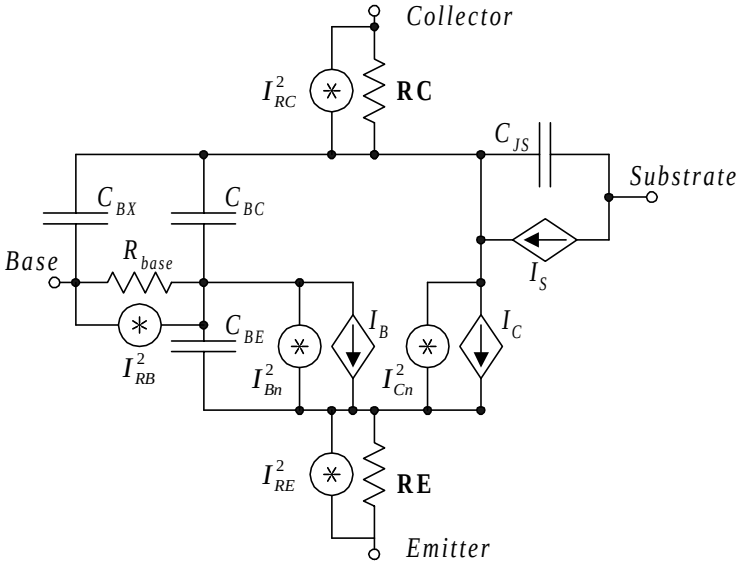


Fig. Q-1. The model diagram for an **NPN** bipolar transistor. In the case of the **PNP** transistor the directions of current sources are reversed. In the case of the **LPNP** the substrate is coupled (by I_S and C_{JS}) with the internal base instead of the internal collector.

Terminal voltages used in equations	
V_{BE}	intrinsic base-emitter voltage
V_{BC}	intrinsic base-collector voltage
V_{BS}	intrinsic base-substrate voltage
V_{BW}	intrinsic base-extrinsic collector voltage
V_{BX}	extrinsic base-intrinsic collector voltage
V_{CE}	intrinsic collector-emitter voltage
V_{JS}	intrinsic collector-substrate voltage (**NPN**) intrinsic substrate-collector voltage (**PNP**) intrinsic base-substrate voltage (**LPNP**)
Other parameters such as V_T, T, and T_{nom} are defined in the introductory section.	

3. Model equations

dc Currents

$$I_B = Rarea\left(\frac{I_{forward\_diff}}{\mathbf{BF}} + I_{forward\_gener} + \frac{I_{reverse\_diff}}{\mathbf{BR}} + I_{reverse\_gener}\right) \quad \textbf{(Q-1)}$$

$$I_C = Rarea\left(\frac{I_{forward\_diff} - I_{reverse\_diff}}{K_{base\_charge}} - \frac{I_{reverse\_diff}}{\mathbf{BR}} - I_{reverse\_gener}\right) \quad \textbf{(Q-2)}$$

$$I_{forward\_diff} = \mathbf{IS}\left[\exp\left(\frac{V_{BE}}{\mathbf{NF}\,V_T}\right) - 1\right] \quad \textbf{(Q-3)}$$

$$I_{forward\_gener} = \mathbf{ISE}\left[\exp\left(\frac{V_{BE}}{\mathbf{NE}\,V_T}\right) - 1\right] \quad \textbf{(Q-4)}$$

$$I_{reverse\_diff} = \mathbf{IS}\left[\exp\left(\frac{V_{BC}}{\mathbf{NR}\,V_T}\right) - 1\right] \quad \textbf{(Q-5)}$$

$$I_{reverse\_gener} = \mathbf{ISC}\left[\exp\left(\frac{V_{BC}}{\mathbf{NC}\,V_T}\right) - 1\right] \quad \textbf{(Q-6)}$$

$$K_{base\_charge} = \frac{2}{1 - \frac{V_{BC}}{\mathbf{VAF}} - \frac{V_{BE}}{\mathbf{VAR}}}\left\{1 + \left[1 + 4\left(\frac{I_{forward\_diff}}{\mathbf{IKF}} + \frac{I_{reverse\_diff}}{\mathbf{IKR}}\right)\right]^{\mathbf{NK}}\right\} \quad \textbf{(Q-7)}$$

$$I_S = \mathbf{ISS}\left[\exp\left(\frac{V_{JC}}{\mathbf{NS}\,V_T}\right) - 1\right] \quad \textbf{(Q-8)}$$

$$R_{base} = \begin{cases} \dfrac{\mathbf{RBM} + \dfrac{\mathbf{RB} - \mathbf{RBM}}{K_{base\_charge}}}{Rarea} & \text{for } \mathbf{IRB} = \infty \text{ (default)} \\ \dfrac{\mathbf{RBM} + 3\,(\mathbf{RB} - \mathbf{RBM})\dfrac{\tan(x) - x}{x\tan^2(x)}}{Rarea} & \text{for } \mathbf{IRB} > 0 \end{cases} \quad \textbf{(Q-9)}$$

$$x = \frac{\sqrt{1 + \frac{144}{\pi^2}\frac{I_B}{Area\ \mathbf{IRB}}} - 1}{\frac{24}{\pi^2}\sqrt{\frac{I_B}{Area\ \mathbf{IRB}}}} \quad \textbf{(Q-10)}$$

Gummel and Poon observed that the saturation current **IS** in modern narrow base-transistors has the same value for forward and reverse operation; see Eqs. (Q-3) and (Q-5). They have also noticed that only the collector current has a truly exponential function of V_{BE} over a wide range of magnitudes. The base and emitter currents are calculated from the collector current using the current gain coefficients β_F and β_R, which are functions of a current level; see Eq. (Q-1). This basic Gummel-Poon model is extended to include several effects at high bias levels. At low currents, the effect of thermal carrier generation must be included; see Eqs. (Q-4) and (Q-6). For high current levels, when the charge of carriers injected into the base becomes comparable to the fixed charge of base impurities, the gain of a transistor degrades significantly; see Eq. (Q-7). Equation (Q-7) also incorporates the Early effect using the Early voltages **VAF** and **VAR**. Output conductances for forward and reverse operation are imposed by Eq. (Q-7).

The parameters **IS**, **BF**, **NF**, **ISE**, **IKF**, and **NE** determine the forward transistor characteristics, while **IS**, **BR**, **NR**, **ISC**, **IKR**, and **NC** determine the reverse transistor characteristics. **RB**, **RC**, and **RE** are series terminal resistances. The base resistance is a function of the current level due to the "current crowding" effect. For proper modeling, additional parameters **RBM** and **IRB** are required - see Eqs. (Q-9) and (Q-10). Note that the base resistance is also a function of the normalized base charge K_{base_charge} as given by equation (Q-7).

Capacitances

$$C_{BE} = C_{BE\_transit} + Rarea\ C_{BE\_depletion} \qquad \textbf{(Q-11)}$$

$$C_{BE\_transit} = G_{BE}\,\mathbf{TF}\left[1+\mathbf{XTF}\left(\frac{I_{forward\_diff}}{I_{forward\_diff}+Area\ \mathbf{ITF}}\right)^2\right]\exp\left(\frac{V_{BC}}{1.44\,\mathbf{VTF}}\right) \qquad \textbf{(Q-12)}$$

$$G_{BE} = \frac{\partial}{\partial V_D}\left(I_{forward\_diff}+I_{forward\_gener}\right) \approx \frac{I_C}{\mathbf{N}_{eff}\ V_T} \qquad \textbf{(Q-13)}$$

$$C_{BE\_depletion} = \begin{cases} \mathbf{CJE}\left(1-\dfrac{V_{BE}}{\mathbf{VJE}}\right)^{-\mathbf{MJE}} & \text{for } V_{BE} \le \mathbf{FC}\ \mathbf{VJE} \\ \mathbf{CJE}\,(1-\mathbf{FC})^{-(1+\mathbf{MJE})}\left[1-\mathbf{FC}\,(1+\mathbf{MJE})+\dfrac{\mathbf{MJE}\,V_{BE}}{\mathbf{VJE}}\right] & \text{for } V_{BE} > \mathbf{FC}\ \mathbf{VJE} \end{cases} \qquad \textbf{(Q-14)}$$

$$C_{BC} = C_{BC\_transit} + Rarea\ \mathbf{XCJC}\ C_{BC\_depletion} \qquad \textbf{(Q-15)}$$

$$C_{BC\_transit} = \mathbf{TR}\ \frac{\partial}{\partial V_D}\left(I_{reverse\_diff}+I_{reverse\_gener}\right) \qquad \textbf{(Q-16)}$$

$$C_{BC\_depletion} = \begin{cases} \text{for } V_{BC} \le \mathbf{FC}\ \mathbf{VJC} \\ \mathbf{CJC}\left(1-\dfrac{V_{BE}}{\mathbf{VJC}}\right)^{-\mathbf{MJC}} \\ \\ \text{for } V_{BC} > \mathbf{FC}\ \mathbf{VJC} \\ \mathbf{CJC}\,(1-\mathbf{FC})^{-(1+\mathbf{MJC})}\left[1-\mathbf{FC}\,(1+\mathbf{MJC})+\dfrac{\mathbf{MJC}\,V_{BE}}{\mathbf{VJC}}\right] \end{cases} \quad \textbf{(Q-17)}$$

$$C_{BX} = Rarea\,(1-\mathbf{XCJC})\,C_{BX\_depletion} \quad \textbf{(Q-18)}$$

$$C_{BX\_depletion} = \begin{cases} \text{for } V_{BX} \le \mathbf{FC}\ \mathbf{VJC} \\ \mathbf{CJC}\left(1-\dfrac{V_{BX}}{\mathbf{VJC}}\right)^{-\mathbf{MJC}} \\ \\ \text{for } V_{BX} > \mathbf{FC}\ \mathbf{VJC} \\ \mathbf{CJC}\,(1-\mathbf{FC})^{-(1+\mathbf{MJC})}\left[1-\mathbf{FC}\,(1+\mathbf{MJC})+\dfrac{\mathbf{MJC}\,V_{BX}}{\mathbf{VJC}}\right] \end{cases} \quad \textbf{(Q-19)}$$

$$C_{JS} = Rarea\ \ C_{JS\_depletion} \quad \textbf{(Q-20)}$$

$$C_{JS\_depletion} = \begin{cases} \mathbf{CJS}\left(1-\dfrac{V_{JS}}{\mathbf{VJS}}\right)^{-\mathbf{MJS}} & \text{for } V_{JS} \le 0 \\ \mathbf{CJS}\left(1+\dfrac{\mathbf{MJS}\,V_{JS}}{\mathbf{VJS}}\right) & \text{for } V_{JS} > 0 \end{cases} \quad \textbf{(Q-21)}$$

Each junction capacitance has two components: $C_{transit}$ which is proportional to the forward junction current; and $C_{depletion}$, which changes with voltage as the depletion-layer thickness changes. Similar formulas are used for both the base-emitter and the base-collector junction; see Eqs. (Q-11) and (Q-15). In the case of the substrate junction, only the depletion capacitance is calculated because it is assumed that this junction is always biased in the reverse direction; see Eq. (Q-20). Transit capacitances are always proportional to storage times **TF** and **TR** and to the small-signal junction conductances, which are proportional to the junction currents; see Eqs. (Q-12), (Q-13), and (Q-16). For normal operation, the basic equation for $C_{BE\_transit}$ is modified to include the transit-time dependence of current and voltage biasing conditions, as shown in Eq. (Q-12).

Depletion capacitances are functions of the junction voltages; Eqs. (Q-14), (Q-17), (Q-19), and (Q-21). Parameters **CJE**, **VJE**, **MJE**, and the **FC** are used for base-emitter junction. Parameters **CJC**, **VJC**, **MJC**, **XCJC**, and **FC** are used for the base-collector junction. Parameters **CJS**, **VJS**, and **MJS** are used for the collector-substrate junction (base-substrate junction in the case of **LPNP**).

Quasi-saturation Effect

The quasi-saturation effect, known also as the Kirk effect, occurs when internal base-collector junction is forward biased while the external base-collector junction is reverse-biased. In order to model this effect, the **RCO, QCO** and **GAMMA** parameters must be specified. A detailed description of this effect can be found in G. M. Kull, L. W. Nagel, S. W. Lee, P. Lloyd, E. J. Prendergast, and H. K. Dirks, "A Unified Circuit Model for Bipolar Transistors Including Quasi-Saturation Effects," *IEEE Trans. on Electron Devices*, **ED-32**, 1103-1113 (1985).

Temperature Effects

$$\mathbf{IS}(T) = \mathbf{IS}\left(\frac{T}{T_{nom}}\right)^{\mathbf{XTI}} \exp\left[\frac{\left(\frac{T}{T_{nom}} - 1\right)\mathbf{EG}}{V_T}\right] \qquad \textbf{(Q-22)}$$

$$\mathbf{ISE}(T) = \mathbf{ISE}\left(\frac{T}{T_{nom}}\right)^{\mathbf{XTB}}\left(\frac{T}{T_{nom}}\right)^{\frac{\mathbf{XTI}}{\mathbf{NE}}} \exp\left[\frac{\left(\frac{T}{T_{nom}} - 1\right)\mathbf{EG}}{\mathbf{NE}\,V_T}\right] \qquad \textbf{(Q-23)}$$

$$\mathbf{ISC}(T) = \mathbf{ISC}\left(\frac{T}{T_{nom}}\right)^{\mathbf{XTB}}\left(\frac{T}{T_{nom}}\right)^{\frac{\mathbf{XTI}}{\mathbf{NC}}} \exp\left[\frac{\left(\frac{T}{T_{nom}} - 1\right)\mathbf{EG}}{\mathbf{NC}\,V_T}\right] \qquad \textbf{(Q-24)}$$

$$\mathbf{ISS}(T) = \mathbf{ISS}\left(\frac{T}{T_{nom}}\right)^{\mathbf{XTB}}\left(\frac{T}{T_{nom}}\right)^{\frac{\mathbf{XTI}}{\mathbf{NS}}} \exp\left[\frac{\left(\frac{T}{T_{nom}} - 1\right)\mathbf{EG}}{\mathbf{NS}\,V_T}\right] \qquad \textbf{(Q-25)}$$

$$\mathbf{BF}(T) = \mathbf{BF}\left(\frac{T}{T_{nom}}\right)^{\mathbf{XTB}} \qquad \textbf{(Q-26)}$$

$$\mathbf{BR}(T) = \mathbf{BR}\left(\frac{T}{T_{nom}}\right)^{\mathbf{XTB}} \qquad \textbf{(Q-27)}$$

$$\mathbf{RE}(T) = \mathbf{RE}\left[1 + \mathbf{TRE1}\left(T - T_{nom}\right) + \mathbf{TRE2}\left(T - T_{nom}\right)^2\right] \qquad \textbf{(Q-28)}$$

$$\mathbf{RC}(T) = \mathbf{RC}\left[1 + \mathbf{TRC1}\left(T - T_{nom}\right) + \mathbf{TRC2}\left(T - T_{nom}\right)^2\right] \qquad \textbf{(Q-29)}$$

$$\mathbf{RB}(T) = \mathbf{RB}\left[1 + \mathbf{TRB1}\left(T - T_{nom}\right) + \mathbf{TRB2}\left(T - T_{nom}\right)^2\right] \quad \textbf{(Q-30)}$$

$$\mathbf{RBM}(T) = \mathbf{RBM}\left[1 + \mathbf{TRM1}\left(T - T_{nom}\right) + \mathbf{TRM2}\left(T - T_{nom}\right)^2\right] \quad \textbf{(Q-31)}$$

$$\mathbf{CJE}(T) = \mathbf{CJE}\left\{1 + \mathbf{MJE}\left[0.0004\left(T - T_{nom}\right) + \left(1 - \frac{\mathbf{VJE}(T)}{\mathbf{VJE}}\right)\right]\right\} \quad \textbf{(Q-32)}$$

$$\mathbf{CJC}(T) = \mathbf{CJC}\left\{1 + \mathbf{MJC}\left[0.0004\left(T - T_{nom}\right) + \left(1 - \frac{\mathbf{VJC}(T)}{\mathbf{VJC}}\right)\right]\right\} \quad \textbf{(Q-33)}$$

$$\mathbf{CJS}(T) = \mathbf{CJS}\left\{1 + \mathbf{MJS}\left[0.0004\left(T - T_{nom}\right) + \left(1 - \frac{\mathbf{VJS}(T)}{\mathbf{VJS}}\right)\right]\right\} \quad \textbf{(Q-34)}$$

$$\mathbf{VJE}(T) = \mathbf{VJE}\frac{T}{T_{nom}} - 3V_T \ln\left(\frac{T}{T_{nom}}\right) - \mathbf{EG}\frac{T}{T_{nom}} + 1.16 - 0.000702\frac{T^2}{T + 1108} \quad \textbf{(Q-35)}$$

$$\mathbf{VJC}(T) = \mathbf{VJC}\frac{T}{T_{nom}} - 3V_T \ln\left(\frac{T}{T_{nom}}\right) - \mathbf{EG}\frac{T}{T_{nom}} + 1.16 - 0.000702\frac{T^2}{T + 1108} \quad \textbf{(Q-36)}$$

$$\mathbf{VJS}(T) = \mathbf{VJS}\frac{T}{T_{nom}} - 3V_T \ln\left(\frac{T}{T_{nom}}\right) - \mathbf{EG}\frac{T}{T_{nom}} + 1.16 - 0.000702\frac{T^2}{T + 1108} \quad \textbf{(Q-37)}$$

The temperature dependence of the saturation currents **IS**, **ISE**, **ISC**, and **ISS** is determined by the energy gap **EG**, the saturation current temperature exponents **XTI** and **XTB**, and the emission coefficients **NE**, **NC**, and **NS**. The temperature dependence of the saturation currents is given by Eq. (Q-22) through **(**Q-25**)**. Equations (Q-26) and (Q-27) model the temperature dependence of the current gain using the **XTB** parameter. Ohmic resistances are described by linear and quadratic approximation as shown in Eqs. (Q-28) through (Q-31**)**. The temperature dependence of the depletion capacitances incorporates the changes of built-in potentials and changes of the silicon energy gap, as shown in Eqs. (Q-32) through (Q-37).

Thermal Noise

$$I_{RE}^2 = Rarea\frac{4kT}{\mathbf{RE}}BW \quad \textbf{(Q-38)}$$

$$I_{RC}^2 = Rarea\frac{4kT}{\mathbf{RC}}BW \quad \textbf{(Q-39)}$$

$$I_{RB}^2 = \frac{4kT}{\mathbf{RB}}\, BW \qquad \textbf{(Q-40)}$$

Thermal noise is generated by the base, emitter, and collector series resistances. The parameter *Rarea* indicates that transistors with large relative areas have smaller collector and emitter resistances. This need not be the case for the base resistance.

Shot and Flicker Noise

$$I_{Bn}^2 = \left(I_{B\_shot}^2 + I_{B\_flicker}^2 \right) BW \qquad \textbf{(Q-41)}$$

$$I_{B\_shot}^2 = 2\, q\, I_B \qquad \textbf{(Q-42)}$$

$$I_{B\_flicker}^2 = \frac{\mathbf{KF}\, I_B^{\mathbf{AF}}}{Freq} \qquad \textbf{(Q-43)}$$

$$I_{Cn}^2 = 2\, q\, I_C\, BW \qquad \textbf{(Q-44)}$$

Both bandwidth *BW* and frequency *Freq* are expressed in Hz. The shot and flicker noise currents are functions of the device current. The shot noise is proportional to the junction current, as shown by Eq. (Q-42) and (Q-44). Flicker noise (1/*f* noise) dominates at low frequency. It increases with the current level and is inversely proportional to frequency, as shown by Eq. (Q-43). The flicker noise source is described by the two parameters **KF** and **AF**.

Z - MESFET SPICE3 only

MESFET Models

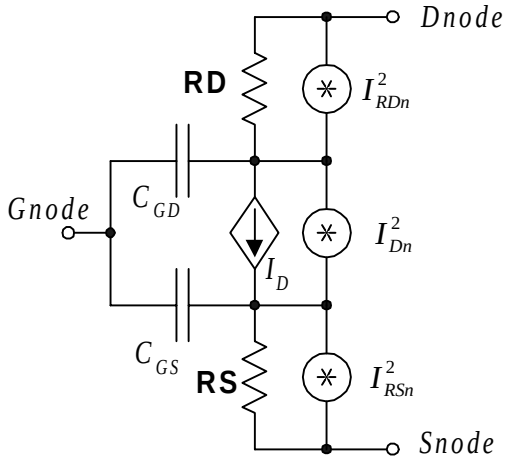
.MODEL *Model_name* **NMF** [*Model parameters*]
.MODEL *Model_name* **PMF** [*Model parameters*]

1. Model parameters

Name	*Parameter*	*Units*	*Default*	*Typical*	*Rarea*
VTO	Pinch-off voltage	V	-2.0	-2.0	
BETA	Transconductance parameter	A/V	1.0e-4	1.0e-3	*
B	Doping tail extending parameter	1/V	0.3	0.3	*
ALPHA	Saturation voltage parameter	1/V	2	2	*
LAMBDA	Channel-length modulation parameter	1/V	0	1.0e-4	
RD	Drain ohmic resistance	Ω	0	100	*
RS	Source ohmic resistance	Ω	0	100	*
CGS	Zero-bias *G-S* junction capacitance	F	0	5 pF	*
CGD	Zero-bias *G-D* junction capacitance	F	0	5 pF	*
PB	Gate junction potential	V	1	0.6	
KF	Flicker noise coefficient	-	0	-	
AF	Flicker noise exponent	-	1	-	
FC	Coefficient for forward-bias depletion capacitance formula	-	0.5	-	

Asterisks in the last column indicates that this parameter in all equations is multiplied by *Rarea* parameter specified in the **Z** device line.

2. Equivalent diagram



Terminal voltage used in equations	
V_{DS}	Intrinsic drain-source voltage
V_{GS}	Intrinsic gate-source voltage
Other parameters such as V_T, T, and T_{nom} are defined in the introductory section.	

3. Model equations

dc Currents

For $0 < V_{DS} < 3/\mathbf{ALPHA}$:

$$I_D = Rarea\frac{\mathbf{BETA}\left(V_{GS}-\mathbf{VTO}\right)^2}{1+\mathbf{B}\left(V_{GS}-\mathbf{VTO}\right)}\left[1-\left(1-\mathbf{ALPHA}\frac{V_{DS}}{3}\right)^3\right]\left(1+\mathbf{LAMBDA}\,V_{DS}\right) \qquad \textbf{(Z-1)}$$

For $V_{DS} \geq 3/\mathbf{ALPHA}$

$$I_D = Rarea\frac{\mathbf{BETA}\left(V_{GS}-\mathbf{VTO}\right)^2}{1+\mathbf{B}\left(V_{GS}-\mathbf{VTO}\right)}\left(1+\mathbf{LAMBDA}\,V_{DS}\right) \qquad \textbf{(Z-2)}$$

Capacitances

$$C_{GS} = Rarea\ \mathbf{CGS}\left(1-\frac{V_{GS}}{\mathbf{PB}}\right)^{-\mathbf{FC}} \qquad \textbf{(Z-3)}$$

$$C_{GD} = Rarea\ \mathbf{CGD}\left(1-\frac{V_{GD}}{\mathbf{PB}}\right)^{-\mathbf{FC}} \qquad \textbf{(Z-4)}$$

Noise

$$I_{RSn}^2 = Rarea\,\frac{4kT}{\mathbf{RS}}\,BW \qquad \textbf{(Z-5)}$$

$$I_{RDn}^2 = Rarea\,\frac{4kT}{\mathbf{RD}}\,BW \qquad \textbf{(Z-6)}$$

$$I_{Dn}^2 = \left(I_{shot}^2 + I_{flicker}^2\right) BW \qquad \textbf{(Z-7)}$$

$$I_{shot}^2 = 2\,q\,I_D \qquad \textbf{(Z-8)}$$

$$I_{flicker}^2 = \frac{\mathbf{KF}\ I_D^{\mathbf{AF}}}{Freq} \qquad \textbf{(Z-9)}$$

Both bandwidth *BW* and frequency *Freq* are expressed in Hz. Thermal noise is generated by the series resistance. The parameter *Rarea* indicates that for diodes with large relative area, the actual resistance is smaller. Shot noise is proportional to the drain current as shown by Eq. (Z-8). Flicker noise dominates at low frequencies. It increases with the current level and is inversely proportional to the frequency, as shown by Eq. (Z-9). The flicker noise source is described by two parameters, **KF** and **AF**.

A more detailed description of the MESFET model can be found in: H. Statz, P. Newman, I. W. Smith, R. A. Pucel, and H. A. Haus, "GaAs FET Device and Circuit Simulation in SPICE," *IEEE Trans. on Electron Devices* **ED-34**, pp. 160-169, February 1987.