A Review of Carbon Nanotube Field Effect Transistors

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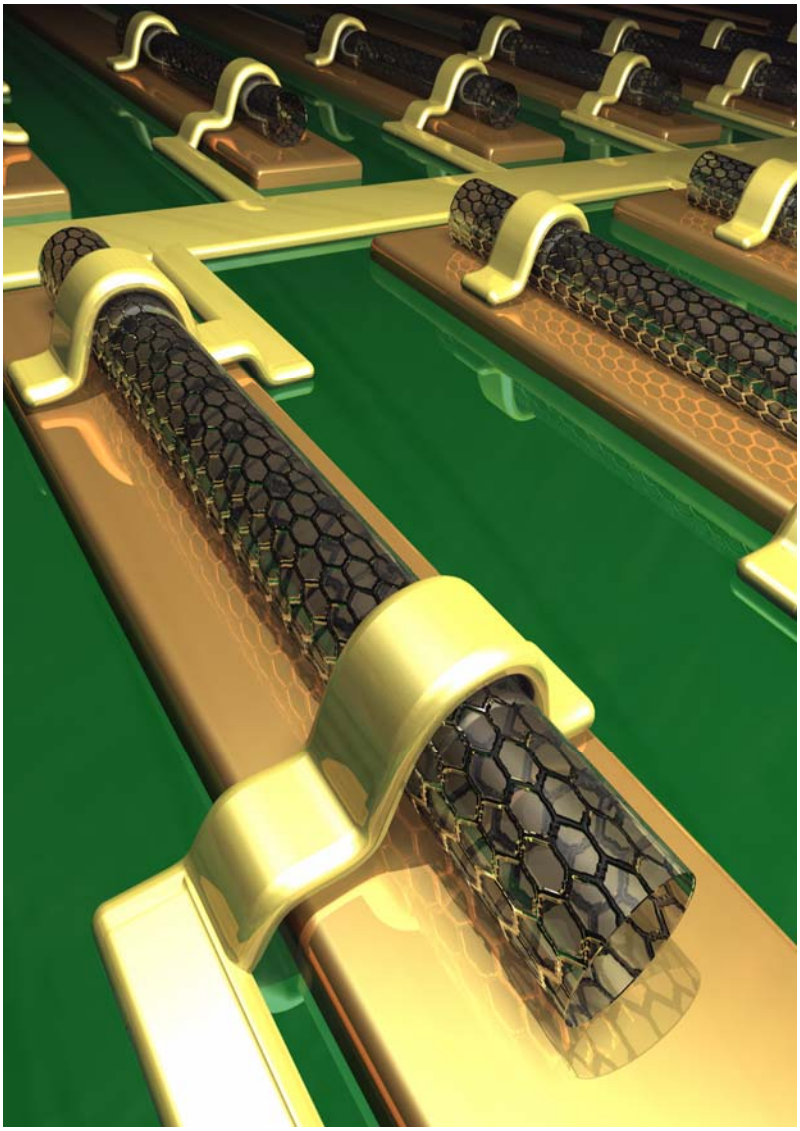

Array of Carbon Nanotube Transistors

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Foreword

Whenever an evolving technology approaches a dead end, a technological revolution is needed. The present VLSI electronic systems rely on the Silicon MOS (metal oxide semiconductor) technology whose advances will soon come to saturation. Carbon nanotubes represent advancement in the materials technology with potential for providing switching devices that may be faster and smaller than the present MOS devices.

Carbon nanotubes are miniature tube structures with intriguing characteristics. The tube, in the normal untwisted state, conducts electricity. When twisted, the tube acts as a semiconductor. In the coming years we should learn more about this new type of substance, construct switching devices and interconnects, and eventually make integrated circuits.

Alokik Kanwal approached me at the beginning of Spring 2003 semester. He wanted me to direct a study project on nanodevices. This project was not required since he had already graduated with a BS in EE in January 2003, but would prepare him to pursue his research interest. In the preceding fall semester he had completed a course on "Nanomaterial: Structural, Mechanical, and Chemical," taught by Professors W. Roger Cannon and Jun John Xu of the Department of Ceramic and Materials Engineering at Rutgers. He also completed a companion laboratory course. In the spring, he was auditing the course, "Photo, Electrical, and Magnetic Properties of Nanostructures," offered by Professors George H. Sigel and Manish Chhowalla of Ceramic and Materials Engineering.

The subject of nanodevices was new for both of us. We held regular discussions, some with the participation of another colleague, Tejaswi Raja. As the semester came to an end, it became clear that for this study to be useful to us and to others in the future we must document it.

This paper is a survey of the field of nanotube devices. Although the bibliography is not as large as one expects a survey to have, the cited references are easily accessible. Many are available through the Internet. The discussion emphasizes overview rather than the detail and a reader only requires the basic understanding of the semiconductor physics and MOS switching devices. The paper is written to initiate a new researcher in the field. A large number of topics are presented with details suppressed to stay within a manageable length. A reader can quickly find the area of greatest interest and then is advised to continue the study through the cited references.

I find that Alokik has made an excellent start in pursuing his chosen research interest. I hope this work will also help other young researchers to enter the field.

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Acknowledgment

I would like to thank Dr. Vishwani Agrawal for helping me put together this paper. In addition the discussions with Tejaswi Raja helped plan the paper. I would also like to thank Dr. Manish Chhowalla and Dr. George H. Sigel, who helped to in the understanding and review of this paper.

Abstract

With the decline of ability to improve the MOSFET technology in the next decade or so, there is a rush to try to find a replacement. Carbon nanotubes, which are sheets of graphene rolled up, are being investigated as replacements for silicon devices. This new class of transistors, known as carbon nanotube transistors, is one of the current leading technologies to replace MOSFETs. Despite the tremendous growth and progress, there are still difficult problems that need to be solved. Therefore, to help with the research, this paper surveys all the current research that has been done and outlines the future research that is needed to create large-scale VLSI chip utilizing carbon nanotube transistors

Contents

Introduction

1.1 Reasons for new type of Transistor

The transistor is considered one of the greatest inventions of the twentieth century. It has helped to bring about both the information and computing age. One reason for success is its ability to decrease in size and increase in speed. This property is summarized in Moore's law[1]. It states that the transistor's size will decrease exponentially while its speed will increase exponentially. Moore's law has allowed the technology sector to progress and remain competitive. Therefore, the continued success of the technology sector and our way of life depends on the continuation of Moore's law. However, both physical and economic barriers will inhibit our ability to continue Moore's law in the next decade or so. The physical barriers arise due to the continued shrinking of the current transistor used today, the Metal-Oxide Field Effect Transistor or MOSFET. As the size shrinks, the thickness of the insulators, which are used to electronically isolate parts of the transistor, reduces. With the thinner insulation, the carriers are able to quantum-mechanically tunnel across the insulation. The result is a short circuit allowing current to flow directly from source to drain, drain to the body, and even through the thin gate oxide, that separates the gate from the channel. In addition, doping becomes a problem since it relies on percentages. If the total amount of atoms gets very small then a fractional dopant atom might be required, which of course is impossible[2]. In addition, economic problems arise from producing and maintaining the fabrication lines. In 1996, the cost of a fabrication line was $1.5 billion and it is estimated that by 2006 to cost will be greater than $5 billion. One proposed solution is the use of carbon nanotubes instead of silicon to make the transistors.

1.2 The History

1.2.1 History of Carbon Nanotubes

The history of carbon nanotubes goes back farther than most people think. In fact, a US patent was given to two British men in 1889, on the production of carbon nanotubes utilizing marsh gas, otherwise known as methane. The method employed is essentially the same as used today. The patent describes the production of "hair-like carbon filaments" for electrical lighting. It also talked about some of the unique electrical and mechanical properties, "Carbon filament may be bent and twisted into various shapes and will spring back to their original form on being released."[2]

In 1960's a group at National Carbon Company in Parma, Ohio and later in the 1970's at and the University of Canterbury in Christchurch, New Zealand, helped to characterize the carbon nanotubes. Later in 1983, a company called Hyperion Catalysis perfected ways to produce nanotubes and began incorporating them into fuel line for cars. The nanotube's high conductivity would dissipate any electrical charge that could potential build up and spark. Today, 60 percent of the cars on the road use Hyperion's nanotube incorporated fuel lines. Hyperion's nanotubes are also incorporated into plastic

wing panels. This allows the plastic on the wing to be grounded and then sprayed with paint droplets that are charged up to 20,000 volts. The drops are attracted to the wing and stick, thus reducing the wasted paint that would normally mist away in the air.

The real love affair with carbon nanotubes began in 1991, when Sumino limijima and his colleagues created some nanotubes at the research laboratory of the electronics multinational NEC in Tsukulba, Japan[3].

1.2.2 History of Carbon Nanotube Transistors

Around 1998 the first transistors utilizing carbon nanotubes began to pop up. Their construction and operation is similar to the MOSFETs that we use today, thus giving them name Carbon Nanotube Field-Effect Transistor, or CNFET. This design was kept and experimented on until about 2002. IBM at this point comes out with a new optimized design, providing many characteristic improvements over the first generation CNFETs. Detailed information on both generation CNFETs and their differences will be discussed in section 3.

1.3 Comparison to Current Technology

Three of the most important characteristics of any transistor are speed, scalability, and power. These three characteristics are seen directly by the user, and thus are the make or break factors of any type of transistor. So in order for any new transistor to replace the current technology, silicon MOSFET, it much at least match, if not outperform, these three characteristics.

1.3.1 Speed

Thanks in part to the carbon nanotubes' unique one-dimensional nature; it is able to utilize ballistic transport. Ballistic transport means that the mean free path is longer than the path. Thus, the charge carriers do not collide, reducing resistance to negligible levels. The result is a capability to achieve speeds of Terahertz or more, compared to today's processors that operate at 3 gigahertz.

1.3.2 Scalability

A group in IBM discovered an interesting property of the CNFETs scalability. While the CNFETs improve with scaling, it is not conventional. They seem to follow the behavior of Schottky barrier MOSFETs, instead of regular MOSFETs. For this reason, the group at IBM feels that the CNFETs limits for scaling are unclear. However, they do note that, in a structured array, the CNFETs will produce enough gain and fan-out for real life applications. In addition, despite the CNFETs murky limits of scaling, it still will outperform silicon MOSFETs limits of scaling.[4]

1.3.3 Power

Table 1[5] – Comparison of CNFETs to both MOSFETs and SOI MOSFETs

	p-type		
	CNFET	MOSFET	SOI MOSFET
Gate length (nm)	260	15	50
Gate oxide thickness (nm)	15	1.4	1.5
V_t (V)	-0.5	~ -0.1	~ -0.2
I_{ON} (μA/ μm) ($V_{ds} = V_{gs} - V_t \approx -1V$)	2100	265	650
I_{OFF} (nA/ μm)	150	< 500	9
Subthreshold slope (mV/dec)	130	~ 100	70
Transconductance (μS/ μm)	2321	975	650

The same group at IBM compared some properties of the CNFET to both a high performance silicon MOSFET and a newer MOSFET design that utilize Silicon-On-Insulator (SOI) technology, the results are displayed in table 1. One important difference is in I_{OFF}. The CNFET has a drop of about 70% as compared to the conventional MOSFET. This means that the power being wasted while the transistor is off is greatly reduced. In addition, we notice that I_{ON}, or drive current, is larger than both technologies. In fact, it is three to four times larger. Normally we would think that this would be a bad thing since our first instinct would mean higher power consumption. However, since the nanotube has ballistic conductance, it actually has a smaller resistance. Thus, the power consumption is the same if not smaller than the current MOSFET design. This is also supported by the two to four times increase in transconductance.

The real big surprise is that the CNFET is able to outperform both the current and newer technologies, despite the large gate length and gate oxide thickness. So naturally, when the CNFET design is optimized, the CNFET will surely outperform both the current technology and the newer SOI technology. For these reasons, the CNFET is a very strong contender to replace the current technology.

1.4 Goal and structure of Paper

The goal of this paper is to provide a starting point for any one who wishes to start research on CNFETs. By reviewing everything that has been accomplished to date, new research can easily be started without having to spend so much time researching to catch up to the current work. This should help to accelerate the development of CNFETs. In addition, this paper will help people who are just curious about this new and exciting technology, thus helping to educate the public about CNFETs. This will also help informing investors, who will then help to increase funds towards CNFETs development.

The structure of this paper is as follows. First, a review of the physics of carbon nanotubes will be presented. After which, the two main types of carbon nanotube transistors, field effect and single electron transistors, will be analyzed, with emphasis on construction and operation. Next, we will look at the construction of circuits and chips

using carbon nanotube transistors. Finally, we will discuss the problems, which need to be solved to make the carbon nanotube transistors commercially viable.

Basic Physics of Carbon Nanotubes

Carbon nanotubes are hexagonal sheets of graphene, which are single layers of graphite atoms, in the form of rolled up chicken wire. As shown in figure 1.

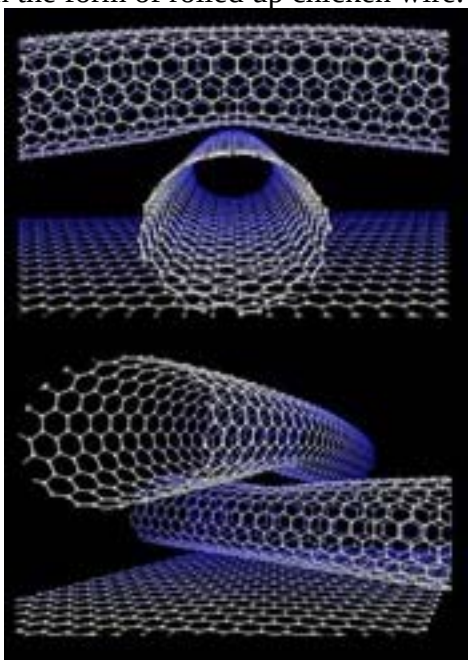

Figure 1[6] – Carbon Nanotubes are sheets of graphene that are rolled up into seamless cylinders.

Due to their hexagonal nature, they are part of a class of molecules called fullerenes, which are closed-caged molecules containing only hexagonal and pentagonal interatomic bonding networks[7].

There are two types of carbon nanotubes. One type is shown in figure 1 and is called Single-Wall-Nanotube, or SWNT. This type consists of only one cylinder, and represents the most promising type in the use of transistors. Their diameter is usually 0.33 to 5.0 nm and their lengths are 2 to 10nm. The other type is Multi-Walled-Nanotubes, or MWNTs. They are a bunch of SWNT in a Russian doll type of configuration, with SWNTs placed inside larger SWNTs. A MWNT's diameter ranges from 3 to 50 nm and their lengths are several microns.

1.5 Physical Properties

Carbon Nanotube's hexagonal structure gives it great strength. In fact, they are 50 times stronger than steel and yet are only a quarter as dense. In addition, carbon nanotubes have very good elastic properties. No matter how much they are squeezed, the nanotube will just bend or buckle, but not break. They will always pop

back into shape. Another amazing property is its heat transfer characteristics. Carbon Nanotubes are able to conduct heat so well that they are more efficient than diamond, which is one of the best heat conductors[2]. These three properties mean that anything made with carbon nanotubes, including transistors, will be extremely resilient and able to work even in the most inhospitable environments.

1.6 Electrical Properties

The electrical properties in carbon nanotubes (CNT) are unique and customizable. Unlike most materials, they come in both metallic and semiconducting forms. In addition, their band gaps can be set to desired level by adjusting some physical characteristics. Another unique property is that they are one-dimensional ballistic conductors even above room temperature.

1.6.1 Electrical Structure of Graphene

Since CNT are composed of graphene sheets, a detailed analysis of the electronic structure of graphene is required to understand the electrical properties of CNTs. The first Brillouin zone for graphene is shown in figure 2

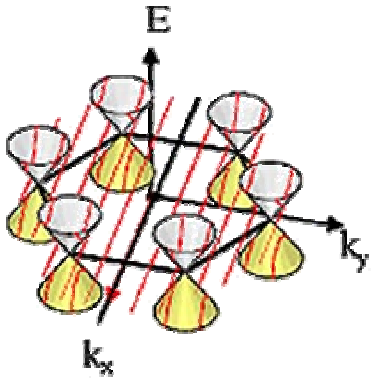

Figure 2[8] – First Brillouin Zone, a plot of energy of conductance vs. electron wavevector.

One of graphene's unique properties is that Fermi Energy is located only at the corners of the Brillouin zone, marked by the cones. This is how graphene is sometimes metallic and others times semiconducting. As a result, graphene is known as a zero-bandgap semiconductor[7].

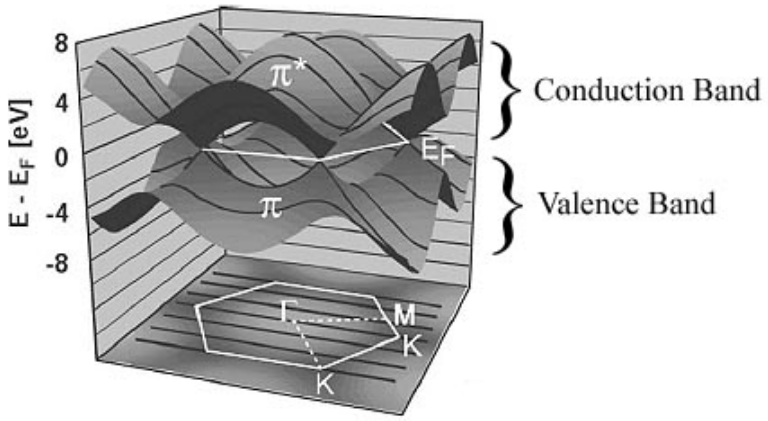

Figure 3[9] – 3D plot of graphene's band structure, along with the First Brillouin Zone.

Figure 3 shows a 3D plot of the band structure, along with the Brillouin zone under the plot. The 3D plot gives us a more real world picture. The Fermi points, the points where the conduction band and the valence band meet, are clearly visible. When mapped to the Brillouin zone, $\overrightarrow{\Gamma K}$ and the other five-wavevector direction (k), each being translated by 60°, are metallic since they correspond to Fermi point on the plot of the band structure. $\overrightarrow{\Gamma M}$ and the other wavevector directions are semiconductors, since they correspond to band gaps in the band structure.

1.6.2 Metallic or Semiconducting

When the graphene sheet is rolled up, the electrons become confined to the circumference of the nanotube. To account for this, a new quantization condition is applied, represented by:Equation Section 2

$$\overrightarrow{k_C} \cdot \vec{C} = 2\pi i \,. \tag{2.1}$$

Where $\overrightarrow{k_C}$ is the wavevector in the circumference direction, $\vec{C}$ is the chirality vector, and i is an integer[8].

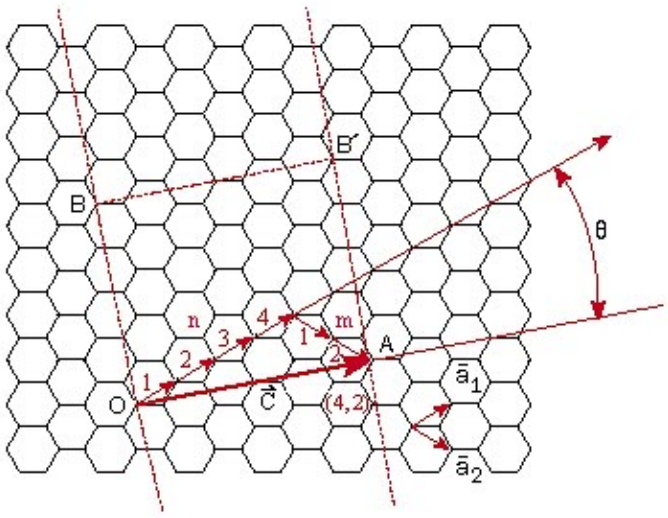

Figure 4[10] – Unrolled (4, 2) nanotube.

Chirality vector, or chiral vector, is defined as $\vec{C} = n\hat{a}_1 + m\hat{a}_2$, where $\hat{a}_1$, $\hat{a}_2$ are unit cell vectors and n, m are integers. Figure 4 shows an example. n and m are derived from a reference point, point O in figure 4, to another point, point A. These points are brought together when the graphene sheet is rolled up to create the nanotube. Carbon nanotubes are classified by their chirality vector and are represented by (n, m), thus in figure 4 case the nanotube is a (4, 2) nanotube. Another way to describe the chirality vector is to use the chirality angle, θ. The chirality angle is measured between direction of n and $\vec{C}$ as shown in figure 4. It is calculated using the formula,[11]

$$\theta = \sin^{-1} \frac{3m}{2\sqrt{n^2 + m^2 + nm}} \tag{2.2}$$

Going back to the new quantization condition, one consequence is the splitting of the band of the graphene sheet, into one-dimensional sub bands labeled by i. These sub bands now represent the allowed electron states in the nanotube. Figure 3 shows the sub bands, represented by the black lines, for a (3, 3) nanotube. If these sub bands cross through the K Fermi points then the nanotube is metallic. The reason being that the electron now has a path, through an allowed state and then through a Fermi point, and is able to enter the conduction band without any extra energy. This occurs for the (3, 3) nanotube in figure 3. However if the bands miss the K points, then the electrons will encounter a band gap and the nanotube will become a semiconductor[8].

A simple way to determine if a carbon nanotube is metallic or semiconducting is to look at the indices that describe it, (n, m). The nanotube will be metallic if $n = m$ or $n - m = 3i$, where i is an integer. Otherwise, the tube is semiconducting. The n and m indices can also be used to check which of the three categories a nanotube fits in, zigzag, armchair, or Chiral. Figure 5 shows examples of all three.

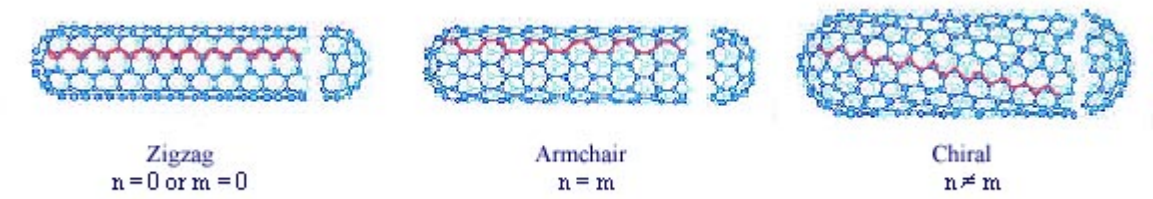

Figure 5[11] – Three types of Chirality.

The zigzag is characterized by its Zigzag shape, the armchair by its armchair shape, and the chiral by its twisted shape as highlighted. By combining figure 5 and the condition for type of conductor, armchair will always be metallic since $n = m$, while the others can be metallic or semiconductor. This is shown in figure 6.

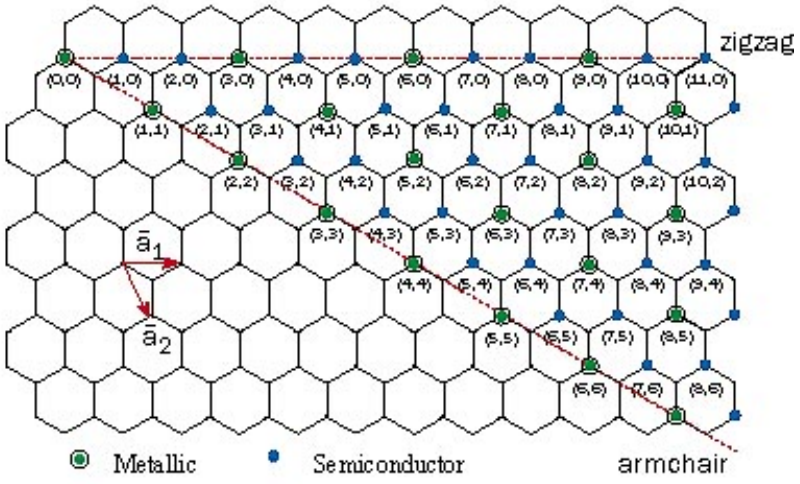

Figure 6[9] – Metallic or semiconducting depending on which point the (0, 0) point is rolled to.

If the (0, 0) point is folded to any of the points along the armchair line, we get a metallic nanotube. However if it is folded along the zigzag line or in the chair area, which is the area between the zigzag and armchair, we get either semiconductor or metallic tube, depending on the n, m rules.

1.6.3 Band Gap

The band gap is inversely proportional to the diameter of the carbon nanotube.

$$E_{Gap} = \frac{4\hbar v_F}{3d}. \tag{2.3}$$

Where v_F is the Fermi velocity and d is the diameter of the nanotube[8]. The diameter can be calculated using the equation:

$$d = \frac{\sqrt{3}a_0}{\pi}\sqrt{n^2 + m^2 + nm}, \tag{2.4}$$

Where $a_0 = 0.142nm$ is the interatomic distance between each carbon atom and its neighbor[12].

Even after the nanotube is created, its band gap can still be modified. A group in Cornell University proved that the band gap of CNT could be altered when the tube is placed under strain. To prove this they hung a NT across two gold electrodes and then using an AFM tip as and gate they pushed the tube, as in figure 7.

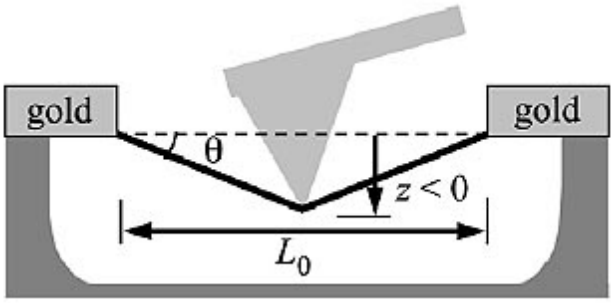

Figure 7 [12] – Experimental set up for band gap and strain relationship test.

The results agreed with the theory. The theory says that the new band gap will result from the equation,

$$E_{Gap} = E_{Gap_0} + \frac{dE_{Gap}}{d\sigma}\sigma, \tag{2.5}$$

where E_{Gap} is the energy of the band gap, E_{Gap_0} is the original band gap derived from the diameter of the tubes using equation 2.4, σ is the axial strain, $\frac{dE_{Gap}}{d\sigma}$ is the rate of change of the band gap with respect to strain, which equals

$$\frac{dE_{Gap}}{d\sigma} = \sin(2p+1)3t_0(1+\upsilon)\cos 3\theta. \tag{2.6}$$

t_0 is the tight-binding overlap integral and is equal to 2.7 eV, υ is the Poisson ratio equaling 0.2, θ is the chirality angle from equation 2.2, and $p = 0, \pm 1$ such that

$$n - m = 3i + p. \tag{2.7}$$

Where n and m are the same indices used to characterize the nanotube and i is an integer.[13]

Another way to alter the band gap is to apply a magnetic field along the nanotubes central axis. The band gap will oscillate with an increasing magnetic field, such that a nanotube will change back and forth from metallic and to semiconducting. The period of the oscillating conducting property is dependent on the field strength.[10]

1.6.4 Ballistic Transport

Ballistic transport occurs when the mean free path is larger than the length the carrier travels. The mean free path is the average length that a carrier has to travel before it encounters a scattering event. The carrier can be scattered by many different sources, such as both acoustic and optical phonons that are vibrations in the lattice, ionized impurities, defect, interfaces, and even other carriers.

It has be discovered that at low voltage and assuming perfect contact, metallic nanotube have been found to have a mean free path of at least 1μm at room temperature. In addition, the mean free path is inversely proportional to the temperature, so the lower temperature nanotubes have longer paths. Comparing this to metals, such as

copper whose mean free path are approximately 10's of nanometers. This is because of a reduction in the cross section of a scattering event due to the 1D nature of the nanotube. At room temperature, acoustic phonons do not posses enough momentum to change the carrier's direction. So unlike metals, where a carrier can use multiple small angle scattering events to reverse its direction, the 1D nanotube forces carriers to move only back and forth eliminating the possibility of small angle scattering events reversing the electrons direction. While optical phonons do have enough momentum to reverse the direction of carriers, they are too energetic to exist at room temperature and at low voltages. In addition, static defects, such as impurities, defects, interfaces, etc., can be eliminated with careful manufacturing of the carbon nanotubes.[7]

Due to the ballistic conductance and the strong covalent bonds between the carbon atoms, the nanotube is able to achieve current densities of $2.5\times10^{9}\,\frac{Amps}{cm^{2}}$. This is significantly higher than any type of interconnect used in today's circuits.

1.6.5 Multi-Walled-Nanotubes

Due to MWNT's construction using SWNTs, there properties are complicated, since each SWNT shell can have different indices and bandgaps. However, it has been discovered that when connected to contacts, the outer shell contributes to most of the electrical transport. Therefore, a simplification can be done on MWNTs for transistors, since the transistor will require the MWNT to be draped over two contacts. It should be noted that there is still some coupling between shells and ultimately these effects will have to be understood. One way to understand them is to use a procedure developed by IBM to remove parts or whole shell and study the transport of each shell.

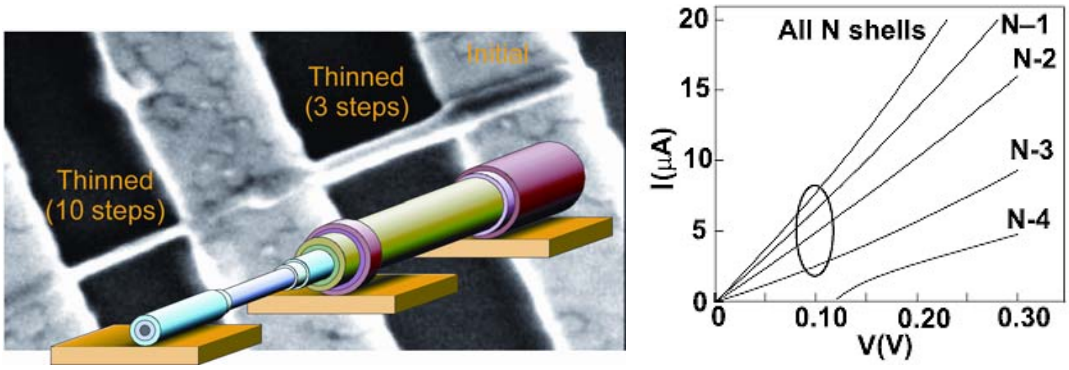

Figure 8[8,14] - Thinned MWNT, layers removed, along with an I-V plot after removal of each shell

Figure 8 shows the result after controlled breakdown and the result of the experiment. Based on the graph, the first three shells are coupled, since the curves all meet back at zero voltage along with all N shell line. The fourth shell is not coupled since it requires an activation energy of a little more than 0.1 volts.[8] More research is need to understand the effects from the coupling shells.

1.6.6 Summary

Table 2 – Equations used to describe Carbon Nanotubes and their electrical properties

Summary of equations	
Chiral Vector	$C = n\hat{a}_1 + m\hat{a}_2$
Chrial Angle	$\theta = \sin^{-1}\frac{3m}{2\sqrt{n^2+m^2+nm}}$
Diameter	$d = \frac{\sqrt{3}a_0}{\pi}\sqrt{n^2+m^2+nm}$
Metallic	$n-m=3i$
Semiconducting	$n-m\neq 3i$
Band Gap	$E_{Gap} = \frac{4\hbar v_F}{3d}$
Band Gap with Strain	$E_{Gap} = E_{Gap_0} + \frac{dE_{Gap}}{d\sigma}\sigma$
Rate of change of the band gap with respect to strain	$\frac{dE_{Gap}}{d\sigma} = \sin(2p+1)3t_0(1+\upsilon)\cos 3\theta$

Nanotubes can come in both metallic and semiconducting forms, depending on their indices, and their band gaps can be customized based on there diameters. In addition, even after construction their band gap can still be altered, giving the possibility of chips that can sense their environment. Moreover, their high current density and ballistic transport will enable them to create computer chips that use less power and operate much faster then any chip today.

1.7 Fabrication

There are three ways to create carbon nanotubes: arc discharge, laser ablation, and chemical vapor deposition (CVD). Each method has its advantages and disadvantages.

1.7.1 Arc Discharge

Arc discharge is the earliest method used to create nanotubes. It involves vaporizing carbon to create the nanotube. Figure 9 shows a schematic inside the chamber where the tubes are made.

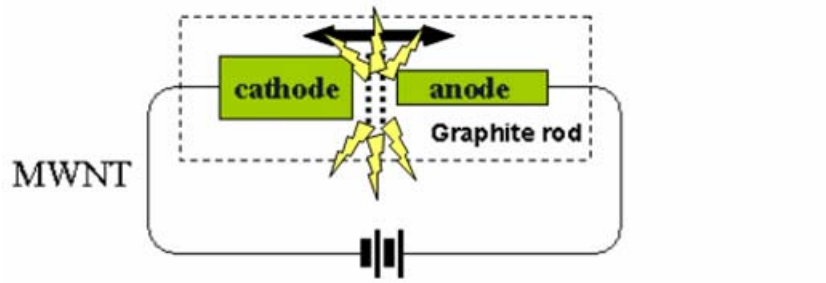

Figure 9[15] – Schematic of MWNT production using Arc Discharge

The apparatus is kept in a helium atmosphere at 50-760 torr. A bias voltage of about 10-30V is applied. The anode, which is composed of amorphous carbon, is brought to the cathode and then removed. The result is a discharge of about 50-300 amps. The discharge vaporizes part of the anode and the helium quenches the vapor to form the nanotubes. After which they collect at the end of the anode. The growth rate directly proportional to the helium pressure.[10]

This method will create MWNTs, but in order to create SWNTs a catalyst is required. The most common is Ni:Yi, other catalysts are Fe, Co, and Ni. The biggest requirement for the catalyst is that they be poor carbide formers. The Ni:Yi catalyst is mixed with the carbon to a 1.5% solution. Figure 10 shows the apparatus setup to create SWNTs.

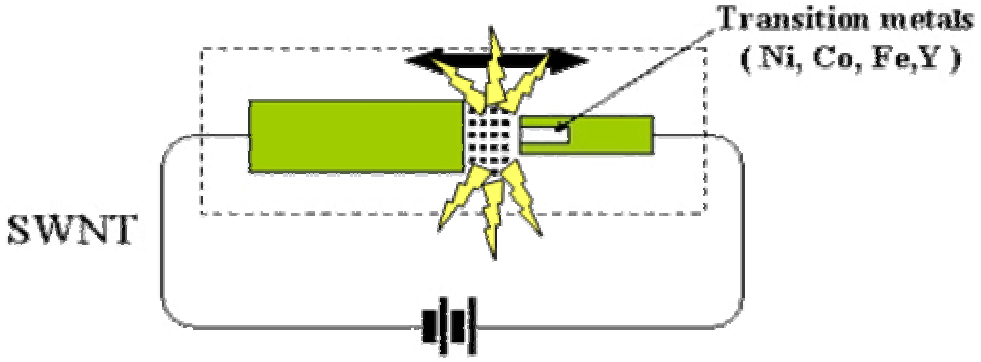

Figure 10[14] - Schematic of MWNT production using Arc Discharge

When the discharge occurs, both the catalyst and the carbon vaporize. The nanotube growth process is depicted in figure 11.

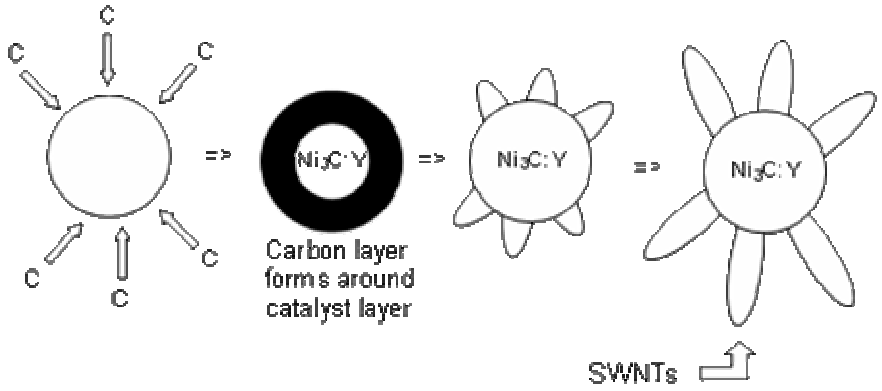

Figure 11 - Vapor-Liquid-Solid growth (VLS growth) mechanism of nanotubes

The carbon vapor is absorbed into the catalyst, which is in a liquid alloy with the carbon. A layer of carbon forms around the catalyst particles. Eventually a saturation point is reached and carbon is precipitated out in the form of SWNTs. During the entire time, carbon is continually being absorbed, allowing the nanotubes to grow. This process is called vapor-liquid-solid growth (VLS growth).

While this method is the cheapest, however it results in contaminated nanotubes that require cleaning. The soot that is produced with the nanotubes needs to be removed and it can easily get in air if not careful. After the tubes are cleaned, they are still jumbled together. Figure 12 shows SEM images of both MWNTs and SWNTs created with arc discharged.

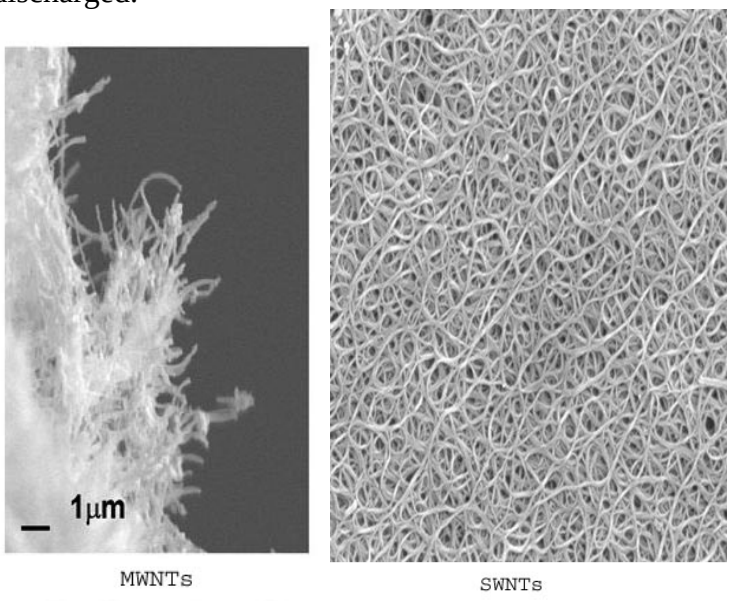

Figure 12 – SEM images of purified MWNTs and SWNTs produced through Arc Discharge

1.7.2 Laser Ablation

The laser ablation apparatus is shown in figure 13.

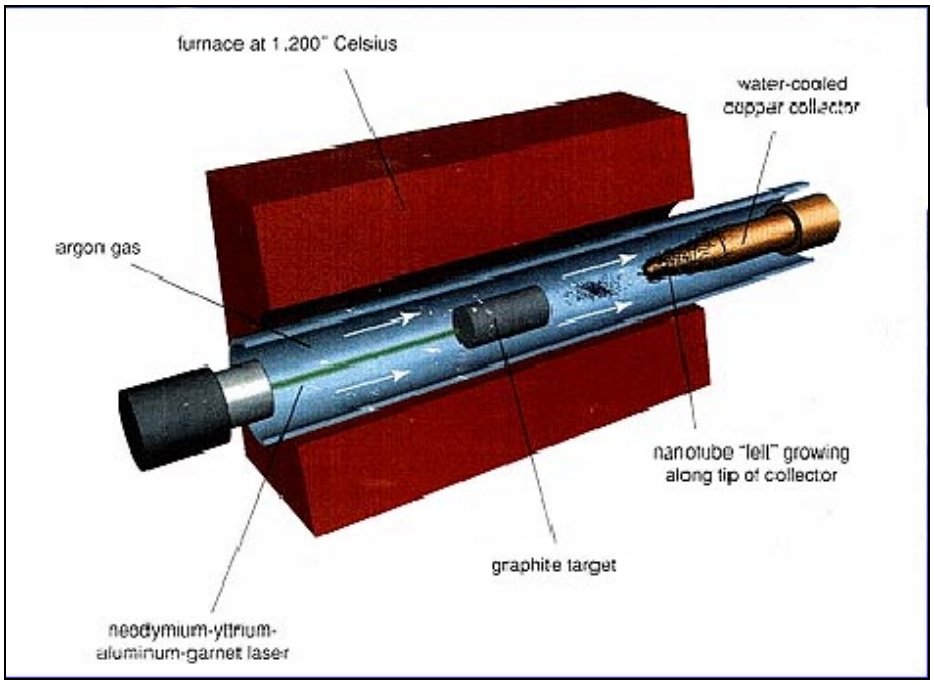

Figure 13[16] – Schematic of Laser Ablation apparatus. Laser vaporizes target and the nanotubes grow via VLS growth. They are then swept and collected on the cold finger.

A 10Hz pulsed laser is focused onto a graphite catalyst target in a quarts tube, which is located in tube furnace. The laser vaporizes part of the target and produces nanotubes using VLS growth. In order for VLS growth to occur, the oven temperature must be chosen such that the catalyst carbon mixture will be in a liquid alloy state and the pure carbon can remain solid, to precipitate out. To choose the correct temperature, a phase diagram is used. An example of the phase diagram used is in figure 14.

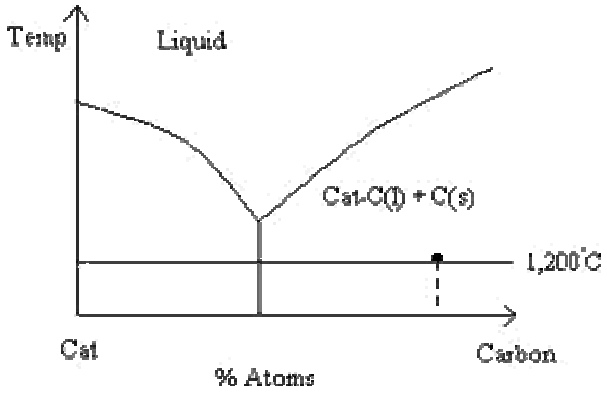

Figure 14 – Phase diagram, temperature chosen so the catalyst and carbon mixture is liquid and the pure carbon is solid.

The nanotubes are then swept by the flowing inert gas, argon in figure's 13, and collected on a cold finger.

Laser ablation will only grow SWNTs and not MWNTs. The SWNT produced are high purity nanotube. Minimal cleaning is required, but they still end up tangled up, making them difficult to use. In addition, Laser ablation is the most expansive, due to the laser required, costing $2,000 per gram with catalyst.

1.7.3 Chemical Vapor Deposition

Chemical vapor deposition (CVD) is the easiest method, involving the layering a catalyst and then having a hydrocarbon gas react with it to grow nanotubes.

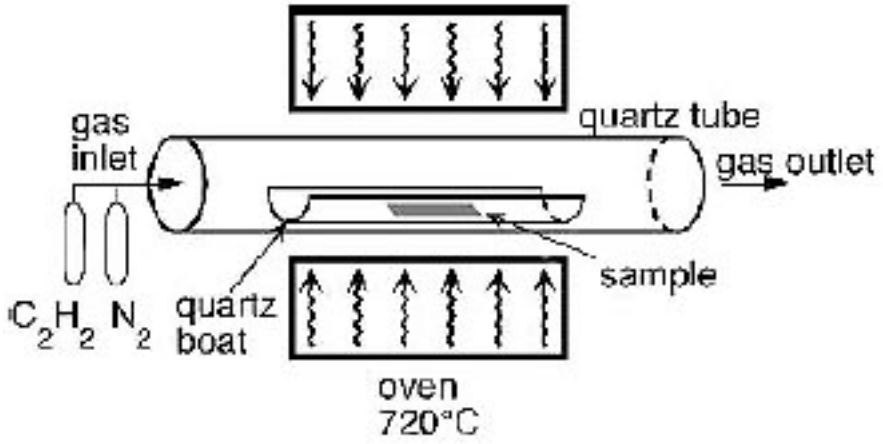

Figure 15[10] - Schematic of Laser Ablation apparatus

Figure 15 shows the apparatus used. The sample, which is a substrate layered with a catalyst particles, is placed in the center, and heated to around 720 degrees Celsius. The hydrocarbon gas is then flowed through the tube. The gas catalytically reacts and grows the nanotubes. The growth process is shown in figure 16.

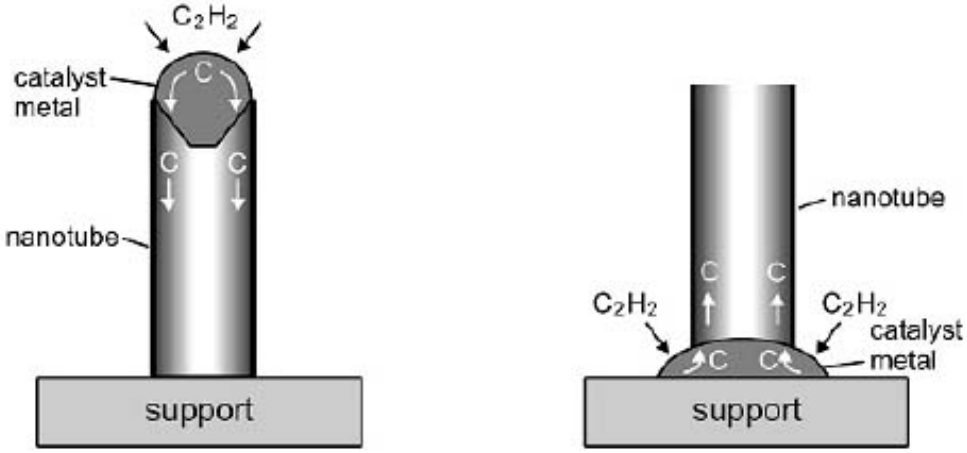

Figure 16[43] – Growth process during CVD production

The nanotube can grow two ways. Both ways are the same except for whether the tube grows underneath the catalyst or above it. The process is similar but slower to VLS

growth. The carbon form the gas is absorbed into the catalyst and the nanotubes are then precipitated out.

CVD produces the cleanest nanotubes, thus no leaning is required. Since the tubes are grow where the catalyst particle are, the nanotubes are not tangled up and are easier to use. In addition, the process is very familiar to the current IC fabrication techniques, so it would be easiest to scale up to industrial production.

1.7.4 Summary

Each method has its advantages and disadvantages. Each method is compared in table 3.

Table 3[17] – Comparison of methods for carbon nanotube production

Fabrication	Typical Yield	Advantages	Disadvantages
Arc Discharge	up to 30% by weight	Cheap, Fast, Both SWNT and MWNT	Very dirty, length less then 50 microns, tangled
Laser Ablation	up to 70 %	Fast, high purity, very long nanotubes	still needs cleaning, expansive, tangled
CVD	20 - 100 %	no cleaning, direct on substrate, easiest to scale up	slightly expansive

CVD seams to be the best option for creating nanotubes to be used in transistors, since they are grown in place, only slightly expansive, and it is similar to lithography techniques used in IC manufacturing.

Carbon Nanotube Field-Effect Transistor

Carbon nanotube field-effect transistors (CNFET) are similar to the MOSFETs of today. They require three terminals, source, drain, and gate. The gate is used to control the current across the source and drain terminal. When the gate is on current is able to flow across the source and drain through a channel. The main difference between CNFETs and MOSFETs is that CNFETS use their carbon nanotubes as the channel, where MOSFET's channel is made form heavily doped silicon. Both technologies use complimentary devices, the p-type and n-type. This helps to reduce power consumption, higher gain, stable, and implanted easily in logic circuits. The p-type transistor conducts holes, where as the n-type conducts electrons. Both types along with another type of device will be analyzed, concentrating on their construction and switching.

1.8 Blueprint of Current CNFET Designs

1.8.1 Evolution

The first CNFETs where designed in the easiest way, since only a proof of concept and a basic understand were the goals of these devices. Figure 17 shows the first generation CNFETs.

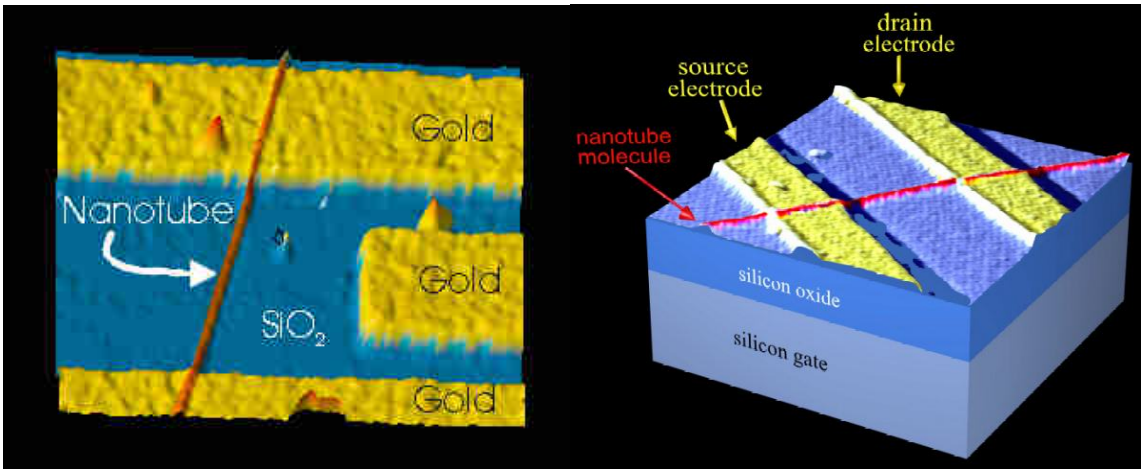

Figure 17[18],[19] - First generation Carbon Nanotube Field-Effect Transistors (CNFET).

The nanotube is draped over two gold electrodes, representing the source and drain. The gate is located either on the side or underneath the transistor. In addition, the gate is separated by an insulator, such as silicon dioxide, to isolate the gate form the nanotube. By having it isolated, the electric field from the gate is able to switch the transistor on and off. If it were not shielded a short would occur, and the transistor would not be able to operate.

They are problems with these designs. The first is that the nanotube is left open to the air, which as we will see causes the transistor to operate as a p-type, or p-FET, only. In addition, the gate placement causes problems. Whither the gate is next to the nanotube or underneath, the gate oxide is required to be thick, at least ~100 nm, which causes the need for high voltages to penetrate the oxide and switch the transistor. Have the gate underneath cause an additional problem in that all transistors are switched at the same time since all the transistors share the same gate. Making it imposable to create large circuit or chips.

1.8.2 Best Current Design

The 2nd generation transistors boast big improvement over the first design. The new design is shown in figure 18.

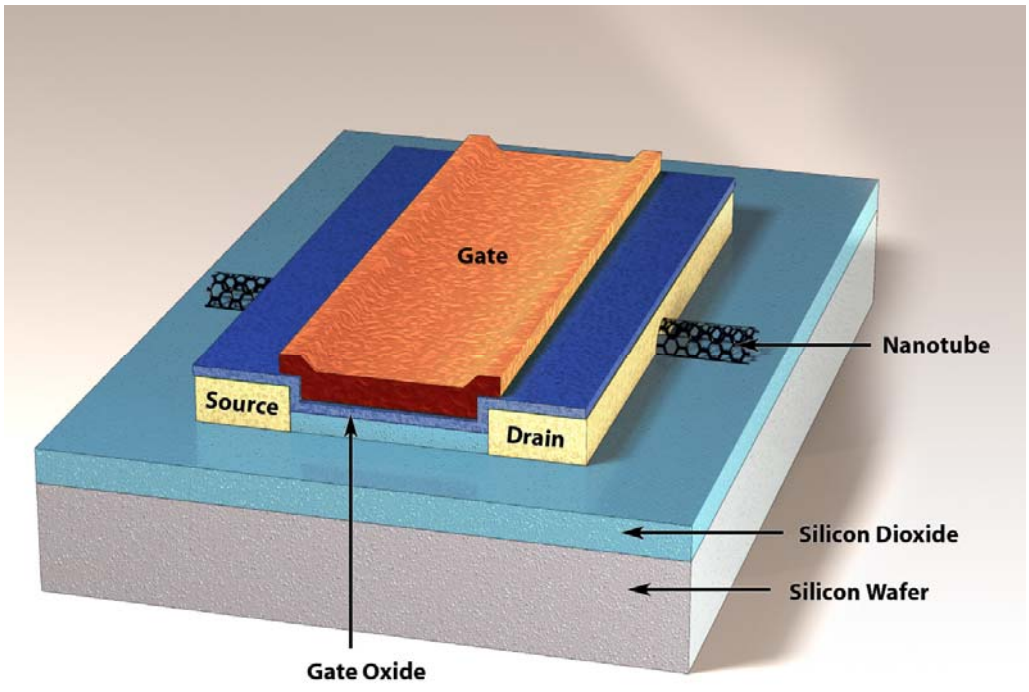

Figure 18[20] – Second Generation CNFET

The main difference between the first generation and the second is the placement of the gate electrode. The gate is now placed on top of the nanotube. This design change seals the nanotube, so the air will not force the transistor to act as a p-type transistor. The other benefit is that the gate oxide is much thinner, about 15 nm, allowing much smaller voltages to be used. Figure 19 shows a plot of the drain current vs. the drain to source voltage.

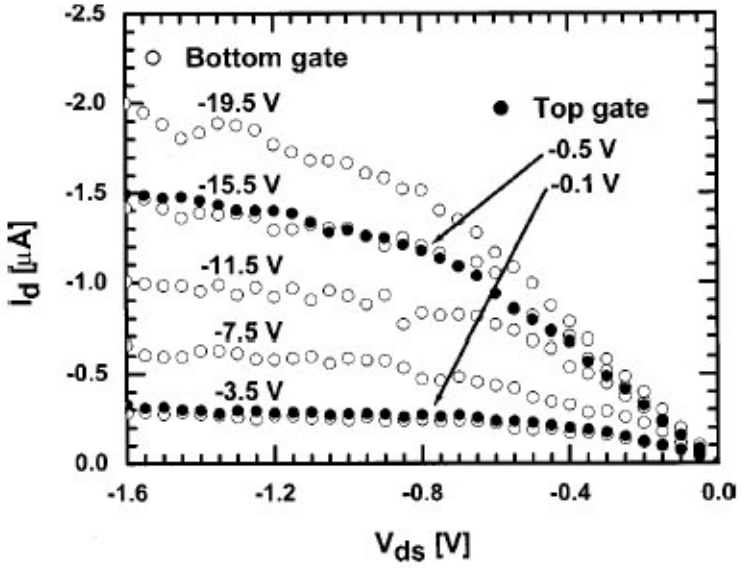

Figure 19[4] – Drain-source I-V curves for both first and second generation CNFETs.

The graph compares the first generation, Bottom gate, to the second generation, Top gate. As expected the top gate design uses significantly smaller gate voltages. The transistors can also be independently operated in the same fashion that MOSFETs are. This is because the MOSFET design is very similar. An example of one is shown in figure 20.

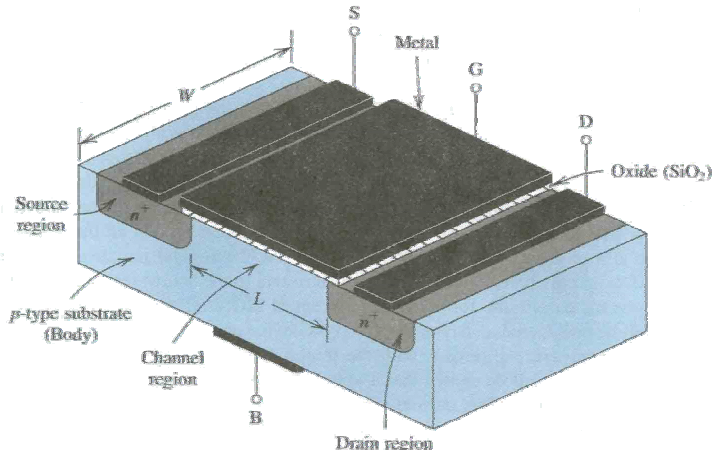

Figure 20[21] – Schematic of a MOSFET device.

Both designs use a top-gated design. In fact, the only difference is with the channel. An addition advantage with the second-generation CNFET is that with some slight modifications, the new design can be well suited for high-frequency operations. This is not possible with the first generation because of the large overlap capacitance from all three electrodes[4].

Another way to create the 2nd generation design is to use an electrolyte to make the gate. A schematic is shown in figure 21.

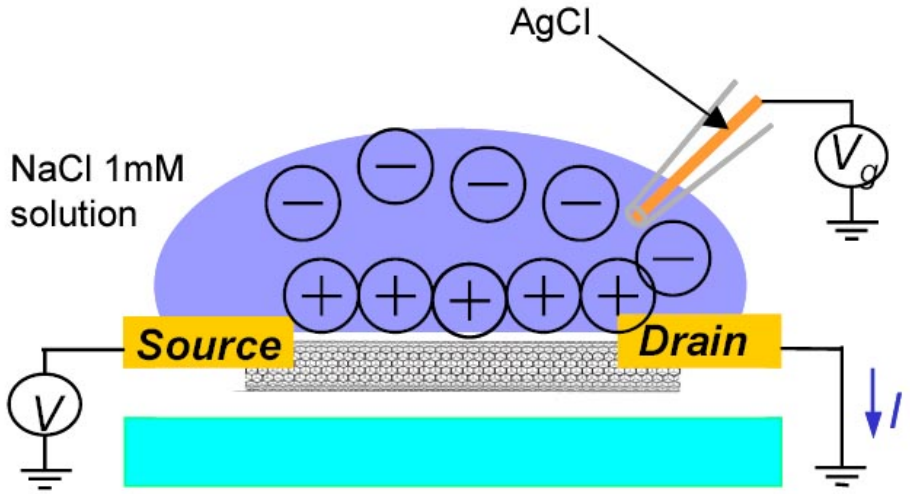

Figure 21[7] – Schematic of a CNFET that uses an electrolyte solution for the gate.

By having an electrolyte solution as the gate, the capacitance between the nanotube and gate is increased as compared to the 1st generation CNFETs. The higher capacitance improves performance. Figure 22 shows the I-V curves for the electrolyte gated CNFET.

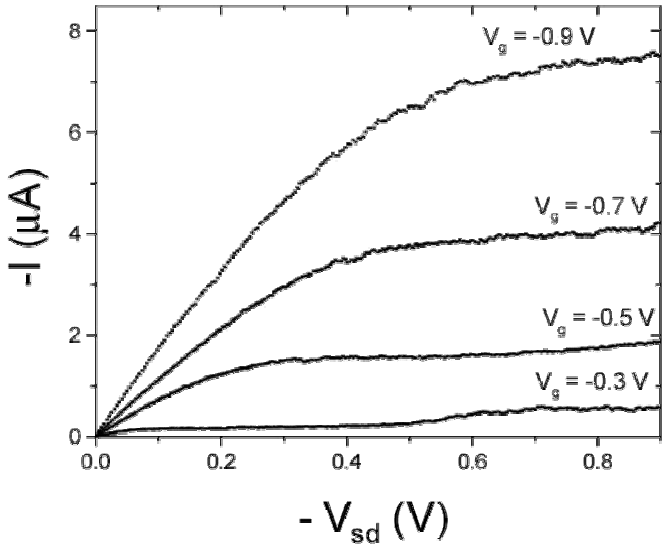

Figure 22[7] – I-V curves for the electrolyte gated CNFET

The curves are very similar to the MOSFET's curves and to the metal top-gate design. One key difference is that the saturation point is reached earlier than both the metal top-gate design and the MOSFET. This means that this design potential might consume less power than both the other transistor types. However, the fact that it uses a liquid electrolyte is a draw back. The electrolyte must be sealed to prevent leakage and to keep the air from diffusing through and converting an n-type into a p-type, which adds extra steps in manufacturing.

1.9 P-Type

P-type transistors conduct holes when a negative voltage is applied to the gate. They do not conduct electron even at high positive gate voltages.

1.9.1 Construction

The following procedure is used to create p-type CNFETs:[4]

1. Single Crystal Si substrates are cleaned and coated with 120 nm of SiO_2.
2. SWNT are produced by either laser ablation or CVD (if CVD => skip to step 5)
3. Clean nanotube
4. Untangle by using sonication
5. Nanotubes are diluted with 1, 2-dichloroethane solution. Density of solution is adjusted to yield approximately one nanotube per a give area.
6. Solution is spun onto the substrate.
7. Confirm placement of nanotubes, using an AFM, SEM, or etc.
8. Create metal source and drain electrode by using e-beam lithography and liftoff

9. Anneal samples, depending on your metal, at 850°C for 100s. This forms metal carbide at the carbon nanotube and metal junctions, which reduces contact resistance.
10. Deposit a mixture of SiH_4 and O_2 at 300°C to create gate oxide.
11. Open source and drain contact holes in the new oxide layer.
12. Anneal at 600°C in N_2 for 30 minutes to densify the oxide.
13. Pattern gate electrode using e-beam lithography and liftoff with ~50 nm of gate metal
14. Perform a forming gas annealing step to reduce trapped charges in oxide interface

The result is a p-type CNFET. There is no need to dope or alter the nanotube to create the p-type transistor. The nanotubes naturally become p-types when they are exposed to air. This is because the oxygen in the air causes the Fermi-level at the contacts to shift closer to the valence band. The result is that the holes see a small barrier, thus they are able to tunnel through, where as the electrons see a much lager barrier, and are not able to tunnel. Figure 23 shows the altered Fermi-level at the contact.

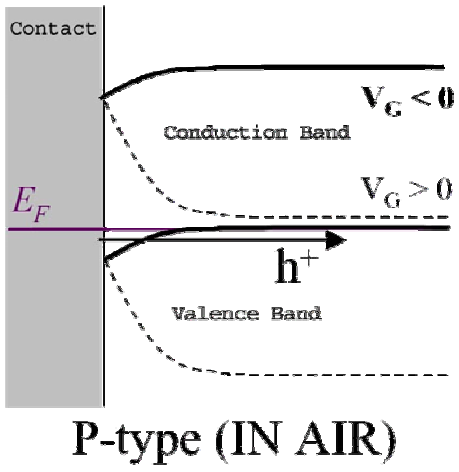

Figure 23[3] – Band structure at nanotube-contact interface for p-type transistor. The Fermi level is closest to the valence band, hence the conduction of holes.

1.9.2 Transfer Characteristics

To study the switching characteristics figure 24 shows a graph of current vs. voltage along with the transfer characteristics, this plots the drain current vs. the gate voltage.

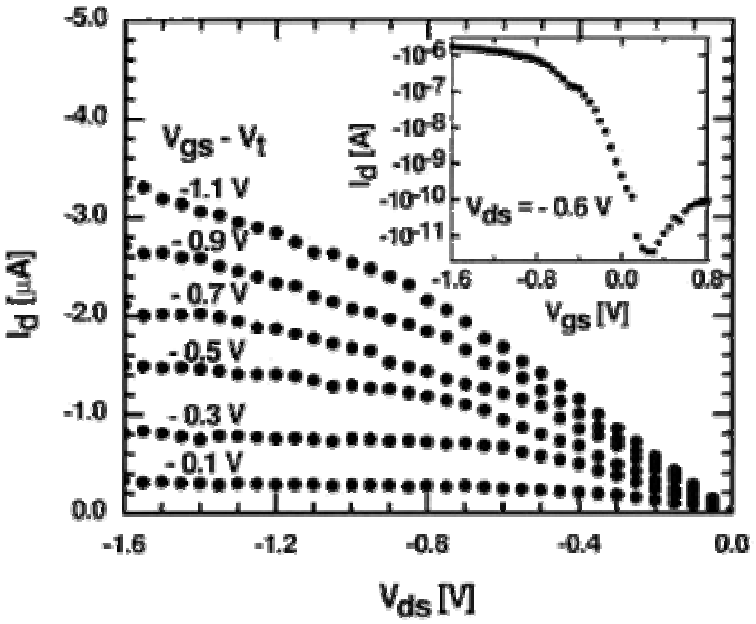

Figure 24[4] – I-V curve along with an inset of the transfer characteristic for the p-type transistor

Based on the transfer characteristic we can see that there is a little bit of conduction when the gate is positive, however this is too small to accidentally turn on another transistor. It will only add a minute amount of power wastage. When the gate voltage is negative, the transistor turns on and delivers a 5-fold increase in drain current. This is good because it means that the transistor will easily be able to drive another one.

1.10 N-type

1.10.1 Construction

The n-type CNFET is made in a very similar way as the p-type. With the exception that the nanotube needs to be converted to an n-type and then sealed to prevent the air from converting it back to a p-type. Fortunately, the nanotube will be seal up anyway in the 2nd generation design with its gate on top. There are two ways to convert to an n-type. One is through annealing and the other is to dope the nanotube.

1.10.1.1 Annealing

The point of annealing is to drive out the oxygen that was absorbed while the nanotube was exposed to air. To do this a new step is introduced before step 8. The new procedure is as follows:[4]

1. Single Crystal Si substrates are cleaned and coated with 120 nm of SiO_2.
2. SWNT are produced by either laser ablation or CVD (if CVD => skip to step 5)
3. Clean nanotube
4. Untangle by using sonication

5. Nanotubes are diluted with 1, 2-dichloroethane solution. Density of solution is adjusted to yield approximately one nanotube per a give area.
6. Solution is spun onto the substrate.
7. Confirm placement of nanotubes, using an AFM, SEM, or etc.
8. Create metal source and drain electrode by using e-beam lithography and liftoff
9. Anneal samples, depending on your metal, at 850°C for 100s. This forms metal carbide at the carbon nanotube and metal junctions, which reduces contact resistance.
10. ***Anneal at 450℃ in N_2 to remove absorbed oxygen***
11. Deposit a mixture of SiH_4 and O_2 at 300°C to create gate oxide.
12. Open source and drain contact holes in the new oxide layer.
13. Anneal at 600°C in N_2 for 30 minutes to densify the oxide.
14. Pattern gate electrode using e-beam lithography and liftoff with ~50 nm of gate metal
15. Perform a forming gas annealing step to reduce trapped charges in oxide interface

By removing the oxygen, the Fermi-level is sifted up towards the conduction band and the barrier for the electrons is reduced, allowing them to tunnel through. At the same time, the barrier for the holes is increasing, so that they can no longer tunnel through. Figure 25 shows the new band structure at the contacts.

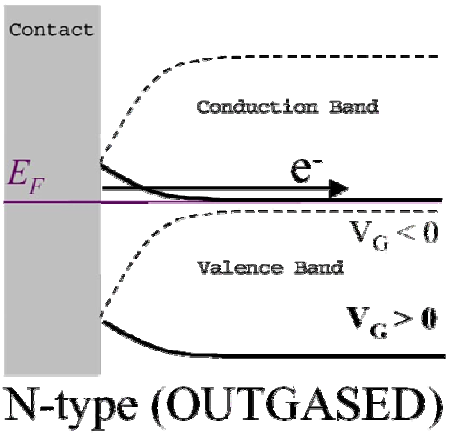

Figure 25[3] – Band structure at nanotube-contact interface for n-type transistor created with annealing. The Fermi level is closest to the conduction band, hence the conduction of electrons.

1.10.1.2 Doping

Doping occurs with an electron donor, such as potassium. The procedure is similar to annealing, accept instead of annealing we dope. The new procedure is as follows:

1. Single Crystal Si substrates are cleaned and coated with 120 nm of SiO_2.
2. SWNT are produced by either laser ablation or CVD (if CVD => skip to step 5)
3. Clean nanotube
4. Untangle by using sonication
5. Nanotubes are diluted with 1, 2-dichloroethane solution. Density of solution is adjusted to yield approximately one nanotube per a give area.
6. Solution is spun onto the substrate.
7. Confirm placement of nanotubes, using an AFM, SEM, or etc.
8. Create metal source and drain electrode by using e-beam lithography and liftoff
9. Anneal samples, depending on your metal, at 850°C for 100s. This forms metal carbide at the carbon nanotube and metal junctions, which reduces contact resistance.

10. Dope nanotube with a electron donor, such as potassium

11. Deposit a mixture of SiH_4 and O_2 at 300°C to create gate oxide.
12. Open source and drain contact holes in the new oxide layer.
13. Anneal at 600°C in N_2 for 30 minutes to densify the oxide.
14. Pattern gate electrode using e-beam lithography and liftoff with ~50 nm of gate metal
15. Perform a forming gas annealing step to reduce trapped charges in oxide interface

The transformation from doping is similar to annealing, except that doping cause the threshold voltage to shift downwards. It is important to note that the Fermi-level is pined down by the doping and does not move. Figure 26 shows the bands during doping.

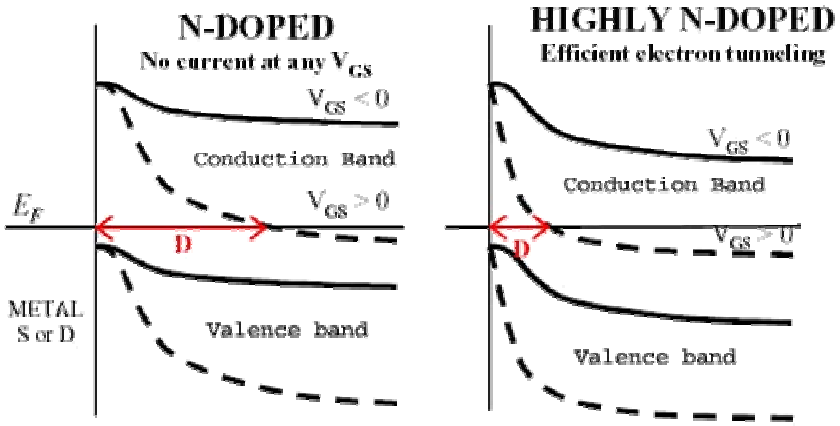

Figure 26[3] – Band structure at nanotube-contact interface for n-type transistor created with doping. Fermi level does not move, instead the barriers thickness, D, is reduced.

The transistors does not become n-type until the nanotube is heavily doped. This is because the bands need to bend enough so that the barrier for the electrons shrinks enough to allow tunneling to occur.

1.10.2 Transfer Characteristics

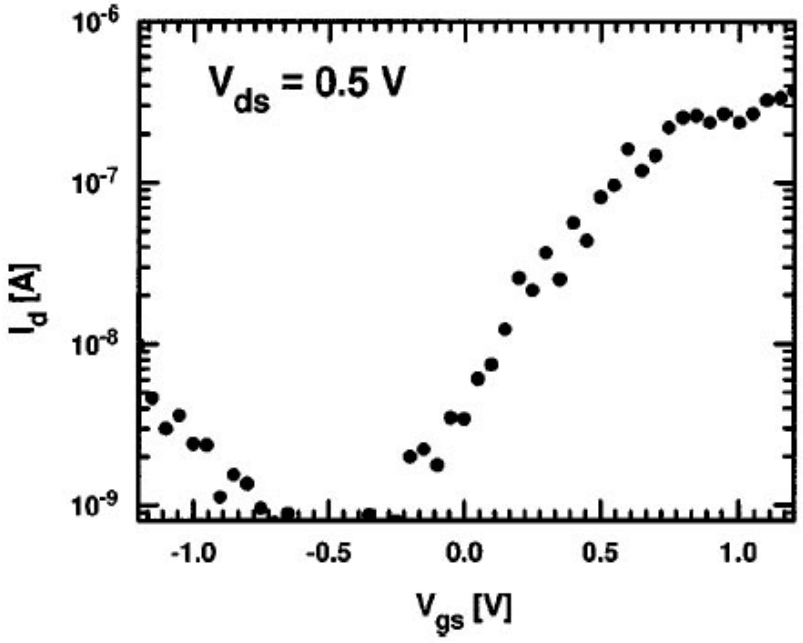

Figure 27[4] – Transfer characteristic of n-type CNFET

Figure 27 is the transfer characteristic of the n-type CNFET. It is the opposite of the p-type's characteristics. The small off current occurs when the gate voltage is negative, instead of positive. In addition, the 5-fold increase occurs when the gate voltage is positive, instead of negative.

1.11 Ambipolar Device

An ambipolar device is unique in that it conducts both holes and electrons. This allows them to be customized on the fly. By applying a bias voltage, they can imitate both p-type and n-type transistors. This makes them useful in circuit that need to adapt, such as neural networks that learn and adapt to a set of inputs.

1.11.1 Construction

The ambipolar device occurs during the annealing process to make n-type transistors. Before the transistor becomes an n-type, it goes through a phase that makes it an ambipolar device. Therefore, to make them, the procedure is the same as for n-types, except that the time the transistor is annealed in step 8 is reduced. The resulting bands at the contacts is shown in figure 28

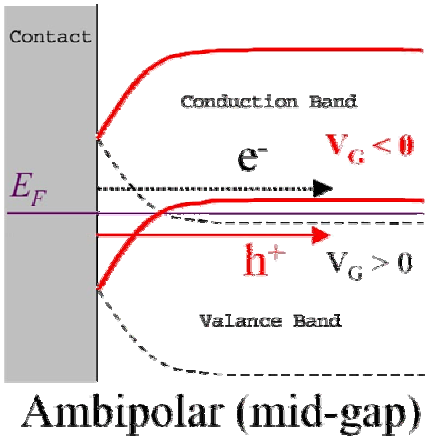

Figure 28[7] – Band structure at nanotube-contact interface for an ambipolar CNFET. Fermi level is close to both conduction band and valence band. Therefore, the ambipolar device is capable of conducting both electron and holes.

By only removing some of the absorbed oxygen, the Fermi level moves up in-between both the conduction band and the valance band. The result is small barriers, of about 15 meV[7], for both electrons and holes. However, the barriers are still thicker than either the p-type or the n-type. With the thinner barriers, the electrons and holes are able to tunnels through and conduct in the nanotube.

1.11.2 Transfer Characteristics

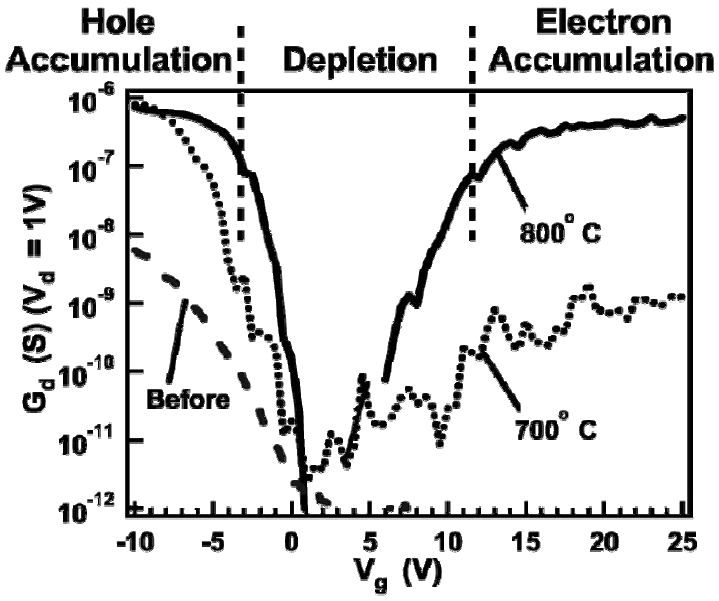

Figure 29[7] – Graph of drain conductance vs. gate voltage for before conversion to ambipolar, which was a p-type transistor, and after conversion. The dashed line represents the p-type.

Figure 29 shows the conductance across the drain vs. the gate voltage. The before line represent the transistor before annealing, when it was a p-type transistor. The

other two lines shows two different ambipolar device created at 700 and 800°C. The 800°C annealed transistor appears to be the best, due to its higher and similar conduction for both holes and electron. The ambipolar transistor shows conduction of both holes and electrons, based on the polarity of the gate voltage. The other important factor is the 5 to 6 fold increase in conduction when the transistor is on. Figure 30 depicts the barriers by plotting the I-V curves at different temperatures.

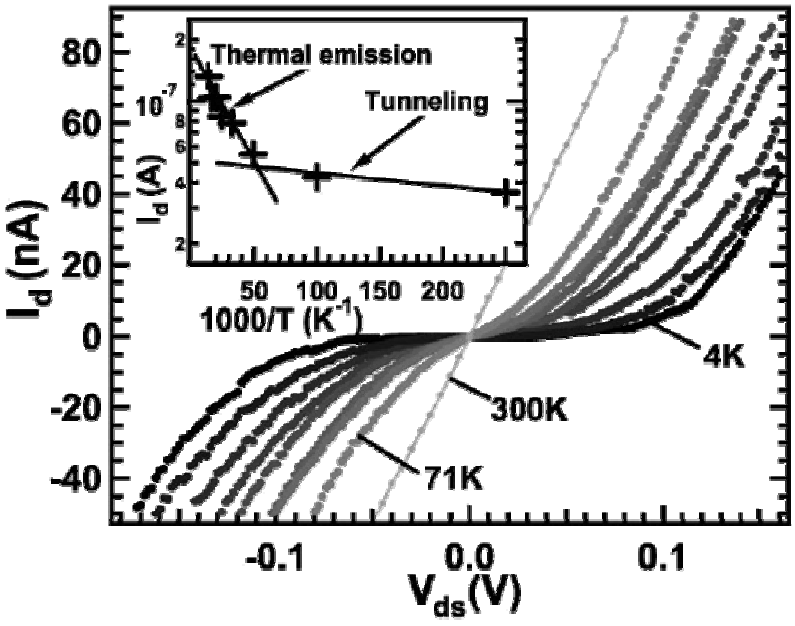

Figure 30[7] – I-V curves for varying temperatures of an ambipolar CNFET. Insert represents conduction through barrier at varying temperature.

The barriers are thick enough to prevent tunneling at lower temperatures. The carriers require assistance from the voltage across the source and drain, to tunnel through and conduct. Once the temperature reaches room temperature, very little voltage is need because the thermal energy is enough to assist the carrier to tunnel through the contact barriers. However, the exec current produced is so small, in nano-Amps, that the contribution to power wastage is small. In addition, the power wastage will only occur during switching of the transistor, thus it will exist during an operation and not continuously.

1.12 Physics of Operation

1.12.1 Switching at Contacts

Conventional MOSFET use the electric field from the gate to modulate the channel. The electric field form the gate will either attract electron or drive them away, depending ton the type transistor. For n-types, the gathering of electrons forms a path allowing other electrons to travel across from the source to the drain, creating the drain-source current. The opposite is true for the p-type.

Surprisingly this is not the case for CNFETs. A group at IBM discovered that most CNFETs actually switch like Schottky barrier MOSFETs (SB-FET). Instead of the gate's electric field modulating the channel, the electric field instead controls the width of the barriers at the contacts. Figure 31 shows the gate's voltage effect on the barriers at the contacts.

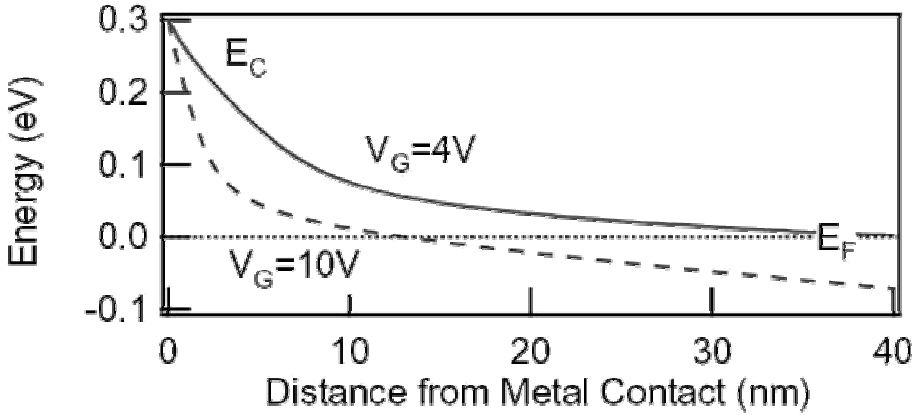

Figure 31[22] – Nanotube-contact conduction band energy. The higher gate voltage causes the conduction band to bend and reduce the barriers thickness.

The increased voltage causes the bands to bend, reducing in energy. This works for all types of CNFETs, so long that the barrier is initially high enough. If the barrier is to low, the CNFET switches like a conventional MOSFET.[21, 7]

1.12.2 Comparison to MOSFET and Conclusion

Table 4[3, 7] – Comparison of the different CNFET geometries along with the conventional MOSFET

	P-type FETs			
	Back-gated CNFET	Metal Top Gate	Electrolye Tope Gate	Si MOSFET
Gate Length (nm)	1030	260	----	100
Gate Oxide Thickness (nm)	150	15	----	0.8
Transconductance (S/m)	244	2100	10000	460
Subthreshold Slope (mV/dec)	730	130	----	80
ON/OFF ratio	10^5	10^6	10^6	10^6

---- Means no data available

Table 4 compares key characteristics to the three main types of CNFET and the current Si MOSFET. The back-gated CNFET is clearly the worst. Si MOSFET has the smallest gate length and oxide thickness. This due to the constant evolution that the Si MOSFET has gone through, the CNFETs will soon catch up with more research. The electrolyte gate CNFET is the best when it comes to transconductance, with the metal top gate in second. Both CNFETs are beating the Si MOSFET already. Moreover, they tie the MOSFET in on off ration. Given these two factors despite the thicker gate oxide, means that the CNFETs have the potential to easily outperform Si MOSFET technology in the near future.

Carbon Nanotube Single-Electron Transistor

1.13 What are Single-Electron Transistors

Single-electron transistors (SETs) are transistors whose drain to source current is composed of only one electron. With only one electron traveling, the power consumption is greatly reduced. For this reason, a lot of research has been done on SETs. However, it has been discovered that SETs will have a very tough time replacing MOSFETs because of there low gain, high impedance, and their sensitivity to background noise. Due to these problems, SETs will most likely not replace MOSFETs. Instead a hybrid system will develop, combining the best of both types of transistors. The SETs contribution is high charge sensitivity, while the MOSFETs are providing the gain and low impendence need for real life application. Another important application for SETs is charge-sensing applications such as the readouts for both electron memories and charge-coupled devices in metrology and astronomy where precision charge measurements are required.[23]

1.14 The Basic Physics of Single-Electron Transistors

SET's operation is somewhat analogous to the operation of a MOSFET. The difference being that SETs operate completely on a quantum mechanical effect, tunneling. Figure 32 shows a basic diagram of single-electron transistors.

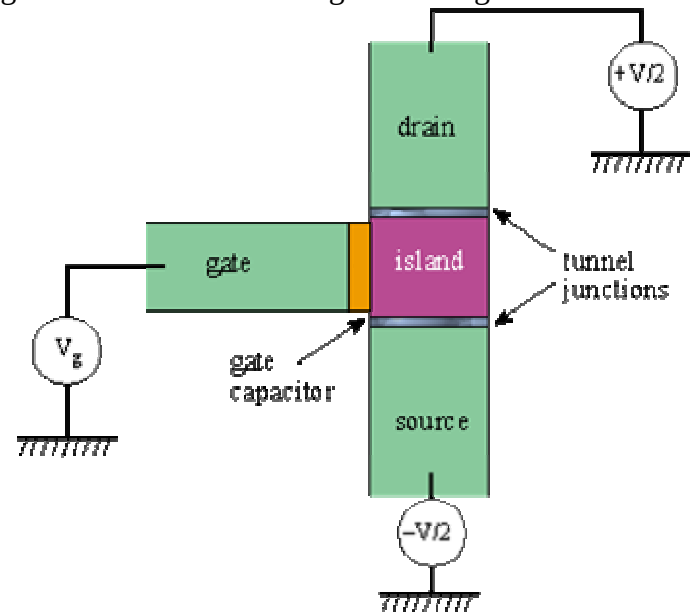

Figure 32[24] – Basic geometry of a Single-Electron Transistor (SET).

The geometry is similar to a MOSFET device, in that both have three terminals. The difference is that SETs include a conduction island, that is isolated from the drain and source by tunneling junctions. However, in real life, a second gate is used to tune the background charge in order to optimize operation[22]. Figure 33 is a scanning electron microscope (SEM) image of a SET.

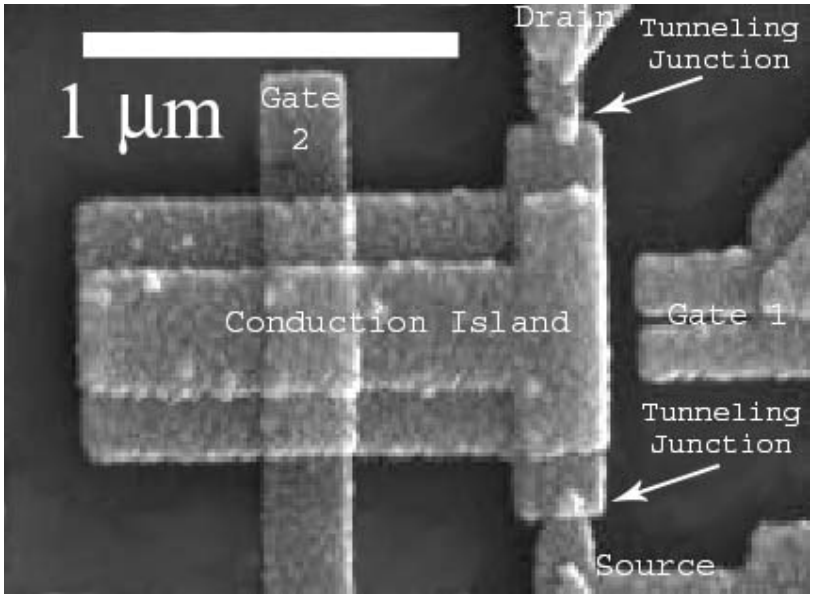

Figure 33[25] – SEM image of a SET.

The first gate is of a standard planar design that is used for the input of the transistor. The second gate is a parallel plate type of gate, used to tune the background charge. The arrows point to the small points where the source and drain make contact. These contact points are the tunneling junctions that isolate the conduction island. An equivalent circuit is in figure 34.

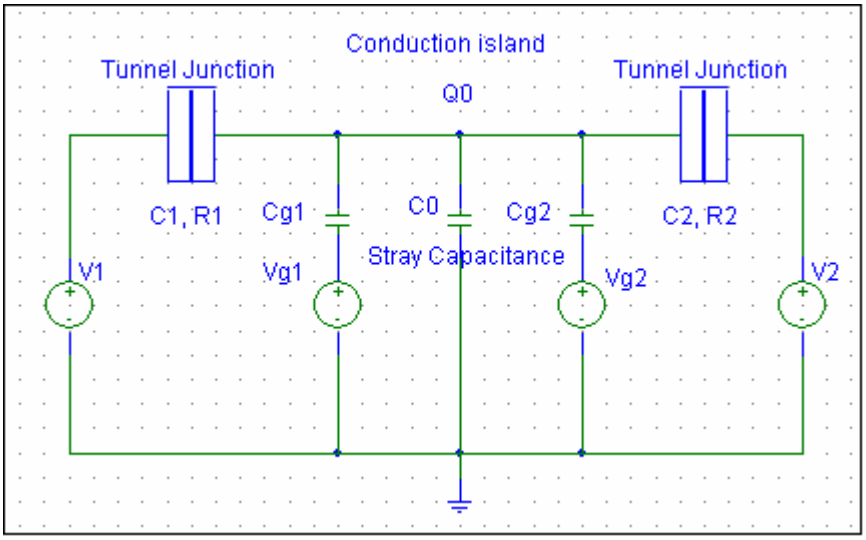

Figure 34[22] – Equivalent circuit of a SET

The capacitor between the island and ground, known as the stray capacitance (C_0), and a background charge of Q_0 on the island are included to help model the real world SET. From the schematic, we can calculate the voltage of the island as a function of the number of electrons on the island:Equation Section 4

$$V(n) = \frac{\left(Q_0 + C_1V_1 + C_2V_2 + C_{g_1}V_{g_1} + C_{g_2}V_{g_2} - ne\right)}{C_\Sigma} \tag{4.1}$$

Where n is the number of electrons in the island, e is the fundamental charge, and $C_\Sigma = C_0 + C_1 + C_2 + C_{g_1} + C_{g_2}$ is the total capacitance. To calculate the energy needed to transfer an electron from ground to the island, integrate equation 4.1 from ground to –e:

$$\int_0^{-e} V(n)dq = -eV(n) + \frac{e^2}{2C_\Sigma} \tag{4.2}$$

Where n is the number of electrons on the island before the additional one. The term $\frac{e^2}{2C_\Sigma}$ is known as the coulomb energy, E_c. The coulomb energy is the energy need to add an electron to the island when $V(n) = 0$. Therefore, the thermal energy must be smaller than the coulomb energy, or else the electrons will be able to tunnel through the barriers themselves without any gate control. Tunneling can occur at both junctions in either direction. This leads to four tunneling conditions:

$$\begin{aligned}
\Delta E_{1_R} &= eV_1 - eV(n) + E_c \\
\Delta E_{1_L} &= -eV_1 + eV(n) + E_c \\
\Delta E_{2_R} &= -eV_2 + eV(n) + E_c \\
\Delta E_{2_L} &= eV_2 - eV(n) + E_c
\end{aligned} \tag{4.3}$$

ΔE_{1_R} represents the energy associated with an electron tunneling towards the right, from the V_1 to island, through tunnel junction 1. ΔE_{1_L} is the energy of an electron tunneling towards the left through junction 1, and so on. If any of the equations become negative, then an electron will tunnel through the corresponding barrier and direction. However if all four are positive, then no electron can tunnel, giving rise to the condition known as Coulomb blockade, which is the off state for the SET. Based on equations 4.3, the critical voltage across the drain and source is $V_{ds} = \frac{e}{C_\Sigma}$. If below $\frac{e}{C_\Sigma}$ then the Coulomb blockade is maintained and in order to switch the transistor on, the gate must receive half and electron. If above $\frac{e}{C_\Sigma}$ then the Coulomb blockade is broken and the transistor is permanently on, allowing electrons to tunnel through both barriers, regardless of the gate.

While keeping $V_{ds} \le \frac{e}{C_\Sigma}$, if the gate voltage is increased all the way to a full electron, the transistor again enters Coulomb blockade and stops the addition of

additional electron on the island. This leads to a step like curve in the graph of the number of electrons on the island vs. the gate voltage as shown in figure 35.

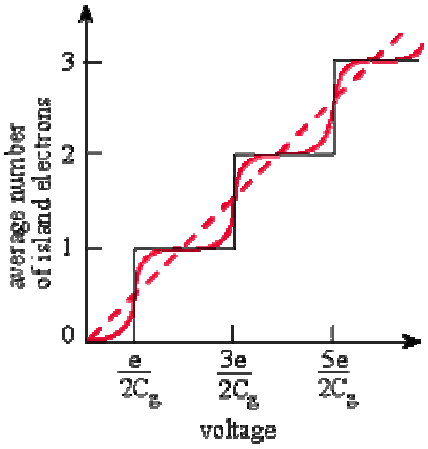

Figure 35[23] – Graph of voltage vs. number of electrons. The steps are sharper for more resistive barriers at lower temperatures.

When the gate voltage is raised to half an electron, or $\frac{e}{2C_g}$, an electron is added to the island. The next half an electron will block the addition of electron until the next half electron is applied to the gate. So the raising of a whole electron charge on the gate will only allow the addition of one extra electron. This give rise to a periodic nature in the conduction of electrons and hence also in the conductance, $\left(\frac{dI}{dV_g}\right)$. Figure 36 plots the conductance versus the drain to source voltage and the gate voltage.

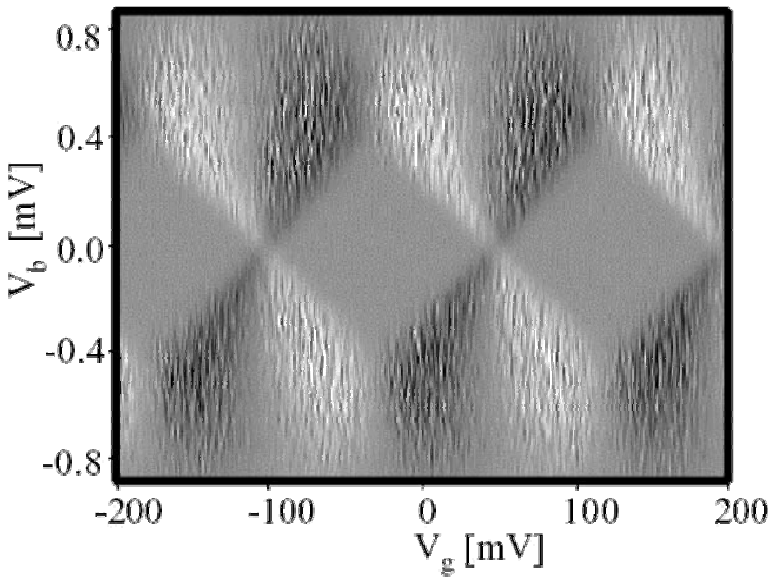

Figure 36[24] – Conduction vs. Drain-Source voltage, or bias voltage, V_b. The diamonds are regions of coulomb blockade and therefore no conduction. Black areas are negative conduction, while the white is positive conduction

The diamond region represents Coulomb blockade regions, and the black is negative conductance and white is positive conductance. Figure 35 and 36 are the tell tail signs of a single-electron transistor, and therefore are used to identify them.

1.15 Single-electron Transistors from Carbon Nanotubes

There are two main ways to create SETs from CNTs (CNSET). The first is to lay a carbon nanotube across two metallic contacts and chill the transistor to low temperatures. The second is to make two buckles, or kinks, in a metallic nanotube.

In the first kind, the nanotube becomes the conduction island. The high resistance at the nanotube contact interface is the barriers that isolate the nanotube. The contacts are of any type of metal, however usually platinum. The substrate used to support the devices acts as the gate. Since the coulomb energy associated with this device is smaller than the thermal fluctuations, low temperature operation is required. Figure 37 shows both an AFM picture of a nanotube draped over platinum electrodes to form a SET, along with a plot of the current vs. bias voltage. In the graph, the staircase is viable, identifying that the transistor is indeed a SET.

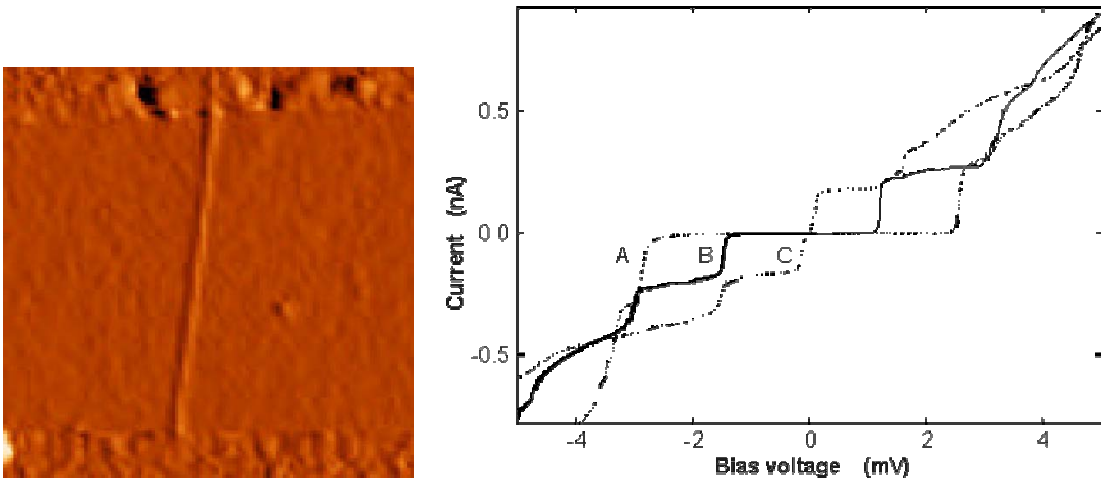

Figure 37 [24, 26] – (Right) AFM image of a SET constructed as a nanotube draped over platinum electrodes. (Left) Plot of I-V curve, the staircase proves SET operation.

There is another way of creating the first type of CNSET. Instead of having the substrate as the gate, another nanotube could be draped over the original one to form the CNSET. Figure 38 shows an AFM image of the CNSET and a graph of the current as a function of both the drain-source and gate voltage.

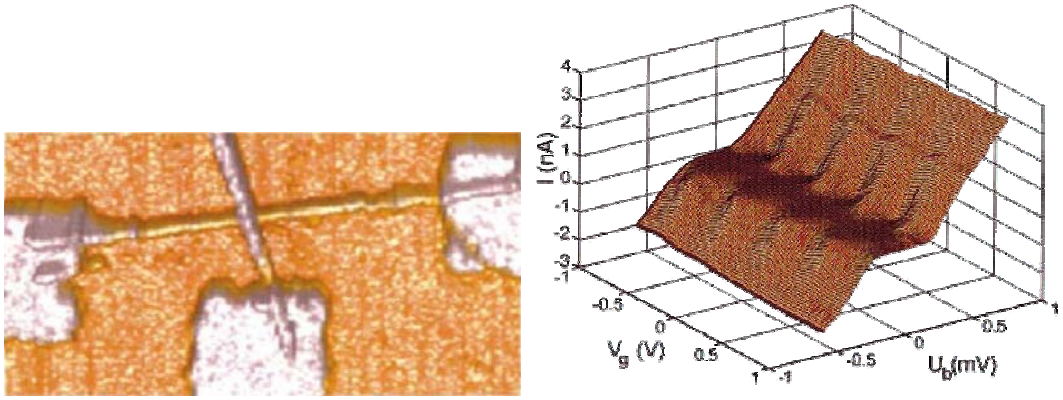

Figure 38[27] – (Right) AFM image of a SET constructed with two nanotubes. Top nanotube is the gate and has only one contact. Bottom Nanotube is the conduction island. (Left) Plot of current vs. both the gate voltage and the bias voltage. Flat dark region are the coulomb blockade

In the AFM image, the contacts are all Au. The bottom nanotube is the island, while the top acts as the gate. The top nanotube is only connected to one contact because we want only the voltage to be transmitted and not any current. The graph shows Coulomb blockade at the dark regions in the middle, where no current flows. This confirms that the transistor is a SET.

The second type, which is created by buckling a nanotube in two places, is able to operate at room temperature, since the coulomb energy is large enough room temperature operation. Figure 39 shows how to construct them.

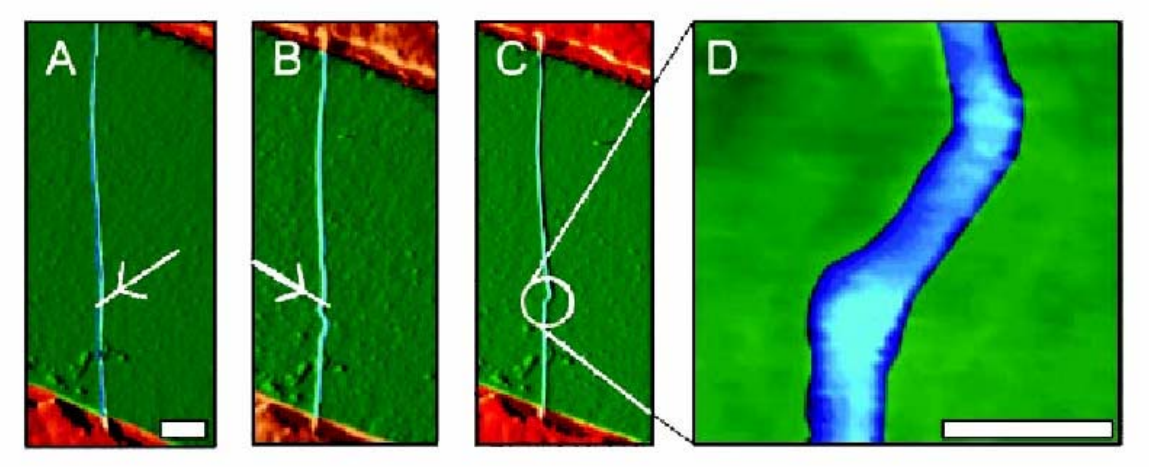

Figure 39[28] – Production of a SET through buckling of a nanotube

The following procedure is used to create them:

1. Drape nanotube across two metallic contacts on a substrate with an oxide layer
2. Image with AFM to make sure placement is good
3. Drop AFM tip all the way down
4. Move in the direction of the arrow in figure 39 A
5. Move a little along tube and repeat steps 3 and 4 in opposite direction of as in figure 39 B

The result is shown in part C and D in figure 39. The contacts are the source and drain, the substrate acts as the gate, and the island is the small length in between the kinks as shown in part D. The graph of the conductance is shown in figure 40.

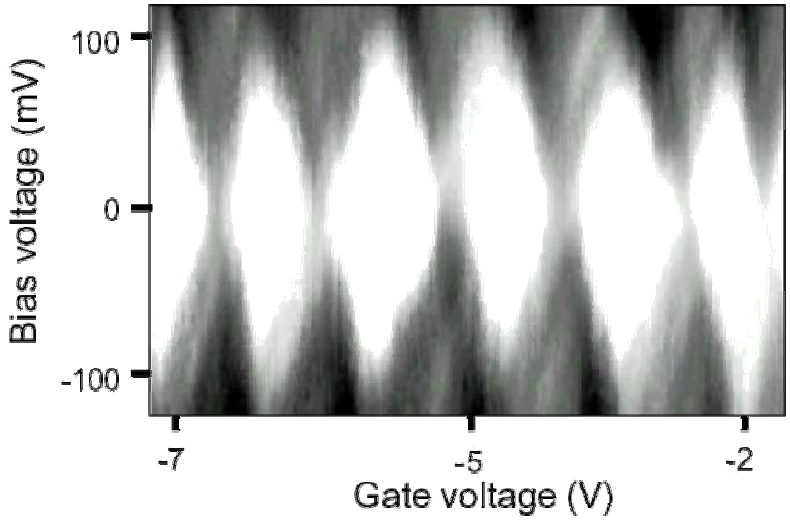

Figure 40 [24] – Graph of conductance as bias voltage vs. gate voltage. White diamonds are coulomb blockade.

The white regions represent the Coulomb blockade, because of zero conduction. In addition, the characteristic periodic oscillation of conduction and zero conductance is visible, proving that the transistor is a SET.

Circuits and Chip Design

Now with the ability to create complimentary CNFETs, the next step is to try to build logic elements, such as inverters, NOR, and NAND gates. In addition, memory devices, such as SRAMs would be useful to create. And eventually possible even fabricating chips with CNFETs. Not a lot of focus will be given to CNSETs since they will have a very hard time to replace MOSFETs in digital applications.

1.16 Inverter

1.16.1 Inter-Nanotube Inverter

1.16.1.1 Ambipolar Inverter

The inverter (NOT Gate) is the first logic element to be created using CNFETs, due to its simplicity. The inverter can be constructed by using just ambipolar CNFETs or using both the n and p type CNFETs. An ambipolar inverter's schematic is shown in figure 41.

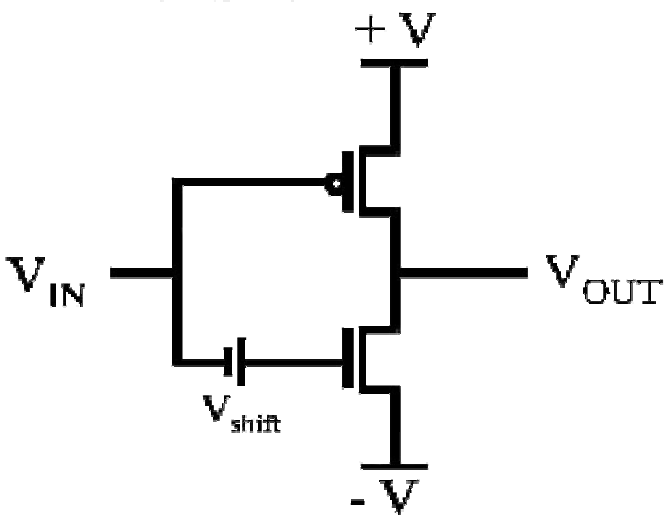

Figure 41 [3] – Schematic of an ambipolar inverter. V_{shift} is included to adjust threshold.

The addition of V_{shift} allows customization of the threshold for the p- and n-CNFET characteristics. The customization is required in order to optimize the inverters gate inversion function, its ability to invert the input signal. Figure 42 is a plot of the input vs. output voltages.

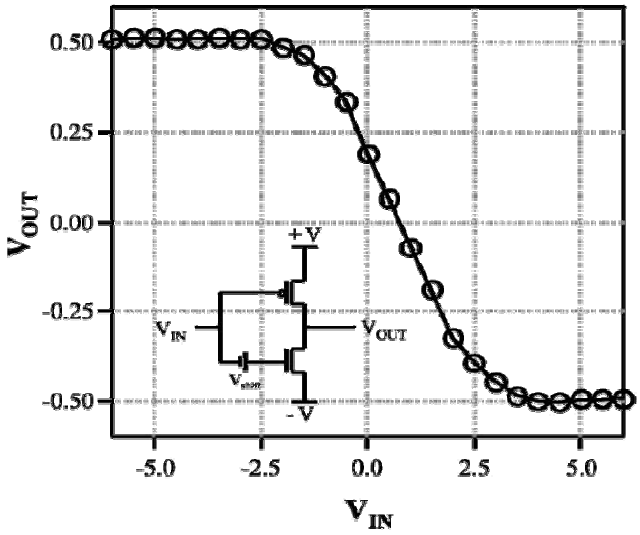

Figure 42[3] – DC characteristics (or transfer curve) of the ambipolar CNFET inverter.

The slope of the curve is sharp and steep, indicating that the gate's response is quick. In addition, the operating voltage is below 5V, which is the current operating voltage of today's MOSFETs. This means that the ambipolar CNFET gate will consume less power than its MOSFET counterpart.

1.16.1.2 N- and P-type Inverter

1.16.1.2.1 Schematic

Instead of using ambipolar CNFETs, the inverter can be constructed using a more traditional design, using complimentary n- and p-type CNFETs. Its schematic is in figure 43. It is same as the ambipolar schematic, with the exception of no V_{shift}.

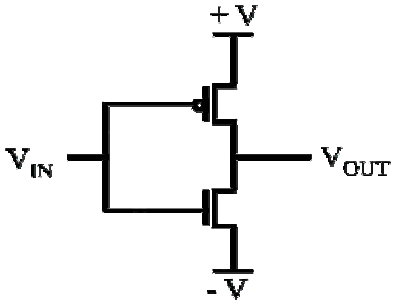

Figure 43 – Schematic of an inverter, using complementary transistors.

1.16.1.2.2 Construction

The procedure to build the inverter is as follows:

1. Create 2 CNFETs on same substrate
2. Convert one CNFET into an n-type (by annealing or doping)

a. Annealing
    i. Choose one to be n-type and seal it with PMMA resist
    ii. Vacuum Anneal both at 200°C for 10 hours
    iii. Expose to oxygen at 10^{-3} Torr for 3 minutes

   Sealed CNFET stays n-type, Unprotected converts back to p-type

b. Doping
    i. Seal both with PMMA resist
    ii. Choose one to be n-type and cut a window above with e-beam lithography
    iii. Dope with an electron donor, such as potassium
    iv. Adjust doping to overlap thresholds of n- and p-type

   Sealed CNFET remains p-type, Unprotected converts to n-type

3. Connect contacts as shown in schematic
4. Seal entire device with 10nm of SiO_2 for operation in air.

The result is shown in figure 44, where annealing is used.

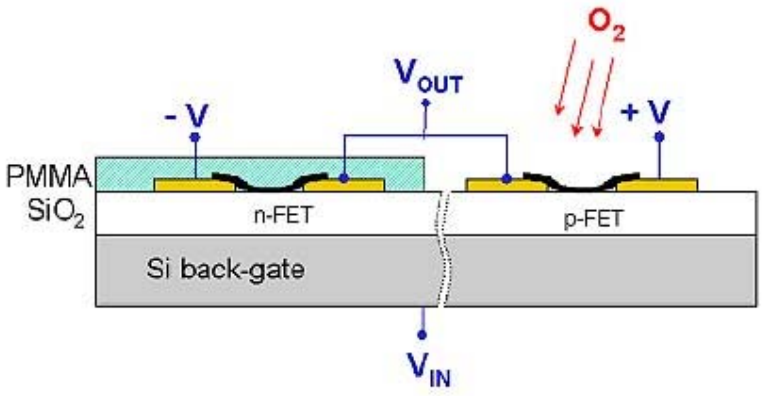

Figure 44[29] – Inverter created using annealing to create n-FET (n-type) and uses exposure to oxygen to convert to p-FET (p-type).

1.16.1.2.3 Characteristic

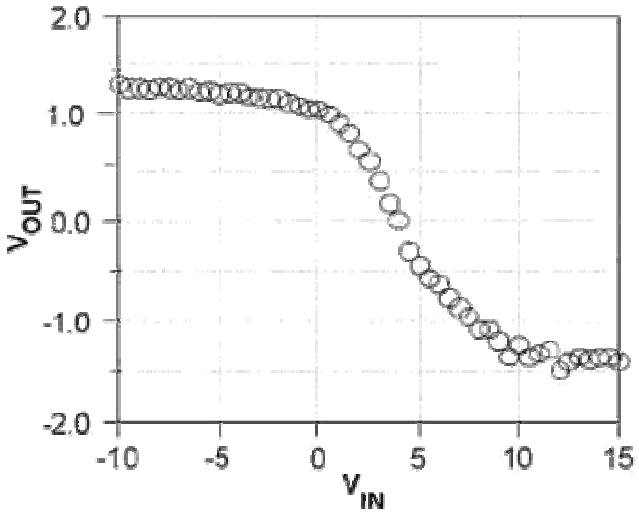

Figure 45[28] – Transfer curve of complementary CNFET inverter

Figure 45 plots the transfer curve for the inverter. The curve is not as well defined as the ambipolar device's curve. Therefore, it is slower and has a smaller gain. In addition, it requires higher input voltages, thus consuming more power than the ambipolar device. This could be due to the slight differences between the two nanotubes that were used, which arise because it is not yet possible to create identical carbon nanotubes in large quantities. The slight differences would make it difficult to optimize the thresholds. The ambipolar device has an advantage in that the thresholds can be tuned after the gate is fabricated and with greater accuracy, since it relies on an adjustable offset voltage. Moreover, both inverters are based on 1st generation gate structure. If the 2nd generation CNFETs were used, better characteristic would have resulted.

1.16.1.3 Resistor-Transistor Logic Inverter

Another way to create an inverter is to use Resistor-Transistor Logic (RTL). A schematic of an inverter in RTL logics is shown in figure 46.

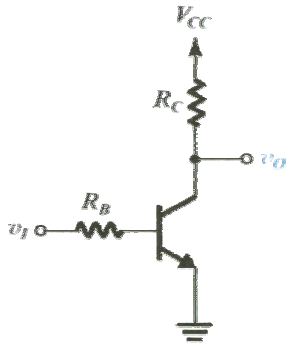

Figure 46[20] – Schematic of an inverter using RTL technology.

In this logic, only one n-type transistor is used. When a logic 0 (0V) is applied to input, V_I, the n-type transistor turns off. Resistor R_C is now free to pull the output, V_O, to logic

1 (V_{CC}). However, when V_I is at logic 1 the transistor is turned on. The lower resistance of the transistor means that R_C is too weak to pull the output to V_{CC}. Instead, a path to ground is created and the output is pulled to logic 0. In both cases, the output is set to the opposite of the input. It is important to note that RTL is an early logic family that was give up for CMOS (Complementary-Metal-Oxide Silicon) technology, which uses complementary MOSFETs. CMOS technology provides higher performance than the RTL technology.

RTL inverter can be created with CNFETs. Figure 47 shows both the schematic along with the transfer curve.

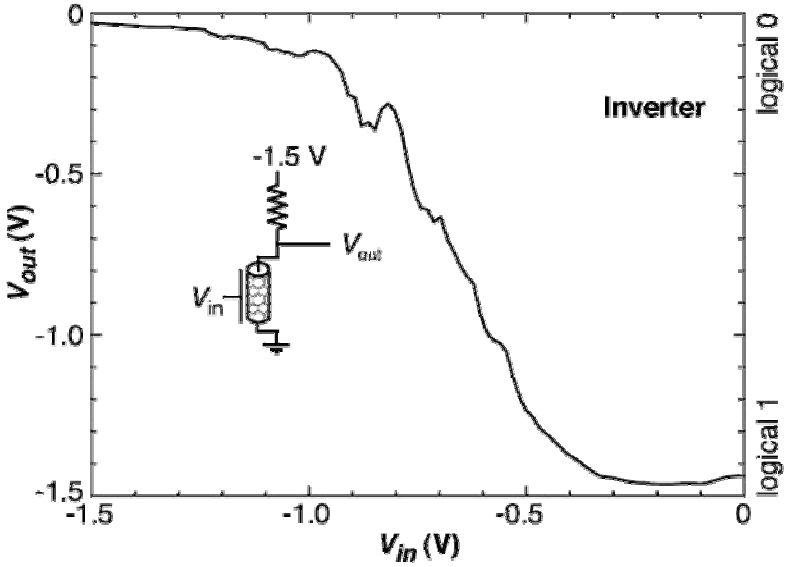

Figure 47[30] – Transfer curve for a CNFET inverter, using RTL technology. Only a n-type CNFET is used.

The slope of the curve is steep, suggesting a fast transition and a high gain. In fact, the gain is estimated to be about 3. The high gain means that it will be easily able to drive any circuit. The power consumption is low since the voltages involved are small. The high gain can be attributed to the geometry of the transistor used. A diagram is shown in figure 48.

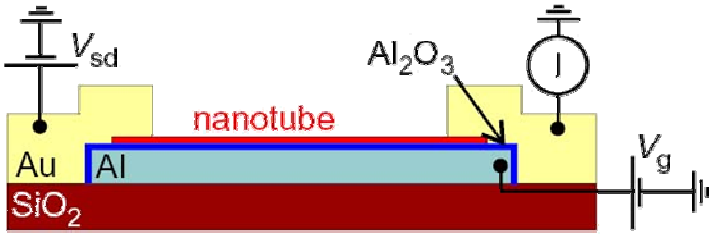

Figure 48[29] - Diagram of an RTL inverter, using a hybrid design of the first and second generation.

The geometry is a hybrid of both generations of CNFETs. It has a back gate design like the 1st generation but it does not use the substrate as the gate. Instead, a separate contact

is made under the nanotube, along with a thin gate oxide of about a few nanometers, allowing for excellent gate-tube capacitance[29]. The small oxide thickness allows the transistor to operate with less power, faster frequency, and higher gain.

1.16.2 Intra-Nanotube Inverter

Another way to build an inverter is to use a single nanotube, the intra-nanotube inverter. This design represents the ultimate integration for nanotube electronics. It avoids the problems associated with using slightly different nanotubes. It uses the same traditional schematic as the n- and p-type inter-nanotube inverter, which is shown in figure 43. A picture of the intra-nanotube inverter is shown in figure 49.

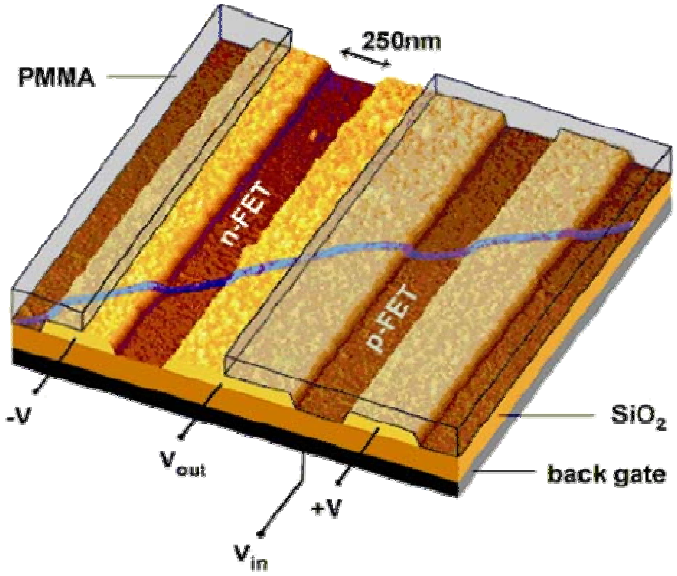

Figure 49[28] – Intra-nanotube inverter, n-FET left open for doping.

Its construction is similar to the n- and p-type inter-nanotube inverter, except that only one nanotube is used, which is draped across the contacts. The gate in figure 46 was created using the doping method, but just as well could be created using the annealing method. Its transfer curve is plotted in figure 50.

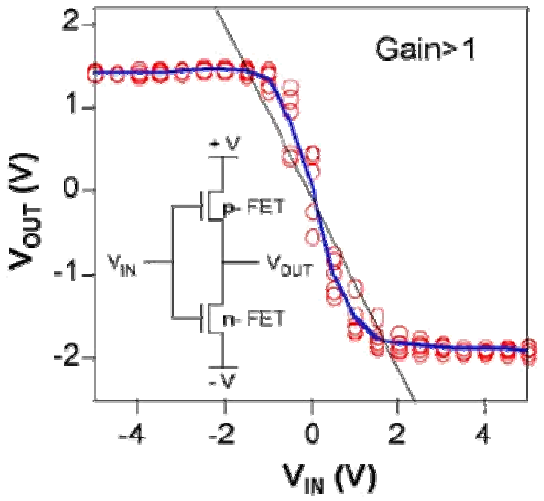

Figure 50[28] – Transfer curve of the intra-nanotube inverter. The straight line represents a gain of one.

The straight line represents a gain of one. The transfer curve goes beyond it, indicating a gain that is greater than one. In fact, the gain is about 1.6. The high gain means that the inverter could easily drive other circuits. The surprising thing is that it can achieve the high gain even while using the 1st generation CNFETs. With the second generation CNFETs, a slightly high gain could be achieved. In addition, the curve is sharper and steeper than both types of inter-nanotube inverters. Thus, the intra-nanotube inverter is faster than the inter-nanotube inverters. Also it consumes less power since the voltages are smaller than the inter-nanotube inverters, with the exception to the RTL inverter. If it were implemented with the 2nd generation CNFETs, it would require even smaller voltages, thus consume less power. The RTL inverter hints at this, with its hybrid design. Therefore, the intra-nanotube design provides superior performance and is convenient to package, since it uses only one nanotube.

1.17 Other Circuit Elements

Most of the other logic gates and circuit elements have been made using the RTL technology with the hybrid geometry design. This is because the 1st generation uses the substrate as a common gate, preventing individual switching of the transistors. The inverter was the only one that could be made using the 1st generation since it was the only logic element whose transistors share the same input, or gate. The hybrid design avoids this problem by having individual gates for each transistor. Now that the 2nd generations CNFETs have been created, it is only a matter of time before other logic gate and circuit elements, based on complementary CNFET logic, start popping up. Eventually they will evolve into intra-nanotube design, similar to the intra-nanotube inverter.

1.17.1 NOR Gate and Other Logic Gates

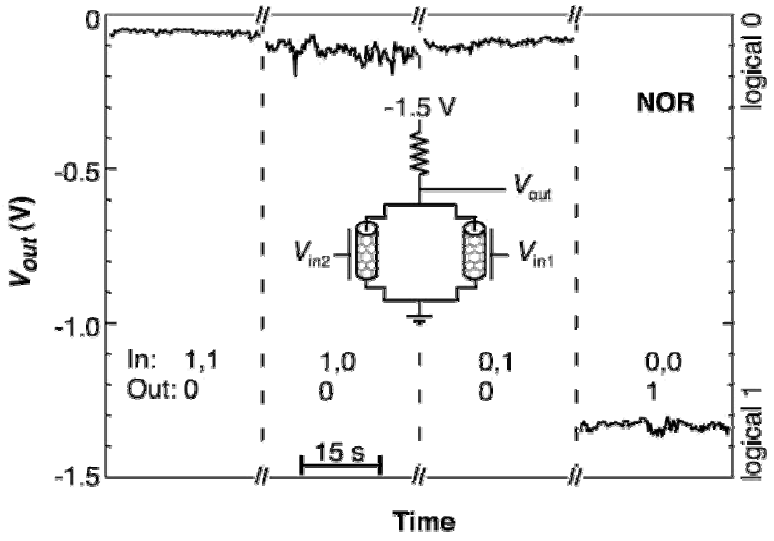

Figure 51[29] – Schematic of a RTL inverter with CNFETs, along with its output voltage as a function of inputs.

The NOR gate is the opposite of an OR gate. Therefore the NOR gate's output is 1 only when both inputs are 0, else the output will be 0. Figure 51 shows the gate operating as a NOR gate. It is constructed by placing two n-type CNFETs in parallel. To make other logic gates, such as NAND, AND, OR, XOR, and XNOR, only slight modifications to the schematic of the NOR gate is required[29]. For example, to make a NAND gate the CNFETs would have to be in series instead of parallel, as in figure 52.

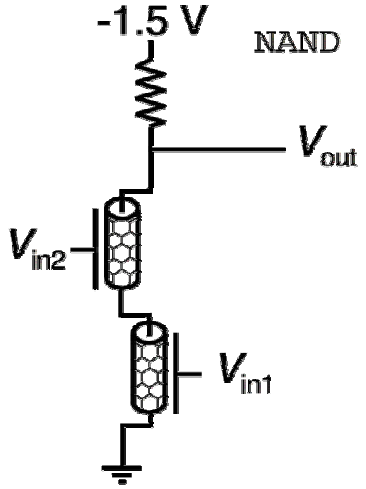

Figure 52 – Schematic of a RTL NAND gate, using CNFETs

1.17.2 SRAM Flip-Flop

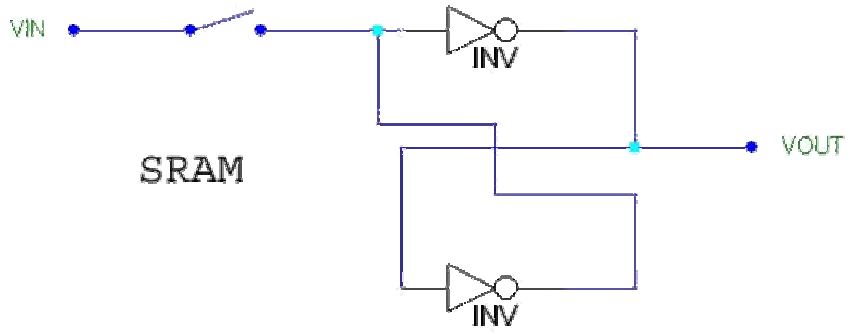

Figure 53[29] – Logic schematic of a SRAM cell, which is nothing more than a D flip-flop

An SRAM is a D flip-flop that holds a logical value. It is constructed using two inverters; the schematic is shown in figure 53. The output of the first inverter is both the output for the circuit and the input for the second inverter. The second inverter's output is fed back to the input of the first inverter. When loading a value, its opposite is fed into V_{IN} and the switch is closed. The new value is looped through both inverters.

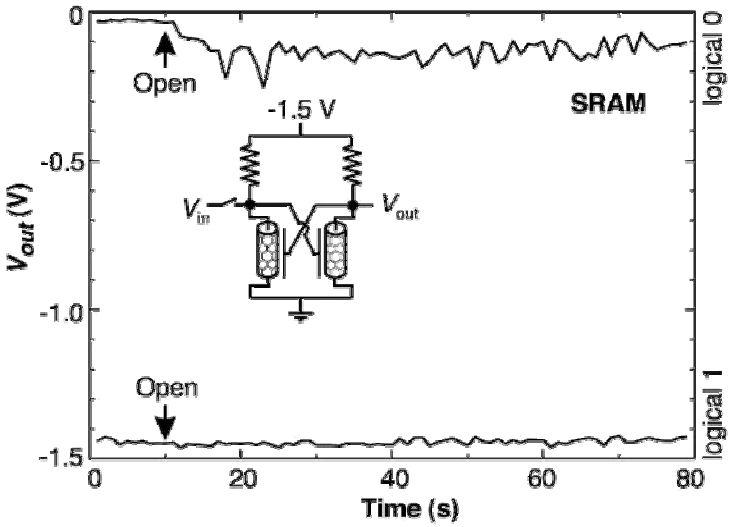

Figure 54[29] – Schematic of a RTL SRAM with CNFETs. The storing of logical state, 0 and 1, are shown after the switch is opened.

The carbon nanotube version is shown in figure 54. Both logic states are analyzed. For the first 10 seconds the switch is closed and the input value is loaded. After 10 seconds, the switch is opened and the circuit holds that value for about 80 seconds.

1.17.3 Intra-Nanotube OR

As stated earlier the evolution of the logic structures is heading towards the use of 2nd generation intra-nanotube CNFETs. An example is an OR gate, shown in figure 55.

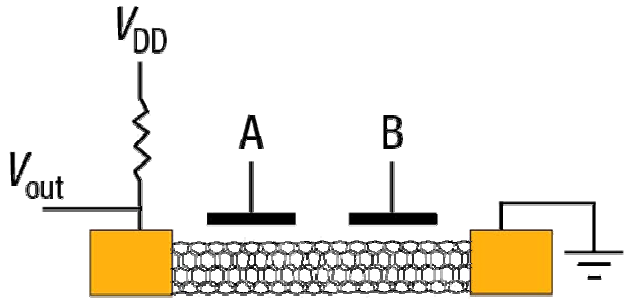

Figure 55[31] – Diagram of a RTL inverter using a 2nd generation CNFET with 2 two gates.

The gate still uses RTL logic, but it makes use of 2nd generation geometry and a p-type CNFET. In addition, the CNFET used uses two gates. If any one of the gates is on, the transistor will turn off, allowing the resistor to pull V_{out} to logic 1 (V_{DD}). If both gates are off, than the transistor turns on and pulls V_{out} to logic 0 (ground). Figure 56 shows the output voltage as a function of input.

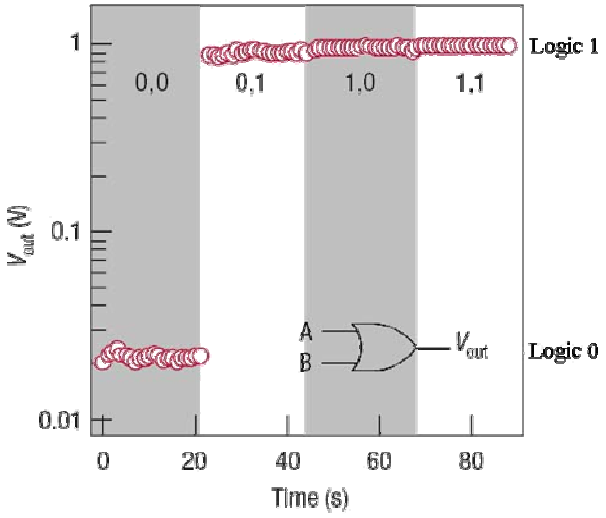

Figure 56[30] – Output voltage as a function of input.

If an n-type CNFET was used instead of the p-type then the logic gate would operate as a NOR function, since any gate with a logic 1 would turn on the CNFET and pull V_{out} to logic 0, else if both gates are logic 0, then the transistor will turn off and the resistor will pull V_{out} to logic 1.

1.18 Memory

Memory systems are important part to any digital system. So it is natural that memory systems be developed that use carbon nanotubes. The simplest way to make

them is to follow the conventional memory systems, such as flip-flops or both static and dynamic RAM. To do this, just simply replace the conventional transistors with CNFETs. However, this is not advantageous because we are not harnessing the full potential of the carbon nanotubes. CNFETs possess unique properties that were not available for use before, and could potential produce memory systems that go beyond the abilities of the conventional memory system designs.

1.18.1 Electromechanical Nanotube Memory

One system uses two layers of nanotubes. The bottom layer is composed of parallel SWNTs. The top layer is composed of parallel SWNTs, rotated 90° compared to the lower layer. A picture of the memory array is in figure 57.

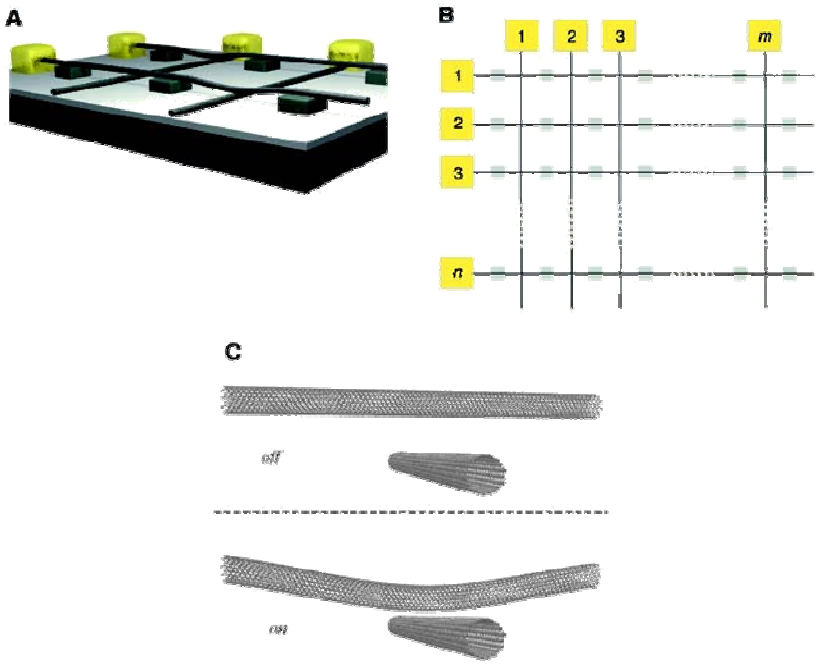

Figure 57[32] – Memory device based on 2 layers of carbon nanotubes, in which the top layer is suspended above the lower layer. (A) A 3D view, gold structures are the contacts, and the black cubes are nonconductive supports. (B) A 2D view showing the matrix used each cross represents a bit. (C) The off state is a normal suspension, while the on state has the top layer bent down towards the bottom.

Figure 57(A) shows a 3D view of the memory system. The gold structures are the contacts, and the black squares are the supports for the top layer of nanotubes. Each cross over point represents a bit and is addressed by referring to its position in the array, (n, m). A logical one (on) is represented by the bending of the top nanotube towards the bottom, as in figure 57(C). Switching between and on and off state is done by transiently charging the nanotube to cause a repulsive or attractive force between the top and bottom nanotube. Reading is accomplished by referring to the bits position in the matrix and looking at the resistance between the two nanotubes. The resistance is dependent on the distance between the two nanotubes. In the on state, the two nanotubes touch and

therefore the resistance is significantly smaller than when the two nanotubes are separated, as is the case for the off position.

Its advantages are that it is theorized to be able to achieve densities of 10^{12} bits per centimeter and can possible achieve an operational frequency in excess of 100 gigahertz[31]. In addition, since it is an electromechanical system, it is nonvolatile, meaning it will never forget the values it stores. However, its mechanical nature causes a problem in that the writing time might be slow, since it has to physical bend.

1.18.2 Electrical Nanotube Memory

Another method is to use an oxide layer to capture a single electron. The single electron would represent a bit. The advantage of a single electron is the drop in power consumption, since the current is composed of only one electron. Attempts have been made to use inorganic SETs, since SETs are the most sensitive charge detectors. However, they are difficult to design to operate at room temperature. To date there has been no attempts to use CNSETs. A solution is to instead use CNFETs. Since the nanotubes are one-dimensional ballistic conductors, a single electron change in the charge is propagated throughout the nanotube, affecting the contacts and thus changing the threshold voltage, (voltage required to switch the transistor). The electron could be captured in the gate oxide, or in an additional layer sandwiched inside the gate oxide layer. In either case, the layer needs to have sufficient electron traps, to hold on to the information. Figure 58 shows an example using an additional layer.

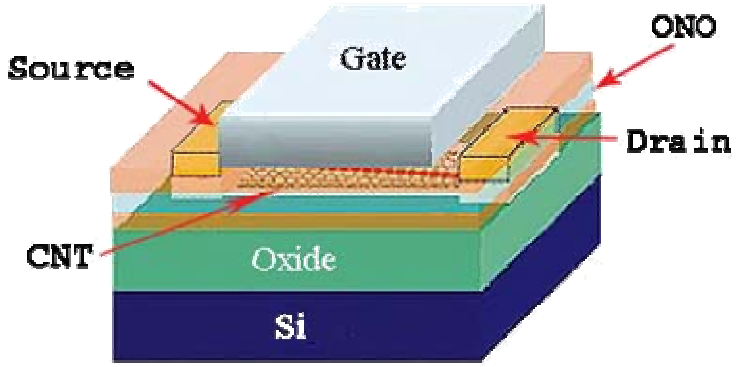

Figure 58[33] – Diagram of a single CNFET used as a memory device. A single bit is stored in the ONO (SiO_2-Si_3N_4-SiO_2) layer as a single electron.

The transistor uses the 2nd generation design, so its perforce is good. The ONO (SiO_2-Si_3N_4-SiO_2) isolates the gate and allows some electrons to enter the Si_3N_4 layer, where they are stored. An example of using the gate oxide layer its self is shown in figure 59

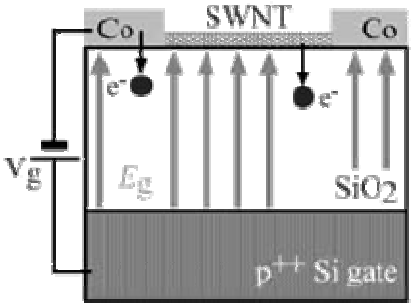

Figure 59[34] – Diagram of a single CNFET used as a memory device. A single bit is stored in the oxide layer as a single electron.

The advantage is that no extra layer is required. However, the disadvantage is that because of its 1st generation based design, the oxide thickness is required to be thick to prevent the trapped electron from tunneling trough to the gate. Second generation designs with different gate oxide layer would work better since the oxide thickness would be less.

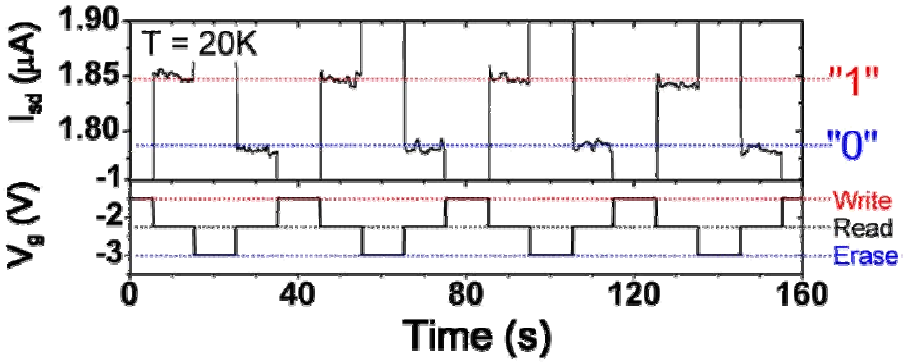

Figure 60[35] – Waveform showing the operation of the single CNFET memory device. The write command writes a 1, the erase writes a 0, and the read reads the current through the nanotube to see which logical state is stored.

A waveform for a simulation of an electron nanotube memory device is shown in figure 60. The bottom graph represents the control signal to the device, which is the voltage level applied to the gate. A write state means that a 1 is written, an erase state means a 0 is written, and a read state is used to read the information stored. When a write state is initiated, an electron enters an oxide layer, whether it is a sandwiched oxide layer or the gate oxide itself. The 1 is resented by an increase in current of about 50nA. During the read state the values is held and the information is read out in the form of a current of 1.85μA. When the erase state starts, it writes a 0 by removing the electron from the oxide, and then a read state can read the 0 as a current of 1.80 μA. One important thing to note is the simulation occurred at a temperature of 20K. The highest operation temperature today is 100K; this is because the oxide layer cannot hold on to the electron long enough at room temperature. A new oxide layers that can trap electrons better are required for room temperature operation.[34-36]

1.19 Interconnects

In any circuits or chips, the individual gates need to be connected. The wires used are called interconnects. While it is possible to use the metals that are used in conventional circuits to make the interconnects, the use of metallic carbon nanotubes would be a much more desirable, due to there better electrical properties. The ballistic transport of the metallic nanotubes would enable significantly lower resistance in the interconnect as compared to the metal ones. In addition, the reduced scattering means that there will be a reduction in the time delay as well. The problem of using metallic nanotubes is separating them from the semiconducting nanotubes and controlling their placement on the chip. While there are processes to filter out the metallic from the semiconducting nanotubes, these processes destroy the metallic ones. An example is the constructive deconstruction process developed by IBM. This process uses the substrate, which the nanotubes are deposited on, to turn off the semiconducting nanotube and burn away the metallic ones.[37]

1.20 Direct Fabrication Using Chemical-Vapor-Deposition

One solution to the placement problem is to directly fabricate the nanotubes utilizing chemical-vapor deposition (CVD). By controlling the placement of the catalyst, the positions of the nanotube can be controlled. The catalyst can be placed as a thin layer that can then be either patterned using photolithography or by heating either the thin film or microcapsules and producing catalyst nanoparticles[38,39]. Alternatively, the catalyst could be placed using an ink jet printing system. However, the nanotube growth direction is random. One way to control the direction of growth is with a magnetic field of about 1.5 Tesla. The nanotubes grow in the direction of the applied magnetic field[40].

This method is great if you want all the nanotube to grow in the same direction. For large VLSI circuits and chips, we would need them to grow in multiple directions. On option would be to use multiple growth steps, with each step having a different field direction. However, this method is very inefficient, due to the multiple steps. Another alternative uses scratches in a substrate to control both the placement and direction of the growth, all in one-step. A silicon(100) substrate is used with a 100nm thick silicon dioxide cap. The oxide layer is patterned using photolithography. The nanotubes grow normal the patterned oxide layer, with growth only on the silicon dioxide regions and avoid the silicon areas. The gas vapor used is xylene/ferrocene ($C_8H_{10}/Fe(C_5H_5)_2$). Since the vapor includes the catalyst and the carbon, no pattering or placement of a catalyst is need. Figure 61 shows an image of nanotubes grown in multiple directions, to form flowers, in a single step. The centers of the flowers are vertical nanotubes and the petals are horizontal nanotubes in different angles.[40]

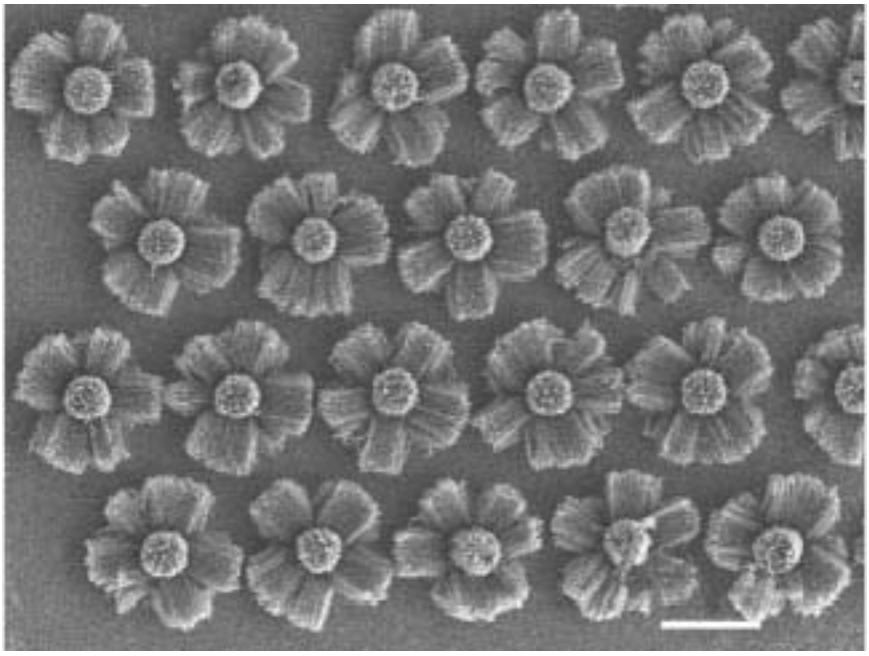

Figure 61[41] – Image of nanotubes grown in multiple direction all in one-step.

Problems to Solve

1.21 Chirality

While new CVD techniques have enabled control over both the position and the diameter of the nanotubes, there is still no way to control the nanotube's chirality. This means that there is no way to control whether a nanotube is metallic or semiconducting. With out this control VLSI circuit and chip cannot be made. There is some hope though. A group a Cambridge found that when bundles of nanotubes are grown using magnetic field alignment, the individual nanotubes in a bundle had the same chirality. However, the chirality between bundles varied. The reason why is not understood. But if the physics explaining why the individual nanotubes in a single bundle posses the same chirality then it might be possible to replicate the physics and precisely produce and place metallic nanotube to form interconnects and produce and place semiconducting ones to construct the transistors.[42]

1.22 Accurate Simulation Tools

After designing circuits, simulation is required to test the design before they are fabricated. Currently there is no accurate model to use for simulation of circuits using CNFETs. The problems stem from the unique properties form the nanotubes, such as ballistic conductance and contact switching. One group made an attempt by creating a Universal Device Model (UDM)[43]. The UDM uses previous qualitative measurement of a device to simulate the device. During simulation, the model looks back at the stored

measurement to predict the output. Since it is based on qualitative measurements that are subjected to errors, its accuracy is limited by the accuracy of the past empirical measurement of the devices characteristics. An independent model that only relies on equations is required for commercial development of chips using CNFETS.

1.23 Multiple Level Interconnects

While there has been work towards controlling chirality to produce metallic nanotubes for interconnects, there has been no research towards developing multiply level interconnects. Conventional VLSI chips have more than one level of metal interconnects. This allows wires to travel over each other, thus reducing space. With out them, chips, such as the Pentium series, would not be possible. One possible solution could be to use multi-walled nanotubes, since they are stacked SWNTs. However, each layer is coupled to each other. Therefore, the different layers still need to be isolated from each other so cross talk would not occur. More research is required to figure out how.

Conclusion

Carbon Nanotube Transistors have come along way in the past 5 years. There development is even outpacing the convention transistors when there were at the same stage of development. With the 2nd generation transistor meeting and in some cases beating the conventional transistors, the further optimization and development of the carbon nanotube transistor will certainly allow them to be a viable option to replace conventional transistors. However, some major hurdles need to be overcome, such as the control of chirality, before VLSI chips with carbon nanotube are developed. Despite the problems research in CNFETs should prove fruitful.

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