Output Hazard-Free Transition Delay Fault Test Generation

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Abstract - Scan based timing comparison tests offer a potential solution to the problem of small delay detection in aggressive nanometer technologies. However, such tests require that circuit delays be unambiguously captured in the scan chains using multiple fast clocks. To ensure this, only those signals that are known to be hazard free at capture are analysed for timing information from the scan-out data. In this paper we present the first systematic ATPG driven approach for generating high coverage output hazard free TDF tests for scan delay testing. Results indicate that acceptable coverage can be achieved, no worse than about 10% below the unconstrained TDF coverage for both LOS and LOC tests, even in the presence of significant process variations.

I. Introduction

Recent technology generations display a noticeable increase in delay defects that impact circuit timing. Such defects are commonly caused by gate oxide failures and resistive opens in the vias and interconnect. Research interest has specially focused on small (fine) delay defects, which can often remain hidden within circuit timing slacks and timing margins during testing. While it is sometimes argued that such defects, not detectable at the rated clock speed during test, are functionally benign and can be ignored, there is an emerging consensus that small delay defects can result in functional and/or reliability failures in the field. Such defects must be detected to ensure acceptable product quality and reliability in high end ICs.

There are two reasons that make it important to target small delay defects during test [1]. Switching delays in CMOS are highly input dependent. Meaningful delay testing requires that worst case delays be tested in the circuit paths. However, such worst case tests with even moderately high coverage are virtually impossible to generate and apply in practice. And even those effective tests, such as robust path delay tests, that can be generated by ATPG often cannot be applied in practice because of structural restrictions which allow only launch-on-capture (LOC) and launch-on-shift (LOS) tests in a scan environment. It is easily possible for a small delay fault to remain undetected during the test, but cause functional failure in the field when worse case input conditions are encountered [2]. Furthermore, many small delay defects are known to degrade in operation and cause early life failure. For example, a resistive open caused by a minimally connecting via can become a complete open in operation due to metal migration. Unfortunately, traditional burn-in stress testing used to eliminate such "latent" manufacturing flaws is becoming extremely expensive for delicate nanometer technologies; it also appears to be losing effectiveness in accelerating certain types of early life failures. As a result, industry is looking for alternate low cost methods for eliminating latent defects. To quote from the 2006 "Research Challenges in Test and Testability" published by the Semiconductor Research Corporation: "*In order to achieve low DPPM levels without additional acceleration such as burn-in, fine delay defect screening appears to offer a solution.*"

Unfortunately, the detection of small (fine) delay defects that fall within circuit timing margins is proving extremely challenging. Effective delay testing often requires faster-than-rated clock tests to discover defects within the timing margins. Even more aggressive detection of small delay defects hidden within the circuit timing slacks in short paths, can require the use of multiple fast clocks. Here each fast clock is used to test only those paths that are shorter than the corresponding clock period; the captured response from longer paths must be masked out and ignored during test evaluation. However, this requires knowledge of the switching time for each signal for each applied test, information which has been traditionally obtained through timing simulation in test systems such as Cadence Encounter (True Time) [3]. However, given the high levels of performance variability from normal process variations observed in current technologies (switching delays for the same path can easily span a 2X range across production lots), meaningful delay simulation to support such a small delay test methodology appears no longer viable. The problem is further aggravated by the "out-of-normal-mode" nature of single cycle scan delay tests which can display additional timing variations because of power supply noise[5,8], temperature differences in the test mode[7], and "clock-stretching"[15].

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An alternative to obtaining the expected switching delays from simulation in faster-than-rated-clock tests is to directly measure and compare such delays in matched ICs to detect delay faults. The Fmax, DDSI [12] and Self Timed [9] techniques are all faster-than-rated clock scan delay test approaches that have been proposed in recent years. The presence of multiple identical cores in state-of-the-art microprocessors makes a comparison delay test methodology even more attractive [15]. Since the performance of identical circuits located physically close to one another on silicon is generally well matched, except for random with-in die variations, the impact of process variations is minimized in such comparison testing. (It is clearly impossible to distinguish delay defects that fall within random timing variations.) An important additional advantage of such comparison tests is that all "out-of-normal-mode" effects associated with the scan delay tests equally affect timing in all the matched circuits that are tested and are thereby factored out in the comparison. A timing mismatch beyond the expected normal statistical variations between the matched circuits is an indication of a small delay defect.

While comparing timing between matched cores or die appears to be attractive option for scan based timing tests, it imposes additional restrictions on the delay tests: the applied tests must be hazard free at all observed outputs [6, 12]. This is because the goal of the comparison tests is to compare the observed switching delays in final stable signals at the circuit outputs at the observation time. A hazard can cause the test to record an incorrect and arbitrary value for a signal, leading to false error indications or test escapes.

While there has been some prior work, this paper is the first to present a systematic ATPG based approach for generating output hazard free (OHF) transition delay fault (TDF) test patterns for scan based delay testing. The rest of the paper is organized as follows. Section II reviews prior research related to output hazard free tests. Section III explains our general OHF test generation methodology using standard N-detect TDF ATPG tools. Section IV presents an innovative approach for generating additional diverse (N-detect) TDF tests for launch-on-shift (LOS) and launch-on-capture (LOC) scan delay tests. Also presented are simulation results showing the improved OHF TDF test coverage from this technique. Section V presents coverage results for combined LOS and LOC, and studies the impact of process variation on OHF TDF coverage. The paper concludes with Section VI.

II. Relation to Prior Research

Output hazard free TDF test sets for scan delay testing were first developed and applied in a Philips experiment [6] aimed at studying the potential of detecting "fine" delay defects with appropriate tests. The test generation methodology employed was straightforward. ATPG generated TDF scan delay tests were analysed using a timing simulator, and outputs with potential timing hazards were masked out. This led to a substantial degradation of TDF coverage, to approximately 40% and 60% for the two test sets considered. However, achieving high coverage was not the aim of this feasibility study. In [10], logical hazard masking was used to obtain output hazard free TDF tests from an initial test set that was generated from random patterns. While somewhat better coverage was reported, the results were still conservative when compared with the coverage that can be obtained if timing information is also taken into consideration. Many potential hazards that are logically possible are in fact filtered out in real circuits because of the actual timing relationship between signals. We present the first ATPG driven output hazard free TDF test generation

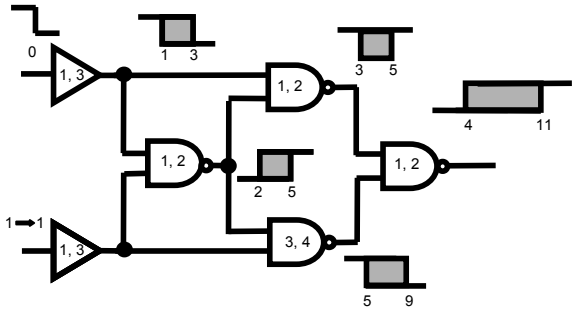

Fig. 1. Min-Max Timing Simulation

methodology in this paper, using low cost min-max timing simulation. Our timing simulation also allows for the significant process variations observed in advanced nanometer technologies. The results present here indicate that acceptable coverage can be achieved, no worse than about 10% below the unconstrained TDF coverage for both LOS and LOC tests, even in the presence of realistic process variations.

III. Output Hazard-Free (OHF) Test Generation Methodology

Recall that a transition delay fault (TDF) test is a two pattern test <v1, v2> which causes a rising (falling) transition at the target node, while v2 is simultaneously also a stuck-at 0 (stuck-at 1) test for the node. We develop a methodology for Output Hazard-Free Transition Delay Test generation. The basic objective is to generate TDF vectors that detect transition delay faults without generating a hazard on the observed output lines. Hazards may occur on other outputs, but those outputs are masked out and ignored. Test generation proceeds in two steps: conventional TDF test patterns are first generated, then a timing simulator is use to filter out those tests that can potentially display hazards at the output. Additional TDF tests are then generated for the dropped faults, and the process repeated until sufficient coverage is obtained.

Our OHF TDF generation strategy relies heavily on the ability of generating multiple diverse TDF vectors for the

same targeted TDF fault so as to maximize the probability of detecting the fault even if many of the tests are invalidated because of output hazards. In the first step, our strategy uses N-detect transition delay vectors generated from conventional TDF ATPG that is configured to favour driving faults effects towards outputs that are statistically observed to have fewer hazards. This test pattern set obtained from TDF ATPG is further augmented by a unique methodology for obtaining additional TDF vectors for the same fault based on stuck-at vectors obtained from n-detect stuck-at ATPG. The stuck-at vectors generated from the conventional ATPG provide the v2 vector in the two pattern TDF delay test, <v1, v2>, for the target fault. The v1 vector to be associated with each v2 is constrained by the structure of scan chains. The techniques for generation of vector v1 depend upon the capture procedures applied in the scan environment. For a Launch-On-Shift (LOS) test, vector v1 for the two pattern delay test is simply obtained by applying a one-bit shift to v2 in the direction opposite to that of the normal scan shift. This v1 however does is not guarantee the desired transition at the target node when applied as an LOS test; several v2 vectors from the N-detect stuck-at set for v2 are therefore tried until the desired TDF test is obtained. For Launch-on-Capture (LOC) tests, finding a v1 vector to go with the v2 vector generated by stuck-at ATPG is more challenging; the v1 vector is obtained as a stimulus for the combinational block that leads to the v2 vector as the next state. Our novel ATPG based n-detect TDF test generation methodology creates a richer set of TDF patterns, which are more likely to contain the desired OHF TDF test patterns. OHF TDF test patterns are next selected from candidate TDF test using efficient timing simulation to achieve high coverage tests as described below.

The second step of our test generation methodology involves filtering of the above generated diverse set of transition delay patterns to eliminate those tests that generate hazards at the observed outputs. This filtration is achieved by using a min-max delay simulator developed by other fellow researchers [13]. The min-max simulator uses a bounded delay model, where in each gate is assigned the lower and upper bounds for delay, also called the min-max delay specification [14]. These delays depend on the best and worst case switching delays (gate inertia) for the gate. To define and represent signal timing in the bounded delay model, we use the term ambiguity region. This timing region is shown in Figure 1 as the shaded region at the outputs of the gates. This ambiguity region represents an area of signal uncertainty i.e. the signal may transit in that region, possibly more than once creating a hazard, but the exact timing of the transitions is uncertain. *The simulation makes the conservative assumption that a hazard always occurs at the output of a gate if the ambiguity region is large enough to accommodate the multiple transitions needed to create the hazard*, based on the most favourable (minimum) switching delays for the gate. A circuit output can be termed hazard-free for the TDF test vector applied if there is no possibility of a hazard. On the other hand if the test stimulus applied to the circuit generates hazards on certain output lines, these output lines are masked out and not observed for fault detection. The min-max delay simulator can also be used to deal with performance variability occurring due to manufacturing process by including a tolerance with the use of bounded delay model [13,14]. For the simulations results presented in this paper, this variance is conservatively taken to be 30%, i.e. any switching delay can vary 30% from its nominal value. This min-max modelling approach dramatically decreases the computational complexity that is required to filter transition delay vectors as compared to full circuit SPICE simulation, which is not a feasible option for large circuits.

Because many of the transition delay vectors get invalidated due to potential output hazards detected by the min-max delay simulation and

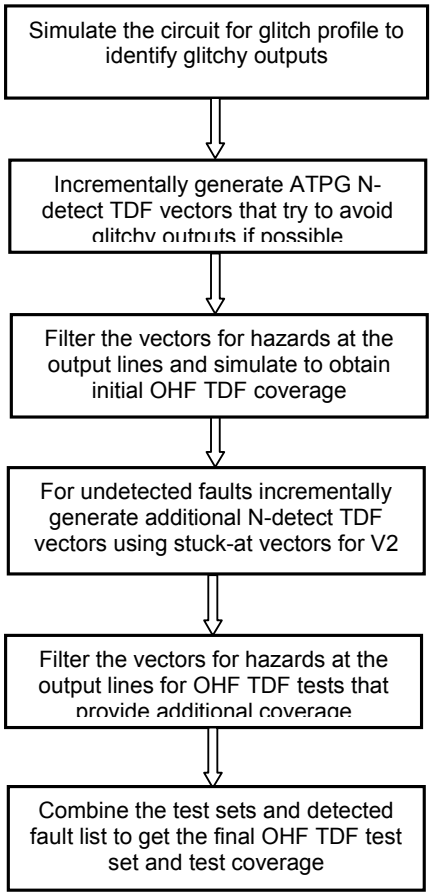

Fig. 2. Overview of OHF TDF Test Generation Flow

filtering procedure, we need N-detect TDF vectors as alternate tests to cover the dropped faults. As outlined above, these are obtained by using our novel techniques to generate multiple TDF test vectors for a given fault.

While standard TDF ATPG can generate N-detect TDF vectors, for both launch-on-shift (LOS) and launch-on-

capture (LOC) scan delay test, it is usually unable to provide a diverse enough N-detect vector set to give a satisfactory coverage after the vectors are screened for the hazards. Based on observations over many experiments, we have developed an effective method for incrementally creating additional TDF vectors for a given fault. Figure 2 illustrates the step by step procedure for the incremental TDF test generation methodology. The success of this incremental N-detect methodology lies in adapting the ATPG tool towards the constraint posed by the timing screening to detect hazards. This adaptation of the ATPG tool requires a profiling of a circuit for identifying the most glitchy output lines. This profiling is done so as to avoid ATPG effort towards generating transition delay vectors that would propagate the faults through these glitchy output lines. Every circuit undergoes this profiling using a stimulus of 1000 random vectors and the above described min-max delay simulator. We create two versions of every circuit during test generation. One version of the circuit has those lines that have a high likelihood of a hazard (above some threshold) constrained to an 'X'. This constraining of the most glitchy output lines to an unobserved value forces the ATPG to avoid these lines for fault propagation. The second version of the circuit is the normal netlist without any constraint. These two versions of the circuit are provided to the ATPG for transition delay vector generation. We then apply the incremental N-detect transition delay vector generation technique on these two versions of the circuit, at each step (run) first using the glitch constrained version of the circuit, and then the unconstrained version. Our technique involves multiple runs that incrementally use N-detect TDF vector generation. The first run is with N=1 uses TDF vectors generated from the conventional ATPG. The faults that are detected by this run (N=1) are dropped from the undetected fault list and the TDF test patterns from this run saved as the delay test set. The undetected fault list from this run serves as a new fault list for the next run (N=2). Thus each run involves dropping of the detected faults, forwarding the undetected fault list to the next run and adding the new OHF TDF vectors to the delay test set. This process is continued until the fault coverage is saturated. The test pattern sets from these multiple runs, on both versions of the circuit, are appended together to yield a comprehensive delay test set.

The above approach of using output constraints and incremental TDF vectors forces the ATPG to generate multiple TDF vectors where needed and enhances the probability of obtaining a high coverage hazard filtered TDF test set. However, using conventional N detect TDF ATPG alone often does not provide a diverse enough set of N-detect TDF vectors as a starting point for obtaining high coverage OHF TDF tests. Therefore, the undetected fault list at the end of this first phase of OHF TDF generation is further also used as the target for incrementally generating additional N-detect TDF vectors, using a novel approach that begins with appropriate stuck-at "seed" vectors as the v2 vectors. (Recall that the v2 vector is a stuck-at 0 for a slow-to-rise transition fault and stuck-at 1 for a slow-to-fall transition fault.) Such v2 vectors can be easily obtained from conventional N-detect stuck-at ATPG and can be used as the second vector in the basic two pattern <v1, v2> delay test. The corresponding v1 for each v2 is generated by taking into consideration the structural constraints of launch-on-shift (LOS) and launch-on-capture (LOC) scan test procedures, as explained in the following section. We again use a similar test flow to phase 1, beginning with the same two versions of the circuit obtained by glitch profiling, and incrementally generating additional N-detect TDF tests, first using the constrained circuit if possible, until a test for the target fault is obtained.

IV. Additional N-detect TDF Test Generation

Recall that Launch-on-Shift (LOS) tests involve the use

.TABLE I: ISCAS 89 COVERAGE RESULTS (LOS and LOC)

Circuit	OHF TDF ATPG		Additional TDF Tests using Stuck-at seeds		Total OHF TDF Coverage		Unconstrained TDF Coverage	
	LOS	LOC	LOS	LOC	LOS	LOC	LOS	LOC
S208	57.34	48.92	19.67	10.31	77.01	59.23	89.7	74.11
S298	60.11	60.45	16.44	20.89	76.55	81.34	83.25	82.16
S344	67.58	66.78	15.4	22.45	82.98	89.23	94.21	93.91
S349	66.65	63.56	20.37	27.56	87.02	91.12	93.54	93.24
S382	50.58	55.42	24.25	20.67	74.83	76.09	89.91	82.45
S386	61.22	47.87	13.09	13.44	74.31	61.31	81.21	83.92
S400	62.31	57.28	16.78	18.51	79.09	75.79	89.68	85.78
S420	47.14	50.13	27.63	17.36	74.77	67.49	85.53	83.12
S444	56.78	46.14	16.39	18.58	73.17	64.72	85.65	78.67
S510	60.38	57.88	23.44	21.28	83.82	79.16	90.48	89.49
S526	54.87	41.35	17.22	15.78	72.09	57.13	86.92	83.78
S526n	55.23	40.01	14.67	18.76	69.9	58.77	86.55	74.94
S641	68.86	60.61	21.51	24.35	90.37	84.96	95.39	90.35
S713	62.11	59.78	18.44	18.83	80.55	78.61	89.76	84.14
S820	42.39	44.76	22.13	11.34	64.52	56.1	80.11	77.12
S832	46.77	36.36	22.63	16.45	69.4	52.81	79.4	84.64
S953	64.51	63.93	24.54	23.52	89.05	87.45	94.99	95.53
S1196	54.39	49.43	23.82	23.9	78.21	73.33	88.21	84.19
S1238	53.86	49.54	11.47	25.57	65.33	75.11	78.35	85.56
S1423	68.76	55.43	20.71	19.97	89.47	75.4	96.13	89.26
S1488	42.67	57.44	24.65	17.83	67.32	75.27	77.58	88.76
S1494	46.75	56.79	17.21	17.24	63.96	74.03	80.14	91.77
S5378	58.76	61.11	20.01	18.49	78.77	79.6	93.12	91.55
S9234	61.26	48.87	18.92	16.4	80.18	65.27	86.28	83.08
S13207	68.54	58.34	19.21	21.27	87.75	79.61	90.77	84.74
S15850	61.22	53.16	17.69	16.82	78.91	69.98	88.88	70.03
Ave.	**57.7**	**53.5**	**19.6**	**19.1**	**77.3**	**72.7**	**87.5**	**84.9**

of the two pattern <v1, v2> tests for transition delay faults, where v2 is a one-bit scan shift vector for v1. A hazard can potentially be generated by the applied two pattern tests and can be propagated (sensitized) to the observed output, resulting in the test being invalidated as an output hazard free (OHF) delay test. Therefore it is essential to generate multiple diverse (N-detect) two-pattern TDF vectors for each fault, biased to propagate fault effects to outputs that do not have a hazard, if an OHF test is to be obtained with high probability. We use an innovative technique for incrementally generating additional N-detect TDF vectors for a given fault to achieve this objective, starting from N-detect stuck-at vectors. The targeted faults are from the undetected fault set of the first phase that directly used conventional TDF ATPG to generate OHF test vectors.

The stuck-at 0 fault at the fault site is first targeted to obtain v2 for a slow-to-rise transition and the stuck-at 1 test is targeted for a slow-to-fall transition. These stuck-at vectors are then used as vector v2 in a TDF test pattern pair <v1, v2>. A possible candidate for the corresponding v1 vector for the target LOS TDF test is simply obtained by a one bit shift in the direction opposite to that of the normal scan shift. However, not all such v1 vectors yield a TDF test for the fault because in some cases the <v1,v2> vector pair may not activate (launch) the desired transition at the fault site. This necessitates working with N-detect stuck-at tests for v2 and fault simulating them to see which <v1,v2> pairs yield the desired TDF tests. These generated tests are then further filtered for hazards to obtain OHF TDF tests. This technique for generating multiple TDF test vectors for a target fault using stuck-at vectors as v2 is incorporated in the same incremental N-detect TDF test filtering strategy explained earlier. This results in a diverse pattern set which increases the possibility of obtaining a hazard-free delay test.

TABLE II: EFFECT OF VARIATION ON COVERAGE (LOC+LOS)

Circuit	10%	20%	30%	40%	50%
S208	84.34	81.48	80.95	76.45	74.83
S298	89.32	87.24	86.67	84.57	78.46
S344	92.05	91.73	91.73	88.47	83.64
S349	94.13	93.86	93.86	91.12	88.67
S382	79.56	79.56	78.42	76.85	74.66
S386	80.64	78.83	76.86	74.18	73.43
S400	82.78	82.05	81.31	79.64	78.58
S420	84.78	81.61	77.89	75.18	72.53
S444	78.57	77.15	76.03	71.22	69.45
S510	87.53	85.16	85.3	81.42	78.67
S526	82.57	79.32	74.68	71.18	71.18
S526n	76.23	74.74	73.14	71.37	69.45
S641	94.12	93.57	93.57	89.23	88.57
S713	89.23	86.28	85.48	83.51	81.74
S820	72.18	71.46	70.11	67.33	64.95
S832	77.18	75.68	74.56	70.14	68.3
S953	92.78	92.64	92.15	89.31	87.45
S1196	85.31	84.5	83.22	81.65	74.37
S1238	83.01	81.99	81.18	79.08	73.61
S1423	95.45	94.13	93.71	87.1	82.78
S1488	83.52	81.49	80.03	79.67	77.31
S1494	81.76	79.08	79.53	77.45	75.41
S5378	86.65	85.1	84.46	82.35	82.35
S9234	88.28	87.91	87.68	85.72	84.01
S13207	89.12	89.75	89.75	80.66	80.05
S15850	85.35	84.23	83.34	78.64	76.43
Ave.	**85.25**	**83.87**	**82.91**	**79.75**	**77.34**

Launch-on-capture <v1,v2> TDF tests are somewhat more difficult to generate from a v2 seed vectors generated using N-detect stuck-at ATPG. The LOC test requires that the vector v1 must be the stimulus to the circuit such that v2 would be the expected response. Therefore to generate the v1 vector corresponding to a target v2, we use the v2 values as constraints and again employ stuck-at ATPG to generate the corresponding v1 stimulus (while additionally constraining the fault site during v1 application to ensure that <v1,v2> launches the required transition at the fault site). The obtained stimulus completes our required <v1, v2> delay test set. These tests are then again filtered for hazards and the same test flow used again as for ATPG generated N-detect TDF tests.

Table 1 presents the OHF TDF coverage obtained from simulation of ISCAS 89 circuits for both LOS and LOC tests. Column 2 shows the saturated OHF TDF coverage from filtering N-detect TDF vectors directly obtained from the off the shelf TDF ATPG tool. Column 3 shows the additional coverage obtained from new TDF vectors generated by using stuck-at vectors (from stuck-at ATPG) as the v2 seed. Column 4 gives the total OHF TDF coverage. The results clearly show the value of the additional N-detect TDF tests generated by our innovative approach based on stuck-at v2 seed vectors in significantly boosting the attainable coverage. Overall all output hazard free (OHF) TDF coverage is only about 10% below the unconstrained coverage.

V. LOC + LOS Coverage and Process Variation

Recall that in our min-max timing simulations used to eliminate the possibility of hazards on circuits outputs, we have in Table I conservatively allowed for a 30% random variability in the delays associated with individual transitions from their nominal (min-max) values. Table 2 shows the effect of changing this variation on test coverage. The columns in Table 2 show combined LOC+LOS coverage for a varying range of variability factors. Combining the two types of scan tests improves overall delay coverage; however LOS scan tests require a high

speed scan control signal which is not supported in many designs. Observe that coverage deteriorates with high variability which increases the likelihood of hazards. However, it is bounded below by the coverage that is obtained based on logic masking alone reported in [10]. This is typically about 20% below the full unrestricted TDF coverage.

VI. CONCLUSION

Output Hazard-Free TDF tests are essential for performing timing comparison, where the logic state of a signal has to be unambiguously sensed at the sample strobe time. In this paper we have proposed an effective Output Hazard-Free TDF test generation methodology for scan based delay tests using a systematic strategy. We have presented innovative methods for incrementally generating diverse N-detect TDF tests for a target fault, which are then filtered for potential output hazards using low cost min-max timing simulation until a valid test is found. Simulation results presented here indicate that such output hazard free tests can be obtained with an average coverage of about 10% below the unrestricted transition delay fault coverage for both Launch-on-shift(LOS) and Launch-on capture(LOC) modes. ATPG effort is modest when compared to using SPICE or other similar full circuit simulators for validating the OHF TDF vectors. Future work is focused on more optimistic methods for OHF test generation in an attempt to boost coverage near to that for unrestricted TDF.

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