2019 32nd International Conference on VLSI Design and 2019 18th International Conference on Embedded Systems (VLSID)

# Energy Efficient Power Distribution on Many-Core SoC

Mustafa M. Shihab* and Vishwani D. Agrawal
Department of Electrical and Computer Engineering
Auburn University, Auburn, AL 36849, USA
*mustafa.shihab@utdallas.edu, agrawvd@auburn.edu*

***Abstract*—We propose a scheme for delivering power to parts of a large integrated circuit, such as cores in a system-on-chip (SoC), at a higher voltage than $V_{DD}$. The increased voltage lowers the current through the power grid and thereby reduces the $I^2R$ loss of the on-chip power distribution. This novel idea for VLSI devices, is inspired from the distribution system of commercial long distance power transmission networks. Our scheme steps down voltage to the $V_{DD}$ level with on-chip DC-to-DC converters placed close to the cores, in a similar way as electrical networks use transformers. The distribution grid efficiency is the fraction of the total power taken from the source that is delivered to loads (cores). SPICE simulation was done for modeled grid for SoCs. A 64-core SoC, each core operating at 1V and consuming 1W, dissipated 88W giving 73% grid efficiency. When the grid distributed 3V (close to the output of a Li-ion battery) and ideal step down converters were used, the efficiency rose to 96%. Using the data of a commercial DC-to-DC converter, we obtained a grid efficiency of 88%. This paper also points to the need for high efficiency DC-to-DC converters suitable for on-chip integration.**

***Keywords*—DC-to-DC converter, $I^2R$ loss, Low-power design, On-chip power distribution, SoC Power grid, Voltage regulator.**

## I. Introduction

Today's most powerful microprocessors can consume 100-150 watts. For battery-powered portable devices, the numbers are smaller but the problem is just as serious. According to ITRS, battery life for these devices peaked in 2004. Since then battery life has actually declined, as features have been added faster than power (per feature) can be reduced [8].

In spite of the research emphasis on low power design at architecture and logic levels, on-chip power distribution has not received much scrutiny. While power supply noise (power droop, ground bounce, coupling, etc.) has been investigated and design solutions for power grid [11]–[13], [16], decoupling capacitors [7] and transient analysis [10] exist, grid power loss and energy efficiency have only begun to attract attention [15]. Power loss can become a significant issue for a system-on-chip (SoC) even when each module or core uses low power design. A SoC typically contains many cores each receiving power through a distribution grid. The total current flow on the grid can be large, leading to significant resistive loss.

We propose a scheme for delivering power to different parts of a large integrated circuit, such as modules on a system-on-chip (SoC), at a voltage higher than the operating $V_{DD}$. This increase in voltage lowers the current on the grid, and thereby reduces the $I^2R$ loss in the on-chip power distribution network.

* Currently a PhD candidate at the University of Texas at Dallas, Richardson, TX 75080, USA.

While our idea is novel for VLSI chips, it is inspired from the power distribution scheme used in long-distance electrical networks, where electricity is transported from the generating source to users via transmission lines carrying small current at high voltage. This in turn saves enormous quantity of power that would otherwise amount to heat loss in the long distance wires [2]. We propose to step down voltage to the $V_{DD}$ level by leveraging DC-to-DC converters physically placed close to the cores, much like how the electrical networks use transformers.

## II. On-Chip Power Distribution Network at Increased Voltage

Designers of long-distance power transmission systems have always been aware of the $I^2R$ loss, and take appropriate measures to minimize the loss and enhance the distribution efficiency. A given quantity of electric power can be transmitted through a transmission line either at low voltage and high current, or at a higher voltage and lower current. When high transmission voltage is used, transformers near the customer site convert the voltage to a suitable lower voltage. Since the power lost in transmission wires is proportional to the conductor resistance and the square of the current, using low current at high voltage reduces the energy lost as heat generated in conductors [2].

According to Joule's Law, energy loss is directly proportional to the square of the current. For example, raising the voltage by a factor of 10 reduces the current by the same factor and therefore the $I^2R$ loss reduces by a factor of 100, provided the same sized conductors are used in both cases [2]. This increase in voltage is usually achieved in AC circuits by using a step-up transformer. High-voltage direct current (HVDC) is used to transmit large amounts of power over long distances, or for interconnections between asynchronous grids. HVDC systems require relatively costly conversion equipment which may be economically justified for particular projects such as submarine cables and longer distance high-capacity point-to-point transmission, but are infrequently used at present [2]. Transmitting electricity at high voltage reduces the fraction of energy lost as resistive heat, which varies depending on the specific conductors, the current magnitude and the length of the transmission line. For example, a 100 mile 765 kV line carrying 1000 MW experiences a loss of 0.5% to 1.1%. For a 345 kV line carrying the same load across the same distance the $I^2R$ loss increases to 4.2% [1].

## III. DC-to-DC Voltage Converters

In terms of voltage conversion, there are three basic categories of converters. A *buck converter* steps down a higher

2380-6923/19/$31.00 ©2019 IEEE
DOI 10.1109/VLSID.2019.00102

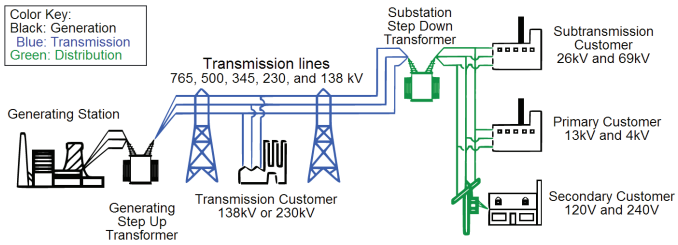


Fig. 1. A typical long-distance power distribution network [2].

input voltage to a fixed lower output voltage. In the present application, we are interested in buck converters [9]. A *boost converter* steps up a lower input voltage to a fixed higher output voltage [9]. A *buck-boost converter* converts lower or higher input voltages to a fixed output voltage [9]. A DC-to-DC voltage converter/regulator is a circuit that generates a regulated DC output voltage from a (possibly) unregulated DC input voltage of different magnitude and/or polarity [9]. Based on the underlying technology, the DC-to-DC converters can be classified into several types.

**Linear DC-to-DC Converters or Regulators:** Linear regulators generate DC output voltage with a lower magnitude and the same polarity as compared to a DC input voltage. They utilize a resistive voltage divider and have intrinsically low efficiency, particularly if the input-to-output voltage ratio is high. They are found in many types of ICs owing to their simple design, low circuit complexity, and small area consistent with on-chip implementation [6], [9].

**Switched-Capacitor DC-to-DC Converters or Regulators:** Switched-capacitor DC-to-DC converters (or charge pumps) generate DC output supply voltage with a different magnitude and/or an opposite polarity as compared to a DC input supply voltage. They contain charge pumps and are widely used in ICs to modify the amplitude and/or polarity of the primary power supply voltage of the system. Similar to a linear regulator, the efficiency of a switched-capacitor converter is typically low. Besides, the area occupied by a switched-capacitor regulator is higher than a linear regulator. However, unlike a linear regulator, a switched-capacitor DC-to-DC converter can change the polarity and also increase the amplitude of an input supply voltage. Switched-capacitor regulators are, therefore, preferred in on-chip low-to-high voltage conversion or polarity reversing applications. They are used in non-volatile memory circuits (flash and electrically erasable programmable read only memories), dynamic random access memories (DRAMs), and analog portions of mixed-signal circuits.

Primary disadvantage of a switched-capacitor DC-to-DC converter is poor efficiency. The operation of a switched-capacitor regulator relies on periodically charging/discharging the charge pump capacitors through resistive switches. The internal power losses of a switched-capacitor regulator are, therefore, typically high. Another disadvantage of a charge pump circuit is the poor output regulation. In order to maintain a steady DC output voltage, a certain amount of charge should be maintained across each charge pump capacitor. Only control mechanism that can be employed in a charge pump regulator to maintain a specific amount of charge in the charge pump capacitors under varying load current conditions is to vary the conductance of the switches charging/discharging the charge pump capacitors. This strategy, however, typically requires high energy consuming feedback circuitry, further degrading the efficiency of the regulator. An energy-efficient feedback control scheme applicable to switched-capacitor regulators does not yet exist.

**Switching Converters or Regulators:** Switching regulators are capable of modifying both the amplitude and polarity of the input voltages. The primary advantages of a switching regulator are the high conversion efficiency and good output voltage regulation characteristics as compared to a linear or switched-capacitor DC-to-DC converter. Primary drawback of switching regulators is inductive elements (inductors and/or transformers) required for energy storage and filtering. Filter inductors are, to date, prohibitive in the fabrication of an on-chip switching DC-to-DC converter.

A switching DC-to-DC converter generates a DC output supply voltage with a different magnitude and/or polarity than the DC input voltage. Among the converter topologies, switching voltage regulators are the most widely used due to the high efficiency and good output voltage regulation characteristics. Unlike a linear or a switched-capacitor DC-to-DC converter, the efficiency of this converter approaches 100% as the transistor switches get closer to being ideal.

Switching DC-to-DC converters can be divided into two primary categories. The first category of switching DC—DC converters utilizes transformers. Switching DC-to-DC converters with transformers are called isolated switching DC-to-DC converters. The primary use of transformers in switching DC-to-DC converters is DC isolation of the input and output grounds. Provided that the primary power supply operates at a relatively high voltage and/or is noisy, isolation of the load from the input supply is necessary to maintain reliable operation of the load. Another advantage of isolated switching DC-to-DC converters is the relatively easy and straightforward generation of multiple DC output voltages from a single DC input voltage. A single control circuit can be used to generate several different DC supply voltages by simply utilizing a multiple winding transformer, provided that the voltage regulation requirements of the load circuits are not excessively tight.

The second category of switching DC-to-DC converters utilizes inductors (no isolating transformers) for energy storage and signal filtering. These switching DC-to-DC converters without transformers are called non-isolated switching DC-to-DC converters. Such converters are widely used in both low power and low voltage applications. Buck and boost types of non-isolated switching DC-to-DC converters are widely used to generate voltage levels required by microprocessors, digital signal processors, memory modules, and hard disks in modern computer systems. Figure 2 gives a comparison of varios types of DC-to-DC converters [9].

## IV. Proposed On-Chip Power Grid

The state-of-the-art on-chip power distribution network (PDN) or power grid has three main components - an off-chip AC-to-DC converter, an off-chip DC-to-DC converter, and the actual chip, which can be a SoC with a number of

| Type of DC–DC converter | Linear | Switched-capacitor | Switching |
|---|---|---|---|
| Low-to-high voltage conversion | No | Yes | Yes |
| High-to-low voltage conversion | Yes | Yes | Yes |
| Polarity reversal | No | Yes | Yes |
| Efficiency | Low | Low | High |
| Voltage regulation | Poor | Poor | Good |
| Area | Small | Medium | Large |
| Typical applications | DRAM | DRAM, flash, EEPROM, and mixed-signal | microprocessors, DSPs, SRAMs, and hard disks |

Fig. 2. A comparison of state-of-the-art DC-to-DC converters [9].

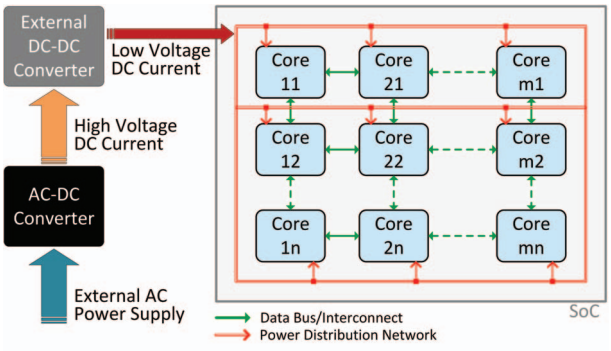


Fig. 3. Conventional SoC power distribution grid, $V_{Grid} = V_{DD}$.

cores/modules. This setup is shown in Figure 3. The AC-to-DC converter gets power from an external AC source and converts it to a high-voltage DC, which is then fed into a DC-to-DC converter that steps it down to a low-voltage $V_{DD}$. Even for portable devices that run on battery, a voltage around 3V to 3.5V is converted down to a 1V or lower $V_{DD}$ by an off-chip DC-to-DC converter. For power $P$, if voltage is $V_{DD}$ and total current is $I_{Circuit}$, then

$$P = V_{DD} I_{Circuit} \tag{1}$$

Because the regular or traditional grid of Figure 3 supplies the chip with $V_{DD}$, generally 1V or lower, if chip's power requirement is high, the current through on-chip power distribution network (grid) will be high. As a result, the $I^2R$ loss in the power grid will be high.

In order to address this power loss, we propose to remove the off-chip DC-to-DC converter from the design and feed the chip with a higher voltage than $V_{DD}$ (Figure 4). We place on-chip DC-to-DC converters [9] to step down the voltage at delivery points close to the cores, much like what is done in commercial/home power networks using transformers.

For illustratration, initially assume ideal DC-to-DC converters with 100% efficiency. Their input and output power must be the same:

$$P_{input} = P_{output} \Longrightarrow V_{Grid}.I_{Grid} = V_{DD}.I_{Circuit} \tag{2}$$

If we use a voltage that is $n$ times $V_{DD}$, grid current will be reduced by factor $\frac{1}{n}$. This in turn, will reduce the $I^2R$ loss in the grid resistances by a factor $\frac{1}{n^2}$. Therefore, this on-chip step-down voltage conversion, instead of doing it off-chip, should allow us to considerably reduce the current $(I_{Grid})$ flowing through the on-chip power network. As a result, we expect

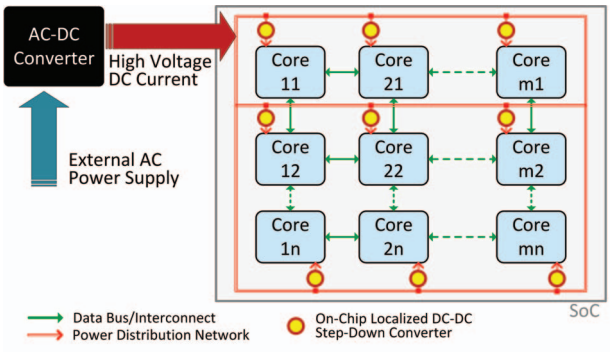


Fig. 4. Proposed high-voltage SoC power distribution grid, $V_{Grid} > V_{DD}$.

this scheme to save significant amount of power by reducing the $I^2R$ loss in the PDN.

**Selection of the Distribution Voltage $(V_{Grid})$:** Power being the product of voltage and current, for a fixed load power if we step up voltage $n$ times, the resulting current becomes $\frac{1}{n}$ of the original value. Consequently, the $I^2R$ power loss is reduced by a factor $\frac{1}{n^2}$.

If there is no limiting factor on the distribution voltage, then we increase power saving by increasing distribution voltage. This power saving results in increased efficiency of the circuit. For a distribution voltage $V$, if load power is $P_{Load(V)}$, Power lost in the grid is $P_{Grid(V)}$ and total power is $P_{Total(V)}$, then,

$$\begin{aligned} \text{Efficiency} &= \frac{P_{Load(V)}}{P_{Total(V)}} \times 100 \\ &= \frac{P_{Load(V)}}{P_{Load(V)} + P_{Grid(V)}} \times 100 \end{aligned} \tag{3}$$

When the distribution voltage is increased from $V$ to $nV$, power lost in the grid, $P_{Grid(V)}$ will decrease to $\frac{P_{Grid(V)}}{n^2}$. So, the efficiency changes to

$$\begin{aligned} \text{Efficiency} &= \frac{P_{Load(V)}}{P_{Load(V)} + \frac{P_{Grid(V)}}{n^2}} \times 100 \\ &= \frac{n^2 P_{Load(V)}}{n^2 P_{Load(V)} + P_{Grid(V)}} \times 100 \end{aligned} \tag{4}$$

Therefore, when $n \to \infty$ the efficiency approaches 100%. We can use this characteristic to increase the efficiency of a PDN. We will attempt to verify this relationship between distribution voltage and efficiency from our experimental results. In reality, however, there are limiting factors such as dielectric breakdown that set upper bound on the distribution voltage.

**Advantages of the Scheme:** The proposed scheme lowers the current flow through the distribution network to a fraction of its regular value by stepping up the supply voltage. This current reduction has expected advantages as listed below.

*Power Saving and Increased Efficiency:* The first and the most anticipated reward from a possible implementation of this scheme is power saving. We have seen from Joule's Law that resistive power loss $(I^2R)$ has a quadratic relation with current. Also, due to the law of conservation of energy, with ideal DC-to-DC converters stepping up the supply voltage $n$ times

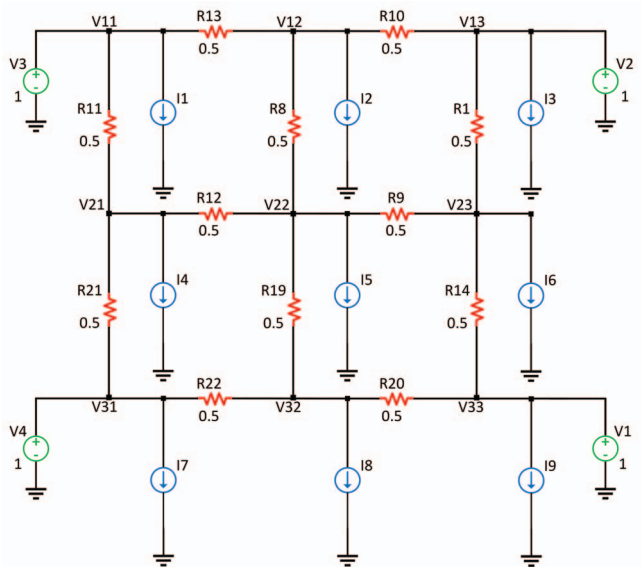


Fig. 5. Conventional power distribution to 9 loads at $V_{Grid} = V_{DD} = 1$V.

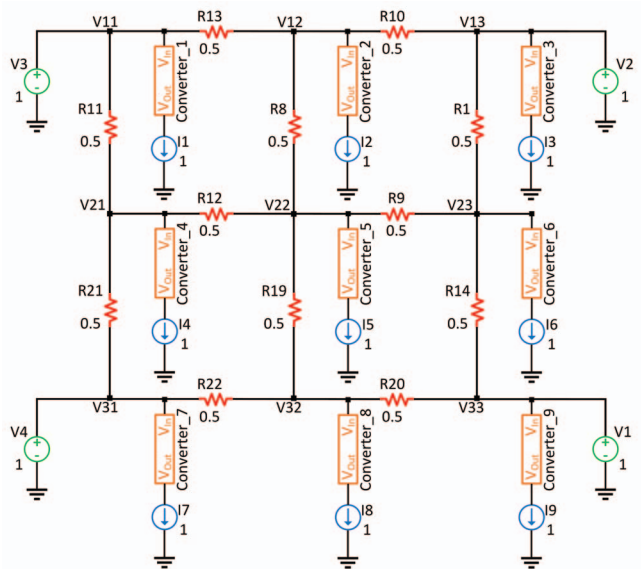


Fig. 6. Proposed high-voltage power distribution to 9 loads at $V_{Grid} = 3$V, $V_{DD} = 1$V.

should give us power reduction of $\frac{1}{\eta^2}$. With non-ideal DC-to-DC converters this power saving will be less. However, with DC-to-DC converters having decent efficiency, we can still expect significant reduction in power loss over the network. In other words, power efficiency of chips will increase vastly. Additionally, the proposed method is also expected to alleviate the following issues with present day on-chip PDN.

*Reduced $IR$ drop:* As current through the network reduces to a fraction of its original value, IR voltage drop across the network would automatically reduce. Moreover, with the DC-to-DC converters adjacent to loads, the overall issue of a load getting the required voltage for optimal performance would probably become negligible. Whatever voltage drop occurs across the nodes, the converter would ensure that a load is fed with optimal supply voltage, e.g., $V_{DD}$ = 1V.

*Reduced Electromigration:* Through reduced current the proposed scheme should also alleviate the electromigration problem in the power distribution network.

*Reduced Signal Delay Uncertainty:* As our scheme reduces $IR$ drop, the signal delay uncertainty should also improve.

*Reduced Noise Margin Degradation:* By reducing $IR$ drop across the network, the proposed scheme should reduce the degradation of noise margins for on-chip signals.

## V. A Simulation Experiment

We use a commercially available DC-to-DC converter to illustrate the proposed scheme. The LTC3411-A is a constant frequency, synchronous step-down DC-DC converter from Linear Technology Corp. [4]. It operates for a 2.5V to 5.5V input voltage range and has a user configurable operating frequency up to 4MHz, allowing the use of tiny, low cost capacitors and inductors, $1mm$ or less in height. The output voltage is adjustable from 0.8V to 5.5V. Internal synchronous power switches provide high efficiency. The LTC3411-A's current mode architecture and external compensation allow the transient response to be optimized over a wide range of loads and output capacitances [4]. The LTC3411-A can be configured for automatic power saving burst mode operation ($I_Q$ = 40$\mu$A) to reduce gate charge losses when the load current drops below a level required for continuous operation. For reduced noise and RF interference, the SYNC/MODE pin can be configured to skip pulses or provide forced continuous operation. To further maximize battery life, the P-channel MOSFET is turned on continuously in dropout (100% duty cycle). In shutdown, the device draws less than 1$\mu$A [4].

We have used the Linear Technology's LTC3411-A converter circuit configured for 1V output voltage at 1A current. We created an LTSPICE module and replicated it at all required locations within the power distribution network.

### A. Experimental Setup

For evaluating the proposed scheme, we simulated three power distribution networks in SPICE and compared the results. We modeled networks with 1, 4, 9, 16, 25, 64, 100 and 256 loads, respectively.

We have used LTSPICE [3], the SPICE simulator from Linear Technology, for all our simulations. We assumed 1 watt loads running at $V_{DD} = 1$V supply voltage and drawing 1A current. We modeled loads as current sources.

For interconnect resistances $Rij$ in Figures 5 and 6, we assumed 0.5$\Omega$ according to ITRS 2012 Datasheet [14]. Also, we assume, interconnect resistivity $\rho$ = $2\times10^{-6}$ $\Omega$-cm, interconnect thickness $T$ = $1\times10^{-6}$ m, interconnect width $W$ = $50\times10^{-6}$ m, and interconnect length $L$ = $5\times10^{-3}$ m. The interconnect resistance $R$ is given by,

$$R = \rho \cdot \frac{L}{T \cdot W} \quad \text{ohms} \tag{5}$$

The first among the three modeled on-chip power distribution networks is a present-day (traditional, $V_{DD}$) grid carrying power at 1V, which is also the $V_{DD}$ (Figure 5). We simulated this network for grid loss and efficiency.

In the second network, power is carried at 3V before being delivered to load at 1V. We have chosen the value 3V as it is close to the terminal voltage of a Lithium Ion battery

TABLE I. POWER CONSUMPTION BREAK DOWN AND EFFICIENCY OF THE TRADITIONAL PDN (DISTRIBUTION VOLTAGE = $V_{DD}$ = 1V).

| Number of loads | Power in Watts | | | Efficiency % |
|---|---|---|---|---|
| | Load | Interconnect | Total | |
| 1 | 1 | 0.13 | 1.13 | 88.50 |
| 4 | 4 | 0.67 | 4.67 | 85.65 |
| 9 | 9 | 1.69 | 10.69 | 84.19 |
| 16 | 16 | 3.57 | 19.57 | 81.76 |
| 25 | 25 | 7.02 | 32.02 | 78.08 |
| 64 | 64 | 23.76 | 87.76 | 72.93 |
| 100 | 100 | 49.32 | 149.32 | 66.97 |
| 256 | 256 | 169.4 | 425.4 | 60.18 |

TABLE II. POWER CONSUMPTION BREAK DOWN AND EFFICIENCY OF THE HIGH-VOLTAGE PDN (DISTRIBUTION VOLTAGE = 3V) WITH IDEAL (ASSUMED LOSSLESS) CONVERTERS.

| Number of loads | Power in Watts | | | Efficiency % |
|---|---|---|---|---|
| | Load | Interconnect | Total | |
| 1 | 1 | 0.01 | 1.01 | 98.58 |
| 4 | 4 | 0.07 | 4.07 | 98.17 |
| 9 | 9 | 0.19 | 9.19 | 97.96 |
| 16 | 16 | 0.40 | 16.40 | 97.58 |
| 25 | 25 | 0.78 | 25.78 | 96.97 |
| 64 | 64 | 2.64 | 66.64 | 96.04 |
| 100 | 100 | 5.48 | 105.48 | 94.80 |
| 256 | 256 | 18.82 | 274.82 | 93.15 |

operating at 90% efficiency. At each load point a DC-to-DC converter steps down the voltage to 1V and feeds it to the loads (Figure 6). However, we assume the converters have 100% efficiency and do not consume any power.

In the third network also power is distributed at 3V and at each load point a DC-to-DC converter steps down the voltage to $1V$ before feeding to the load (Figure 6). However, now we consider the converter's actual efficiency in calculation.

### B. Results and Analysis

In the regular (traditional, $V_{DD}$) power distribution network (PDN), for a single load when load power is 1W and interconnect power is 0.13W, the total power as 1.13W. As network size increases, interconnect power grows rapidly becoming a larger component of the total power. For the 256 load network, load power is 256W, and interconnect power becomes 169.4W (Table I), making the total power as 425.4W.

Also, as the component of interconnect power increases with network size, efficiency of the circuit decreases significantly. For single load, the system efficiency is 88.50%. However, for the 256 load network it drops to 60.18% (Table I), which may not seem too desirable from a system perspective.

*1) High-Voltage On-Chip Power Distribution Network (PDN) Considering Ideal DC-to-DC Converters:* In the high-voltage distribution network with ideal DC-to-DC converters, interconnect power grows rather slowly wth network size. Even for large networks total power is not affected that much. For the 1-load network, load power is 1W, interconnect power is 0.01W and so the total power is 1.01W. Even for large network sizes grid power loss remains small. For the 256 load network, load power is again 256W and the interconnect power is only 18.82W (Table II), making up a total power of 274.82W.

TABLE III. POWER CONSUMPTION AND EFFICIENCY OF THE HIGH-VOLTAGE PDN (DISTRIBUTION VOLTAGE = 3V) WITH NON-IDEAL (LOSSY) CONVERTERS.

| Number of loads | Power in Watts | | | Efficiency % |
|---|---|---|---|---|
| | Load | Interconnect | Total | |
| 1 | 1 | 0.02 | 1.02 | 98.04 |
| 4 | 4 | 0.11 | 4.11 | 97.32 |
| 9 | 9 | 0.39 | 9.39 | 95.85 |
| 16 | 16 | 1.21 | 17.21 | 92.97 |
| 25 | 25 | 2.68 | 27.68 | 90.32 |
| 64 | 64 | 9.12 | 73.12 | 87.53 |
| 100 | 100 | 18.97 | 118.97 | 84.05 |
| 256 | 256 | 63.3 | 319.3 | 80.18 |

As interconnect power starts small and does not grow much, comparatively speaking; system efficiency is high in this case and remains high even for very large networks. The system efficiency for 1 load in the high-voltage distribution system, considering ideal converters, is 98.58%. But most importantly, even for a huge circuit with 256 loads, the simulated efficiency is still 93.15% (Table II).

*2) High-Voltage On-Chip Power Distribution Network (PDN) Considering Non-Ideal DC-to-DC Converters:* The actual efficiency of DC-to-DC converters increases the power consumed in the grid. Even then, interconnect power increases only from 0.02W for single load to 63.3W (Table III) for 256 loads. This is an excellent result as it keeps total power consumed in the 256 load SoC relatively low at 319.3W.

A similar trend is seen in efficiency. The system efficiency for the 1-load network is 98.04% and for the 256 load network it becomes 80.18% (Table III), which is again a good performance for such a huge circuit with readily available technology; it could be better if converter technology improves.

## VI. CONCLUSION AND DISCUSSION

First, we verify Equation 4 that relates the grid voltage and efficiency of a fixed size power grid. From Table I, for 256 1W loads and a distribution voltage $V_{DD} = 1$V, the load power is 256W, grid power loss is 169.4 and efficiency is 60.18%. According to Equation 4, if we increase the distribution voltage to 3V, i.e., $n = 3$, then the grid power loss should come down to $\frac{169.4}{3^2}$ = 18.82W. The efficiency should increase to $\frac{256}{256+\frac{169.4}{3^2}} \times 100$ = 93.15%. From Table III we can see that for a distribution voltage of 3V with ideal converters, indeed grid power loss comes down to 18.82W and efficiency increases to 93.15%. Thus, the relationship established in Equation 4 is verified to be correct. Finally, in order to get a better idea about distribution voltage and efficiency of a grid, we use Equation 4 and Table I to plot efficiencies of 64, 100 and 256 load grids for distribution voltages of 1V, 2V, 3V, 4V and 5V (Figure 7).

Simulations show that interconnect power and its contribution to the total power consumption of a system increases as the network grows. However, while the rate of this increase is rather high in a traditional PDN, it remains low in case of high-voltage PDN considering ideal DC-to-DC converters. Even if we consider the efficiency of the DC-to-DC converters, interconnect power loss grows significantly slower in the proposed scheme.

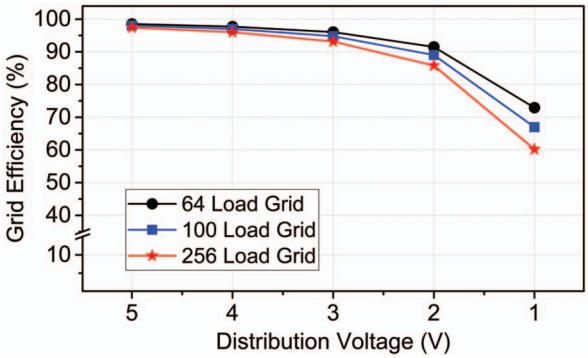


Fig. 7. PDN (grid) efficiency versus distribution voltage $V_{Grid}$ for 64, 100, and 256 load SoCs. $V_{DD} = 1$V.

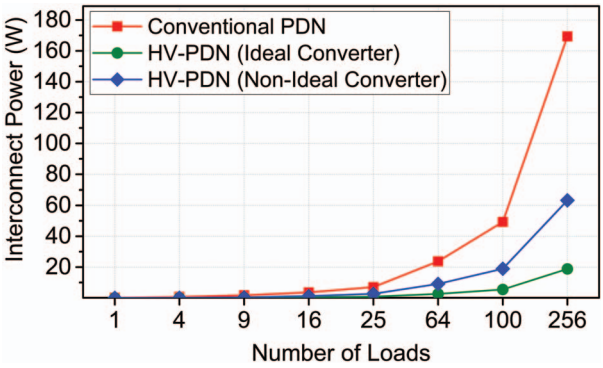


Fig. 8. Grid power loss when power distributed to SoC at 1V (red), 3V with ideal converters (green), and 3V with lossy converters (blue). 1W per load, $V_{DD} = 1$V.

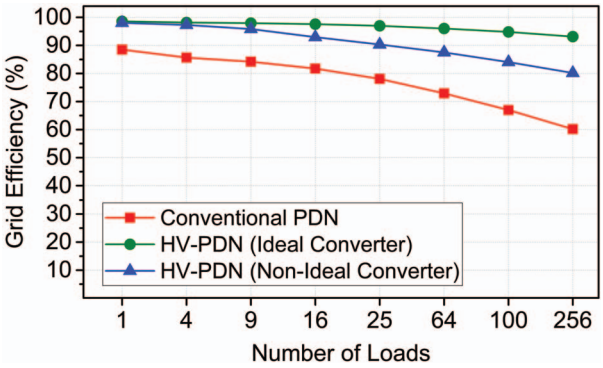


Fig. 9. PDN (grid) efficiency for an SoC ($V_{DD} = 1$V) when power is distributed at 1V (red), 3V with ideal converters (green), and 3V with non-ideal converter (blue).

For distribution at $V_{DD}$, the grid loss is 0.13W for the single-load system but 169.40W for 256-loads. Distributing at 3V with ideal converters, the grid loss for 1 load is 0.01W and for 256 loads it rises only to 18.82W. Adding the converter power loss, the grid loss increases to 0.02W for 1 load and to 63.3W for 256 loads (Figure 8).

Due to interconnect power growing rapidly with increasing grid size, the present day $V_{DD}$ distribution becomes inefficient for large systems with huge number of cores. In simulation, the efficiency dropped from 88.50% for 1 load to 60.18% for 256 loads. However, in case of high-voltage distribution system with ideal DC-to-DC converters, the efficiency is much higher and remains almost the same regardless of network size. For 1 load it is 98.58% and for 256 loads its 93.15%. Even when the efficiency of converters is considered, the grid efficiency is still 80.18% for 256 loads (Figure 9).

From the above discussion, we can reasonably concur that, power distribution at $V_{DD}$ will become inefficient for large SoCs in the future. This in turn validates the need for the proposed methodology. However, its implementation will require efficient DC-to-DC converters that can be effectively integrated on the SoC. Suitable designs of converters are needed. Figure 7 shows that the energy efficiency of power distribution approaches 100% as the grid voltage increases. Future research may explore upper bounds on the distribution voltage based on materials breakdown. Also, PDN optimization algorithms for higher voltage distribution will be worth investigating [5].

***Acknowledgment:*** Authors are grateful for support of this research from Intel Corporation through a gift.

## REFERENCES

[1] "American Electric Power Transmission Facts." http://bit.ly/11nUMvf; accessed on July 01, 2013.

[2] "Electric Power Transmission." [http://bit.ly/15ar90; accessed on July 01, 2013].

[3] "Linear Technology Corp.." http://www.linear.com/company/; accessed on April 17, 2013.

[4] "Linear Technology: LT3411A DC-DC Converter Demo Circuit," Nov. 2011.

[5] S. Dash, *Novel Metaheuristics for the Performance Analysis and the Design Optimization of VLSI Circuits*. PhD thesis, Indian Institute of Technology Guwahati, Guwahati, India, 2018. in preparation.

[6] R. W. Erickson, *DC-DC Power Converters*. John Wiley and Sons, Inc.

[7] R. Jakushokas, *Power Distribution Networks with On-Chip Decoupling Capacitors*. Springer, 2011.

[8] M. Keating, D. Flynn, R. Aitken, A. Gibbons, and K. Shi, *Low Power Methodology Manual for System-on-Chip design*. Springer, 2007.

[9] V. Kursun and E. G. Friedman, *Multi-Voltage CMOS Circuit Design*. Wiley, 2006.

[10] Y.-M. Lee and C.-T. Ho, "InTraSim: Incremental Transient Simulation of Power Grids," *IEEE Trans. CAD of ICs and Sys.*, vol. 36, no. 12, pp. 2044–2051, Dec. 2017.

[11] A. Mezhiba and E. G. Friedman, *Power Distribution Networks in High Speed Integrated Circuits*. Springer, 2012.

[12] M. Popovich, E. G. Friedman, M. Sotman, and A. Kolodny, "On-Chip Power Distribution Grids with Multiple Supply Voltages for High-Performance Integrated Circuits," *IEEE Transactions on VLSI Systems*, vol. 16, no. 7, pp. 908–921, 2008.

[13] S. S. Sapatnekar and H. Su, "Analysis and Optimization of Power Grids," *IEEE Design & Test of Computers*, vol. 20-3, pp. 7–15, 2003.

[14] Semiconductor Industry Association, "International Technology Roadmap for Semiconductors," 2012. http://www.itrs.net/Links/2012ITRS/Home2012.htm.

[15] M. M. Shihab, "A High-Voltage On-Chip Power Distribution Network," Master's thesis, Auburn University, Auburn, AL, June 2013.

[16] K. Wang and M. Marek-Sadowska, "On-Chip Power-Supply Network Optimization using Multigrid-Based Technique," *IEEE Trans. CAD of ICs and Sys.*, vol. 24, no. 3, pp. 407–417, 2005.