Power Problems in VLSI Circuit Testing*

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Abstract. Controlling or reducing power consumption during test and reducing test time are conflicting goals. Weighted random patterns (WRP) and transition density patterns (TDP) can be effectively deployed to reduce test length with higher fault coverage in scan-BIST circuits. New test pattern generators (TPG) are proposed to generate weighted random patterns and controlled transition density patterns to facilitate efficient scan-BIST implementations. We achieve reduction in test application time without sacrificing fault coverage while maintaining any given test power constrain by dynamically adapting the scan clock, accomplished by a built-in hardware monitor of transition density in the scan register.

Keywords: Test power, test time, transition density, weighted random patterns, built-in self-test, scan testing.

1 Introduction

Controlling power dissipation in large circuits during test is a major concern in the VLSI industry. High power dissipation occurs during test because, unlike the normal mode operation of the system, correlations between consecutive test patterns do not exist in the test mode [6, 7]. To increase the correlation between consecutive vectors during testing, several techniques have been proposed for creating low transition density in pattern sets and thus control the power dissipation. However, this in turn increases the test application time as the test has to run for longer time to reach sufficient fault coverage. Increase in test time is also undesirable.

In this work we show that by properly selecting the characteristics of either weighted random patterns (WRP) or transition density patterns (TDP) for a given circuit we can reduce the test time that is proportional to the number of vectors. In some cases, we may also get higher fault coverage because many

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random-pattern resistant faults become detectable by WRP or TDP. Section 3 describes experiments run on the ISCAS89 benchmark circuits and compares the test lengths to reach certain fault coverage for weighted random patterns and transition density patterns against the conventional "purely" random patterns.

New test pattern generators (TPG) proposed in Section 4 produce vectors with desired weights or transition densities. Section 5 shows that the test time can be further reduced while maintaining any given power constrain by using a dynamically adaptive scan clock [15, 16]. Section 6 reports simulation results.

2 Background

Weighted random patterns have been used before to reduce test length for combinational circuits [1–3, 8]. Proper selection of the input probability can increase the efficiency of test vectors in detecting faults, resulting in reduced test time [10]. Therefore, to achieve higher fault coverage with shorter test lengths weighted pseudo random patterns are used [5].

Weighted random patterns (WRP) in which the probability of 1, $p1$, instead of being 0.5, can be set to any value in the range [0, 1] have certain advantages. Recent papers discuss low power test using weighted random and other reduced activity patterns. The power dissipation of scan patterns is related to the transitions they produce in the scan register. It is reported that with reduced activity patterns the fault coverage rises slowly and for the same required coverage a larger number of patterns are needed. Thus, a reduced power test may take longer time.

Much work has been reported on the generation and application of WRP in BIST and random testing since the 70s. We cite only a few references here [8, 10]. The primary purpose of WRP is to increase the rate of fault detection and reduce the test time. They are also known to reduce power consumption [22].

Transition density patterns (TDP) are primarily used for reducing power consumption during test [12, 20]. Their potential for enhancing the fault coverage, the main topic this paper, has not been explored before. Transition density for a signal or a circuit was originally defined for estimating the dynamic power as the number of signal transitions per unit time [11].

We consider built-in self-test of full-scan circuits. A hardware test pattern generator (TPG) feeds bits serially into the scan chain. A test controller switches between test and normal modes to perform test-per-scan of the combinational logic as scan-out response bits are sent serially to a signature analyzer (SA). Typical TPGs use a linear feedback shift register (LFSR) or cellular automata (CA) to generate equiprobable 0s and 1s [19].

In scan BIST when the circuit is clocked in the scan mode, the shifting of pattern in the scan register produces transitions that cause power consumption in flip-flops and the combinational circuit. We can call them source transitions. The number of source transitions per clock is the total number of transitions in the bit-stream held in the scan register. As the scan register is loaded during scan-in, the probability of transitions in the incoming bit-stream determines

the average number of transitions that the register will contain. The scanned-in pattern is applied to the combinational logic during normal mode of a test-per-scan process. We do not consider the activity caused by the capture bits on which the scan-in does not have a direct control. Thus, the probability of transitions in the scan-in bits defines the transition density patterns (TDP).

3 Fault Coverage of WRP and TDP

We experimentally examine the fault coverage capabilities of weighted random patterns and transition density patterns.

3.1 Weighted Random Patterns

A Matlab program was written to construct different test vector sets. Each set contained 10,000 vectors but with different weights. Here, the weight is defined as the probability $p1$ of a bit being 1 in a vector. The weights are varied from 0.1 to 0.95 at 0.05 intervals. Thus, 18 sets of vectors are constructed for the weights 0.1, 0.15, 0.2, etc., up to 0.95.

Target fault coverage was set at 95% of the total faults and fault simulation was done using the 18 vector sets mentioned above. The number of vectors needed to reach the target fault coverage by each vector set was recorded. For every circuit that was simulated there exists one specific weight that resulted in the shortest test length. The number of vectors obtained in this experiment for s1269 circuit as a function of the weight (probability of 1 in the scan-in bits) is shown in Figure 1. For this circuit the minimum vectors required for achieving the 95% target fault coverage is 22, obtained for weight $p1 = 0.6$.

3.2 Computing Best Case Transition Density from Best Case Weight

The transition density of the best case weighted random patterns can be estimated. The transition density in an uncorrelated-bit sequence that has a 0 probability of $p0$ and 1 probability of $p1$ is given by $p0p1 + p1p0$ since a transition occurs when a 1 follows a 0 or a 0 follows a 1. However, $p0 = 1 - p1$, thus, the transition density can be calculated as:

$$TD = (1 - p1)p1 + p1(1 - p1) = 2p1(1 - p1) \tag{1}$$

Hence, from Figure 1, for circuit s1269, if best case weighted random pattern has a 1-bit probability of 0.6 then the corresponding transition density will be $2 \times 0.6 \times 0.4 = 0.48$.

This implies that if a test vector set is constructed to have a transition density of 0.48, then that vector set will generate an effective test for the circuit with shortest test length. In other words it can be assumed that a vector set of average transition density of 0.48 will result in detecting more faults with fewer vectors when compared to the numbers of vectors applied with transition densities higher or lower than 0.48.

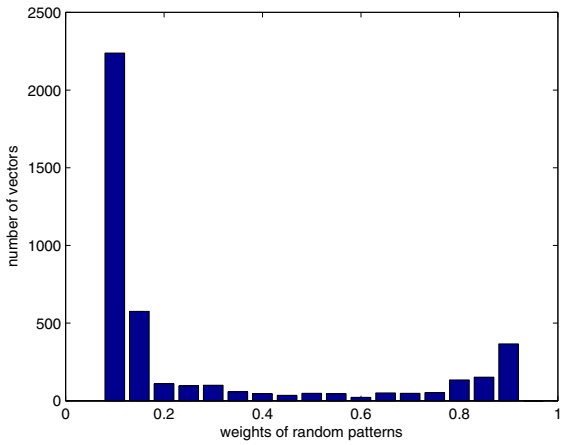

Fig. 1. Number of test-per-scan vectors for 95% coverage in s1269 when 1-probability ($p1$) of scan-in bits was weighted

3.3 Transition Density Patterns

If bits are generated randomly, the probabilities of generating a 1 or a 0 are equal, i.e., $p0 = p1 = 0.5$. Hence the transition density of the bit stream is $2 \times p0 \times p1 = 0.5$. To generate a transition density higher or lower than 0.5, bits must be generated with negative or positive correlation, respectively. Therefore, the bit stream will contain shorter runs of consecutive 1s or 0s for a transition density higher than 0.5 and longer runs of consecutive 1s or 0s for a transition density lower than 0.5.

A Matlab program was written to generate test vector sets, each containing 10,000 vectors but with different transition densities. Here also the transition density was varied from 0.1 to 0.95, with 0.05 intervals. The vector set generated for 0.1 transition density has longer runs of 1s and 0s in consecutive bit positions. Likewise the vector set having transition density of 0.95 has very short runs of 1s and 0s in consecutive bit positions.

Target fault coverage was set to 95% of the total faults and then fault simulation was done using these 18 vector sets. In each case the number of vectors needed to reach the target fault coverage was recorded. For every circuit we simulated, there existed a best transition density (TD) that resulted in the shortest test length. Figure 2 shows a bar chart of the number of transition density vectors obtained from fault simulation experiments to reach 95% fault coverage in circuit s1269. A vector set generated with 0.5 transition density has the best fault detecting capability with smallest number (only 24) as compared with the other transition density vector sets.

A set of ISCAS89 benchmark circuits was used for fault simulation with the transition density vector sets and weighted random vector sets. Table 1 shows the best case results obtained from fault simulation using AUSIM [18]. The table shows the numbers of vectors that achieved 95% fault coverage. The third column

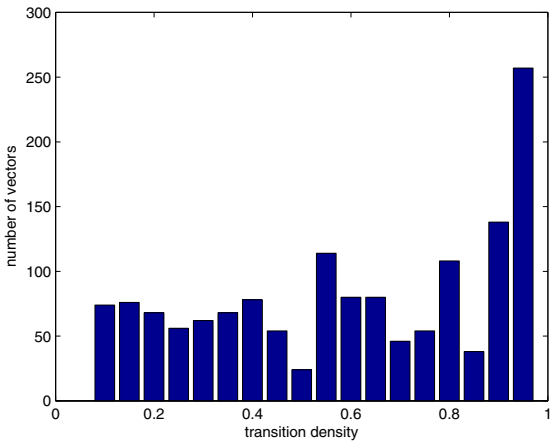

Fig. 2. Number of test-per-scan vectors for 95% coverage in s1269 for various transition densities of scan-in bits

Table 1. Best case weighted random and transition density vectors for 95% fault coverage in ISCAS89 circuits obtained from fault simulation of Matlab-generated patterns. Boldface numbers show the best choice for a circuit

Circuit	Target	Weighted random vectors			Transition density vectors	
name	FC (%)	$p1$	No. of vectors	$TD = 2p1(1-p1)$	Best TD	No. of vectors
s298	77.1	**0.6**	**18**	0.48	0.55	423
s382	95	**0.3**	**56**	0.42	0.45	124
s510	95	**0.4**	**136**	0.48	0.5	152
s635	95	**0.9**	**97**	0.18	0.1	1883
s820	95	**0.45**	**2872**	0.495	0.45	5972
s1196	95	**0.55**	**1706**	0.495	0.45	2821
s1269	95	**0.6**	**22**	0.48	0.5	24
s1494	98.8	0.5	4974	0.5	**0.45**	**3158**
s1512	95	0.75	538	0.375	**0.2**	**338**

gives the weighted random bit probability ($p1$) that required minimum number of vectors shown in column 4. In column 5, the probability $p1$ of column 3 is used to compute transition density from equation 1.

The last two columns of Table 1 give the best case transition density (TD) and the corresponding number of vectors obtained from simulation. The differences in the transition densities of columns 5 and 6 can be because the two were obtained from two different statistical test samples. Also, equation 1, used for computing TD in column 5, assumes uncorrelated neighboring bits, an assumption that is yet to be validated for our transition density vectors.

However, unlike highly efficient weighted random patterns the patterns constructed based on transition density were not able to detect 100% of faults for

some circuits. As shown in Table 1, the weighted random patterns and the transition density based vectors do not always have the same effectiveness. Which is better, often depends upon the circuit. While the generation of weighted random patterns is well understood, transition density patterns need further study.

Note that weighted random bits have a transition density of their own. But our transition density patterns generated by the toggle flip-flop always have equal number of 0s and 1s. Though the transition density of weighted random bits as obtained from equation 1 for any $p1$ can never be higher than 0.5, our transition density patterns generated by a toggle flip-flop (Section 4) can produce transition densities greater than 0.5. Such patterns will produce high power consumption, which can be lowered by the adaptive test clock procedures [15] as discussed in a Section 5, if the vectors gave accelerated fault coverage. This aspect needs additional study.

4 BIST-TPG for Controlled Weight Probability and Transition Density

We propose a new test pattern generator (TPG) for producing vectors of desired weights or transition densities. The illustration in Figure 3 contains a 28-bit external linear feedback shift register (LFSR) using the polynomial $p(x) = x^{28} + x^3 + 1$. The Scan Bit Generator block consists of AND gates, inverters, an 8-to-1 MUX to select from eight different probabilities of a bit being 1, and a toggle flip-flop. A simple finite state machine (FSM) provides the select inputs to the MUX. The Scan Bit Generator produces eight different weighted random bit sequences. The weights are constructed by ANDing two or more outputs from non-adjacent cells of the LFSR.

As shown in Figure 3, any one among eight weights for the probability $p1$ of a bit being 1, i.e., 0.125, 0.25, 0.375, 0.4375, 0.5, 0.625, 0.75 and 0.875, respectively, is selectable by an 8-to-1 MUX. The probability of a bit being 1 or 0 at the output of any cell of the LFSR is 0.5. These are signals W[0] through W[1]. One of these is directly fed to an input of the MUX. Two outputs from two non-adjacent cells were ANDed to produce a weight 0.25, three outputs from three non-adjacent cells are ANDed to produce a weight 0.125, and inverting these two weights we get weights 0.75 and 0.875, respectively. For generating a weight 0.375, the weight 0.75 is again ANDed with another cell output that is not adjacent to any of those two cells that are used in creating the 0.75 weight. Similarly, for generating a weight 0.4375, the weight 0.875 is ANDed with another non-adjacent cell output. Finally, to construct a weight 0.625, the weight 0.375 is inverted. An FSM controls the three select lines of the 8-to-1 MUX to choose any intended probability $p1$ for WRP_bits.

A toggle flip-flop constructed with a D flip-flop and an XOR gate produces bits with transition density $TD = p1$ from the weighted random bits of weight $p1$ as shown in Figure 3. Through the select lines of the MUX, weight $p1$ is selected as the bit sequence fed to one of the inputs of the XOR gate; the other input line of the XOR gate is the output of the D flip-flop. The selected wight

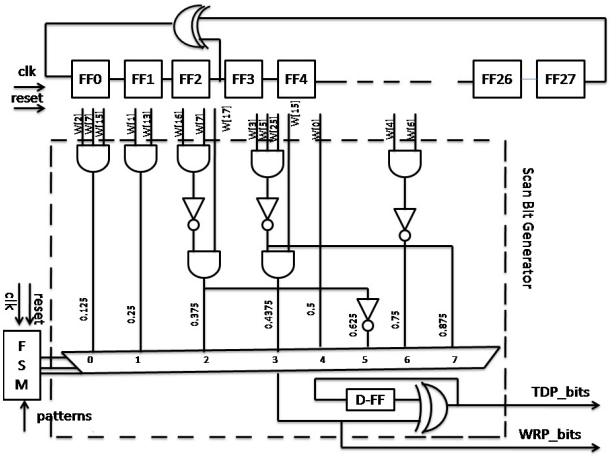

Fig. 3. Test pattern generator (TPG). Equiprobable 0-1 bit outputs, W[0] through W[27], of a 28-bit LFSR are transformed into weighted random pattern (WRP) and transition density pattern (TDP) bits for scan-in.

$p1$ thus controls the transition density at the output of the XOR gate. A 1 in the bit sequence will produce a transition at the output of the XOR gate and a 0 will produce no transition. The resulting TDP_bits at the output of the XOR gate have a probability of a transition to occur, which is same as the weight $p1$ selected from the MUX.

Output WRP_bits or TDP_bits from TPG of Figure 3 feeds the scan chain input of the circuit under test (CUT). For multiple scan chains, the Scan Bit Generator block in TPG is copied multiple times to generate inputs scan_in1, scan_2, etc., for scan chains, as discussed in the next section. The LFSR outputs, {W[i]}, are permuted differently as they are supplied to the duplicated blocks to reduce correlation among the scan chain inputs.

Figure 4 shows that the proposed TPG for WRP and TDP is capable of producing vectors with the desired weight ($p1$) or transition density. The bars in the figure show the numbers of TPG test-per-scan vectors for 95% fault coverage in s1512 as determined by fault simulation. The best cases are 406 TDP vectors for $TD = 0.25$ and 768 WRP vectors for $p1 = 0.75$. These are within statistical variation from the data for s1512 in Table 1, which was obtained by fault simulation of Matlab-generated patterns. The best cases there were 338 TDP vectors for $TD = 0.2$ and 538 WRP vectors for $p1 = 0.75$.

5 Dynamic Control of Scan Clock in BIST Circuit with Modified TPG

Recent work shows that by deploying a dynamic test clock control scheme in scan testing we can reduce test time while maintaining any given peak power limit [14–17]. We extend that technique to multiple scan chains and then use

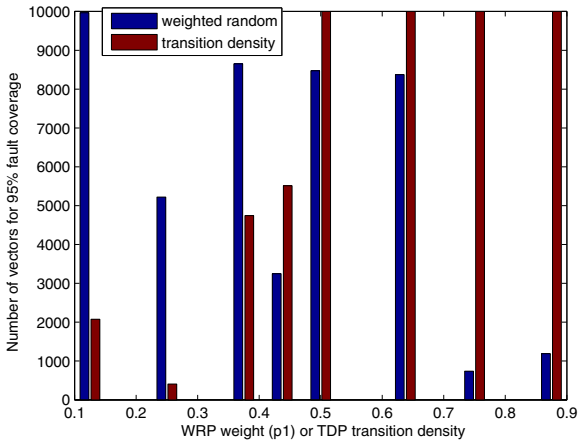

Fig. 4. Performance of transition density and weighted random patterns of s1512

the transition density or weighted random patterns produced by the TPG of the last section. The scheme automatically adjusts the scan clock to keep the test power constrained while reducing the test application time. Our objective is to examine the test time reduction benefits of various types of patterns.

The adaptive scheme of scan clock in scan-BIST consists of a separate inactivity monitor for each scan chain, which keeps track of total inactive bits entering the scan chain as shown in Figure 5. In addition, a frequency divider block provides different frequencies to choose from by a control clock select block. The scanning in of the bits of a test vector starts with the slowest test clock and depending on the number of inactive bits scanned in, the scan clock frequency is gradually increased. We assume that the captured vector produces worst-case activity of 1, that is, the scan chains are filled with alternating 1s and 0s prior to scan-in. We use a TPG with multiple scan bit generator blocks as described in the previous section, along with a finite state machine that selects the weight or transition density from the TPG as shown in Figure 5. The finite state machine (FSM) takes the number of the patterns applied as inputs from the BIST controller and controls the wight or transition density of the test vectors.

The circuit under test (CUT) in Figure 5 has a built-in self-test (BIST) architecture with flip-flops inserted on all primary inputs (PI) and primary outputs (PO). All flip-flops are configured into multiple (e.g., four, as shown in the figure) scan chains of nearly equal lengths [13, 15]. Unlike the Illinois scan [9] where identical bits are broadcast to all chains, this TPG supplies (presumed, though not verified) independent bits, scan_in1 through scan_in4, to CUT, which in the figure has four scan chains. Under the control of a BIST controller once, using the scan mode, all chains are filled with bits from TPG, one normal mode clock cycle captures the circuit response in flip-flops. Then, again using the scan mode

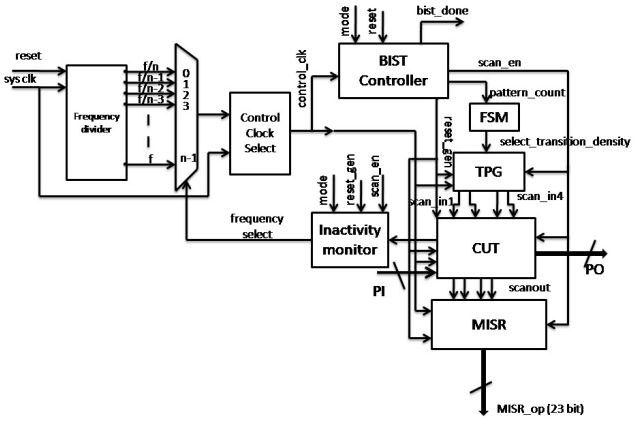

Fig. 5. Adaptive scan clock scheme with modified TPG

as the next pattern is scanned in the captured bits are supplied to a multi-input signature register (MISR) [4, 19]. This completes the application of one test-per-scan vector.

We can pre-determine the best case transition density with the modified TPG and run the whole test session with a pre-selected transition density. Also the circuitry to dynamically adapt the scan clock will help speed up the test clock by monitoring the inactivity and, therefore, keep the whole test session power-constrained. The time reduction in scan-in will be dominated by the largest scan chain and for a transition density TD and the number of frequencies available to adapt from v, the reduction in scan-in time is given by [13, 15],

$$\text{Test time reduction} = \frac{1}{2}(1 - TD) - \frac{1}{2v} \tag{2}$$

6 Experimental Results

Experiments were done on ISCAS89 benchmark circuits. Table 2 shows the comparison between the number of vectors needed to reach 90% fault coverage for each of the circuits. It is to be noted that for each circuit there exists a particular weight or a particular transition density that results in the shortest test length. Consider s13207 circuit with the conventional BIST using a fixed frequency clock. For a 90% target fault coverage, Table 2 gives 4262 random ($p1 = 0.5$) vectors, 2127 WRP ($p1 = 0.35$) and 1490 TDP ($TD = 0.3$). We use the conventional BIST with random vectors as the reference for test time. When the BIST is implemented with TDP, the test time will be reduced by $100 \times (4262 - 1490)/4262 = 65\%$. There will be additional gain with adaptive clock.

So, we examine the reduction in test application time when a dynamic scan clock scheme is used [15]. Results for a selected set of ISCAS89 circuits are given

Table 2. Test lengths for random and best-case weighted random (WRP) and transition density (TDP) patterns for 90% fault coverage in ISCAS89 circuits

Circuit	DFFs	Gates	PIs	POs	Number of vectors for 90% coverage			$p1$ for	TD for
					Random, $p1 = 0.5$	Best WRP	Best TDP	best WRP	best TDP
s27	3	10	4	1	15	5	12	0.15	0.6
s298	14	119	3	6	52	52	> 10000	0.5	0.0
s382	21	158	3	6	42	30	16	0.3	0.4
s386	6	159	7	7	621	317	609	0.35	0.4
s344	15	160	9	11	50	34	> 10000	0.45	0.0
s510	6	211	19	7	70	84	76	0.4	0.5
s420	16	218	18	1	> 10000	300	263	0.9	0.1
s832	5	287	18	19	1380	1126	2128	0.45	0.55
s820	5	289	18	19	962	806	1524	0.45	0.45
s641	19	379	35	24	38	31	41	0.7	0.55
s713	19	393	35	23	109	131	139	0.75	0.55
s967	29	394	16	23	746	268	656	0.4	0.45
s953	29	395	16	23	746	312	458	0.4	0.35
s838	32	446	34	1	> 10000	488	491	0.95	0.15
s1238	18	508	14	14	2506	1759	2598	0.55	0.45
s991	19	519	65	17	34	34	23	0.5	0.75
s1196	18	529	14	14	675	537	712	0.65	0.3
s1269	37	569	18	10	14	10	12	0.6	0.85
s1494	6	647	8	19	460	416	266	0.6	0.4
s1488	6	653	8	19	438	410	247	0.6	0.55
s1423	74	657	17	5	12	6	11	0.85	0.2
s1512	57	780	29	21	46	46	78	0.5	0.6
s13207	669	7951	31	121	4262	2127	1490	0.35	0.3
s15850	597	9772	14	87	2463	2463	3293	0.5	0.3

in Table 3. In each case four scan chains of nearly equal length were inserted using the BIST architecture of Figure 5. Test times for all three types of vectors shown in Table 2 were obtained by simulation.

As an example, consider s13207 again. Since flip-flops are added to primary inputs (PIs) and primary outputs (POs), total scanned flip-flops are $669 + 31 + 121 = 821$. Given there are four nearly equal scan chains, the longest chain has $\lceil 821/4 \rceil = 206$ flip-flops. For fixed frequency test a clock period of 40ns is assumed. This is generally specified on the basis of the maximum energy consumption by a vector and the power dissipation capability of the circuit. Test time for 4262 random vectors is calculated as [4],

$$\text{Test time} = (207 \times 4262 + 206) \times 40\text{ns} = 35.3\text{ms} \tag{3}$$

Similarly, the test time for 2127 WRP vectors is 17.6ms and that for 1490 TDP vectors is 12.3ms. For this circuit, the shortest vector set is for TDP, which reduces the test time to $100 \times (35.3 - 12.3)/35.3 = 0.65\%$ of the random vector test time.

For the adaptive scheme, we use four clocks ($v = 4$) of periods 40ns, 30ns, 20ns and 10ns. Assuming the worst case activity from the captured bits, we begin each scan with the slowest clock of 40ns, which is sped up by the activity monitoring circuitry. Test times for the three types of vectors were obtained by simulation of the BIST circuit as 31.6ms, 16.2ms and 10.2ms, respectively, as shown in Table 3. When we compare the adaptive clock BIST with the best transition

Table 3. Comparing test times for 90% coverage by conventional random (R), weighted random (WRP) and transition density (TDP) patterns when adaptive scan clock is used

Circuit	Types of patterns				
	Random (R), $p1 = 0.5$	Weighted random (WRP)		Transition density (TDP)	
	test time (ns)	Best $p1$	Test time (ns)	Best TD	Test time (ns)
s298	10050	0.5	10050	0.5	1974026
s382	10320	0.3	6661	0.4	8287
s510	18200	0.4	19570	0.4	19852
s820	348392	0.4	268971	0.4	504453
s953	418073	0.4	162371	0.3	231833
s1196	264652	0.6	221416	0.3	262350
s1488	124572	0.6	117901	0.5	72831
s13207	31565011	0.35	16180025	0.3	10149712
s15850	16341260	0.5	16341260	0.3	20109065

density patterns and the conventional fixed clock random pattern BIST, the test time reduction is $100 \times (35.3 - 10.2)/35.3 = 71\%$.

Once again, time reduction is measured as the time required for the vectors to be scanned-in using fixed scan clock minus the time required for the vectors to be scanned-in using the variable scan-clock. We see a significant reductions in test application time in s13207 and s1488 as the best case transition density vectors were applied along with the dynamic adaptive scan clock scheme.

7 Conclusion

For scan-BIST testing it is important to note that both power and test time contribute to the test cost as well as quality of the test. Transition density can be effectively selected for any circuit analogous to weighted random patterns to generate test session with shorter test length. Table 2 shows that for certain circuits, 90% fault coverage can be achieved with a minimal number of vectors if transition density patterns are used. Once the transition density is known the test application time can be further reduced by dynamically controlling the test clock keeping the test power under control as shown in Table 3. Thus, this work contributes towards generating high quality tests with reduced test application time and keeping the test power constrained.

Renewed interest in low power test patterns [12, 20, 21] has shown applications of low toggle rate vectors for reducing test power. Low toggle rate is often associated with slow rise in fault coverage. In this paper, we show that this is not necessarily true when the toggle rate (or transition density) is suitably determined for the circuit under test. Even higher toggle rates can be used when they provide quicker fault coverage because power consumption can be constrained by an adaptive scan clock, thus reducing the overall test time on balance.

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