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Enhancing Random Access Scan for Soft Error Tolerance

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Abstract – Recent work on random access scan (RAS) has shown its advantages in reducing test application time, test data volume and test power over those of the conventional serial scan (SS). This paper is first to examine the soft error tolerance of RAS. The RAS structure not only improves error tolerance ability during test, it also provides capability to efficiently enhance the circuits error tolerance during normal function mode. A single event upset (SEU) induced error in a flip-flop of SS propagates to other flip-flops via scan while the error for RAS remains localized to the affected flip-flop. We enhance the error tolerance by applying the built-in soft error resilience (BISER) and triple modular redundancy (TMR) techniques to RAS and serial scan (SS). Results show that the BISER implementation for RAS can save on average 20.51% hardware over BISER applied to SS. TMR-RAS saves on average 179.28% over TMR-SS for ISCAS89 benchmarks.

I. Introduction

A variety of improvements in electronic system reliability have been studied to keep pace with innovative and cutting-edge technologies. Around 1950, theories of fault tolerant and self-repairing computing systems were developed in response to the increased reliability requirements of critical applications like space missions. STAR (Self Testing and Repairing) computer, a 1970s project funded by NASA and JPL employed several fault tolerant computing techniques targeting an over 10 year life cycle is a good example [3]. The International Technology Roadmap for Semiconductors (ITRS) predicts continuous downscaling of the transistor size, threshold voltage and oxide thickness to meet the high performance computing requirement. This will increase clock frequencies to multiple gigahertz range, drop load capacitances of circuit nodes to femtofarads, and decrease supply voltages below one volt. These trends are posing new challenges to electronics reliability. Well-known error sources in electronic systems include noisy power supply, lightning and electrostatic discharge (ESD), ground bounce, and interconnect coupling capacitances. In addition, there are soft errors, which are caused when charged particles striking the sensitive regions of silicon devices. They used to be one of the major concerns for avionics and space mission applications during the past decades, but have become critical reliability threats for ground-based electronic systems. With advances in the design and manufacturing technologies, the soft errors induced by cosmic rays and alpha particles will remain the prevalent reliability concerns [16].

Scan design is the backbone for modern VLSI chip testing and manufacturing. Scan provides very high controllability and observability in complex VLSI chips. In serial scan (SS) flip-flops are accessed in the test mode through a serial shift register. It is the most widely used technique in the chip industry. But its drawbacks of high test time and power consumption increase dramatically with increased number of flip-flops. Random access scan (RAS) places flip-flops in a fashion similar to a random access memory (RAM) so that any flip-flop can be readily written to or its content is retrieved [1], [2], [6], [11]. RAS gives an orthogonal solution that drastically reduces the test power and test time, simultaneously, with some moderate cost in hardware overhead. In [1], average 60% reduction in write test data volume compared with conventional RAS design is achieved, using a proposed cluster based techniques.

A unique advantage of RAS, however, is a natural soft error tolerance capability provided by its routing structure. To our knowledge, this feature has never been mentioned in the literature. In this paper, we conduct a comprehensive soft error tolerance analysis of RAS design and propose two enhanced error tolerance designs. In Section 2, we summarize the soft error tolerance techniques and the basic concepts of RAS. In Section 3, soft error tolerance is analyzed for RAS and serial scan (SS) to demonstrate the error tolerance advantages of RAS. In Section 4, we apply space redundancy to the RAS structure to enhance the soft error tolerance using built-in soft error resilience (BISER) and TMR techniques. Hardware overheads are compared. A summary and conclusion are given in Section 5.

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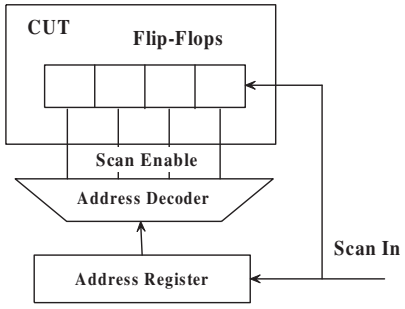


Fig. 1. Basic RAS structure.

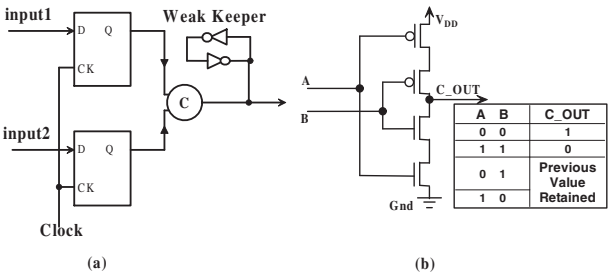


Fig. 2. (a) BISER design and (b) c-element.

II. Background

Error tolerant computing techniques are characterized by the level of reliability they provide and their costs in area and performance.

- Device-level error tolerance techniques either increase the device critical charge (minimum charge to induce an error [16]) or decrease the collected charge to reduce SER. Additional isolation to reduce the amount of charge collected by creating potential barriers is possible [5].
- Circuit or system level error tolerance techniques include error detection and correction (EDAC) codes and time or space redundancy [8], [13]. Additional system-level error tolerance techniques include rewriting and instruction re-issue when an error is detected [9]. Reuse of scan flip-flops for timing redundancy to reduce the SER of combinational logic with minimal area overhead has been proposed [7].

The built-in soft error resilience (BISER) technique corrects radiation-induced soft errors in latches and flip-flops [10], [19]. Proposed error-correcting latch and flip-flop designs are power efficient, can correct both flip-flop errors and combinational logic errors, and reuse the on-chip scan design-for-testability hardware for circuit-level error recovery. The BISER flip-flop consists of duplication of flip-flops, a c-element and a weak-keeper. If the outputs of two flip-flops are different, the c-element retains its previous value. The weak-keeper improves the error tolerance. A diagram of BISER and the truth table

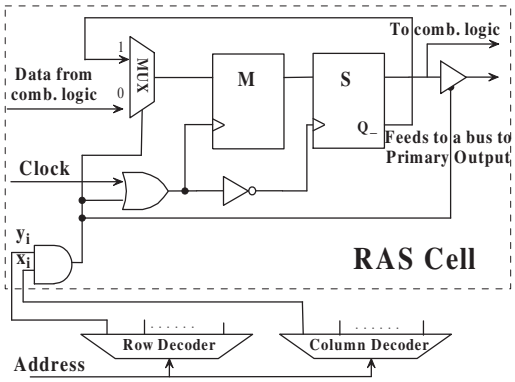


Fig. 3. A RAS cell with toggle mechanism.

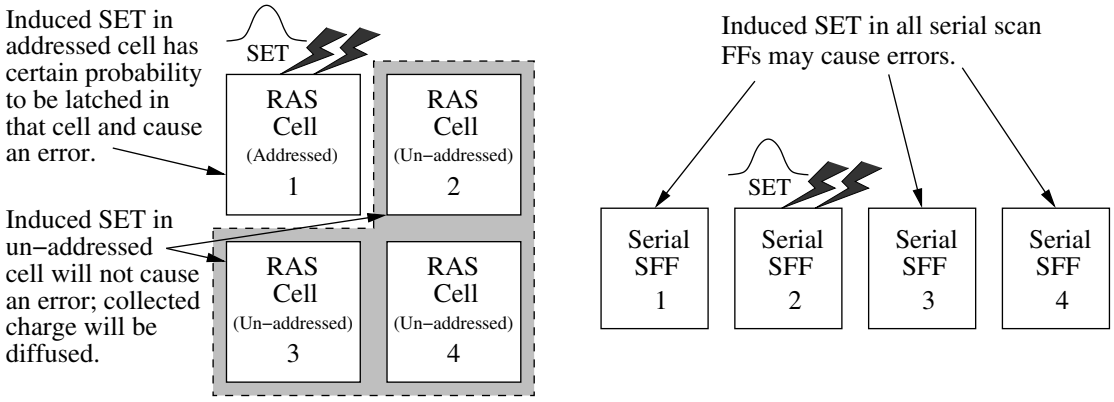
of c-element are shown in Figure 2. In this paper, we will use BISER to enhance the RAS reliability.

Soft errors in logic circuits are often filtered out by the circuit itself and may not affect the performance. This occurs through logic masking, electrical masking or temporal masking [12], [18]. The influence of complex topology of a logic circuit on SER makes it different from a RAM that has a regular cell structure.

A. Random Access Scan (RAS)

In serial scan (SS), long scan-in and scan-out paths are seamless chains that form shift registers. This increases the test time and the unnecessary circuit activity makes the power consumption unacceptable for very large multi-million-flip-flop chips. Slowing down the clock may solve the power consumption problem but will increase test time, which is undesirable. Random Access Scan, an alternate scan architecture is worth examining because it addresses the test time and power dissipation problems. Basic RAS structure is shown in Figure 1. It consists of an address register, an address decoder and the scan-in signal. RAS allows reading or writing of any flip-flop. The address decoder produces a scan enable signal for the flip-flop (FF) that is to be updated. Unlike conventional serial scan, RAS does not work with shift registers. The address signals enable the access to only one FF in the circuit, thus test time and power dissipation are significantly reduced. The operation of RAS, similar to writing and reading a random access memory (RAM) cell, significantly reduces the time of loading and observing a flip-flop but requires moderate overheads both in gates and test pins. A decoder is used in RAS to address every FF hence at any time only one FF is activated while all other FFs simply hold their states [2], [11]. The scan-in signal and a unique test control signal are broadcast to all FFs. The output from FF either propagates into a multiple input signature register (MISR) or to a primary output.

A recently proposed RAS design has lower hardware overhead [11]. This toggle-RAS design is illustrated in



(A) Random access scan (RAS). (B) Serial scan (SS).

Fig. 4. Soft error tolerance analysis of (A) RAS and (B) SS.

TABLE I. RAS control signals.

Data function	Clock	Address decoder outputs	
		Row(x)	Row(y)
Normal	active	0	0
Toggle	inactive	1	active clock
	inactive	active clock	1
Hold	inactive	1	0
	inactive	0	1
	inactive	0	0

Figure 3 and its key signals are described in Table I. This RAS FF has three operations, i.e., capture the response of the circuit in the normal mode, or toggle the current state of the FF being addressed, or retrieve the FF content to the output in test mode. When a RAS FF is not addressed, it continues to hold the previous value. In Figure 3, each RAS FF is fed by two signals, one from row (x) line and the other from column (y) line. In the normal mode the output of every AND gate is "0", which enables clock through OR gate and routes data from the combinational logic through the MUX to be captured in the FF. In the test mode, the clock is stopped and the row and column decoders select only one FF which has logic "1" on both x and y lines. The MUX now takes the inverted content of the FF. Thus, the addressed FF toggles while all unaddressed RAS cells hold their previous states. Since the output from the AND gate is "0" for the unaddressed FF, the clock is not activated. In the next section, we examine the toggle-RAS design and illustrate its natural soft error tolerance ability.

III. Soft Error Tolerance of RAS

In RAS operation, only one FF is addressed and its content toggled, while all other unaddressed FFs hold their previous values. This architecture has a unique error tolerant nature. Consider a 4-cell example. Figure 4(A) shows a 4-cell RAS structure and Figure 4(B) shows serial scan (SS). For clarity, the figure does not show the address decoder and signal routing. We neglect the soft errors occurring in the combinational logic and focus only on those in sequential parts. Assume that the particles coming from radiation sources and striking the circuit's surface have a flux rate of $N \cdot cm^{-2} \cdot s^{-1}$, the probability of flipping the value stored in FF per strike is P, and the sensitive area per FF is A. The sensitive area is the region affected by a single event. A sensitive volume is normally determined by the the channel region of an off nMOS transistor or the drain region of an off pMOS transistor in CMOS technology [14], [17]. In Figure 4 (B), all FFs are clocked and activated so the sensitive area for them is approximately $4 \times A$. The MUX and other gates in the scan structure also have certain probability of induced error, but they are not the determining factors for the soft error rate comparison here. In RAS structure, at a time only one cell is activated so the sensitive region area is A.

When a particle strikes the non-addressed RAS FF, charge is collected to form a single event transient (SET). But this transient will not be captured since the clock is disabled, and the charge will be diffused in a short time, approximately, less than 100*ns* for 35*nm* technology [4]. When a RAS FF is selected, each striking particle has probability P to cause a SET pulse. Probability P is determined by the striking particle's energy distribution. Only a high energy particle strike has a chance to collect more than the critical charge to induce a SET. Also, this pulse should occur within a certain interval (window) around the clock edge to be captured into the FF. This "timing window" scenario has been studied in the literature [12], [15]. The temporal derating is proportional to the clock frequency. We define temporal derating as $\alpha \cdot f$, where α is a temporal derating factor and f is clock frequency. By definition, the induced SET has probability $\alpha \cdot f$ of being captured by clock to finally become a soft error.

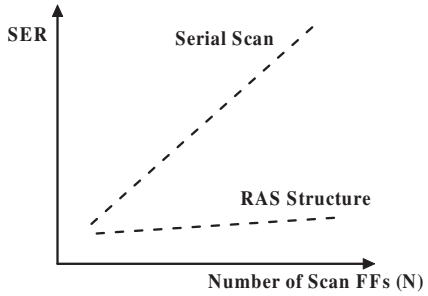


Fig. 5. Predicted SER for RAS and SS without error tolerant technique applied.

Thus, SER for the 4-cell RAS structure is

$$N \cdot (A + \Delta) \cdot P \cdot \alpha \cdot f \quad (1)$$

while the SER for the serial scan structure is

$$4N \cdot A \cdot P \cdot \alpha \cdot f \quad (2)$$

where, *N* is the particle flux in $\#particles \cdot cm^{-2} \cdot s^{-1}$, *A* is sensitive area per FF in cm^2, *P* is probability of SET per strike in a FF, Δ is average area overhead (routing, decoders, etc.) per FF to implement RAS, and αf is a temporal derating factor between 0 and 1 (it is the probability of capturing an induced SET by clock of frequency *f*).

The analysis shows that the SER of serial scan structure will be 4 times that of RAS structure in this 4-FF example where no other fault tolerance techniques is used. For more scan FFs, we can expect the SER of SS to increase much more than that for RAS design because the sensitive area of SS will increase linearly with the size of circuit. This is shown in Figure 5. The SER in RAS structure stays stable with only a slight increase due to the larger hardware overhead of address decoder and output buffers, which will induce more soft errors.

IV. Further Enhancing Error Tolerance

Besides the natural soft error tolerance, the RAS grid architecture offers additional opportunity to enhance soft error tolerance. Suppose the total number of FFs is $n_{ff} = m \times n$ such that a row decoder selects one among m lines and a column decoder selects one among n lines. To minimize the number of address lines, which is $m+n$, the numbers of row and column lines should be equal, i.e., $m = n = \sqrt{n_{ff}}$.

In Figure 6, we apply the 1:1 space redundancy error resilience technique to the RAS grid, which we refer to as BISER-RAS, while the application of BISER [10], [19] to the serial scan structure will be the reference design called BISER-SS. The first column of FFs is added as the redundant copy, the column line Ry feeds into these

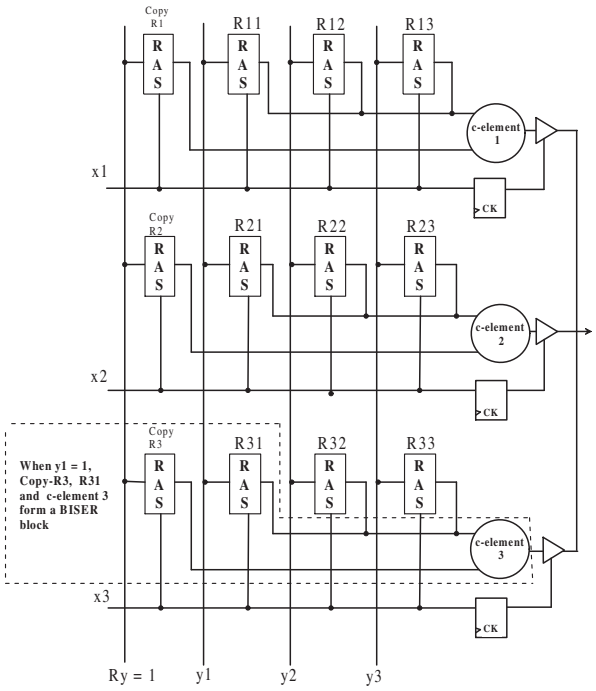


Fig. 6. Proposed fault tolerant design using BISER-RAS.

FFs and is permanently set to "1". The row signal is shared with the other RAS FFs in the same row. There are signals coming from combinational logic (CL_i) and scan-in (SI_i) that feed into each RAS FF. These are not shown in Figure 6.

Signals from combinational logic (CL_i) are routed to FFs in the functional mode. The scan-in signals and combinational logic input signals to functional FFs are encoded as the combinational input and scan-in input, respectively, to the redundant FF. These encoders are also not shown in Figure 6. The encoding scheme ensures that the redundant FF has the same content as the addressed FF either in normal mode or in test mode, so the error tolerance remains effective during the normal function and during test. Combinational input signal to the redundant FF is

$$CL = CL_1 \times y(1) + CL_2 \times y(2) + ...CL_{\sqrt{n_{ff}}} \times y(\sqrt{n_{ff}}) \quad (3)$$

Since there are $\sqrt{n}_{ff}$ functional FFs in the row and only one is selected each time, so only one column signal $y(i)$ is 1, while others are 0. Similarly, scan-in signals of functional FFs are $SI_1, SI_2...$ and the scan-in signal to the redundant FF is

$$SI = SI_1 \times y(1) + SI_2 \times y(2) + ...SI_{\sqrt{n_{ff}}} \times y(\sqrt{n_{ff}}) \quad (4)$$

where $\sqrt{n_{ff}}$ is total number of flip-flops in the row and $y(n)$ is the nth column line.

TABLE II. Comparison of hardware overheads for ISCAS'89 benchmark circuits.

Circuit	No. of FFs	Comb. gates	BISER design overhead (%)			TMR design overhead (%)		
			SS	RAS	Reduction	SS	RAS	Reduction
s208	8	112	87.41	82.41	5.09	283.33	97.14	186.19
s349	11	176	80.77	71.67	9.10	261.54	83.26	178.28
s510	6	211	46.49	46.45	0.04	150.55	55.49	95.06
s641	19	379	70.12	56.92	13.20	227.07	64.58	162.48
s1196	18	529	53.31	43.63	9.68	172.64	49.61	123.02
s1494	6	647	17.82	17.81	0.02	57.71	21.27	36.44
s5378	179	2779	82.27	53.45	28.82	266.40	56.38	210.02
s9234	211	5597	57.49	37.00	20.49	186.17	38.88	147.28
s13207	638	7951	93.49	57.30	36.19	302.73	59.06	243.67
s15850	534	9772	74.21	45.77	28.44	240.29	47.30	192.99
s35932	1728	16065	108.83	64.93	43.90	352.39	66.18	286.21
s38417	1636	22179	89.15	53.25	35.90	288.66	54.30	234.36
s38584	1426	19253	89.36	53.54	35.82	289.34	54.67	234.68
Average			73.14	52.63	20.51	236.83	57.55	179.28

Note that the original "toggle" RAS design [11] is not used in this fault tolerant architecture because the redundant FF is now shared by all FFs in the row. If each time the redundant FF also toggles when we toggle the addressed FF, it will become impossible to keep the values in redundant FF and the addressed cell synchronized. Therefore, the scan-in signal and one more MUX to the "toggle" RAS design are added. The clock gating scheme and cell activating mechanisms are retained in the enhanced BISER-RAS.

The outputs from functional FFs in the same row feed into a shared bus. Because only one FF is activated at a time contention does not occur. The content of bus is captured by a D-FF clocked by normal clock. The outputs of the addressed FF and the redundant FF feed into a two-input c-element of the BISER structure discussed in Section II. The c-element prevents the error by holding its previous value if the two inputs are different. The row address line also feeds a D-FF to drive a tri-state buffer so the output of tri-state can propagate to next stage.

A. Error Tolerance in Function and Test Modes

During the function mode, data from combinational logic is latched by the globally distributed function clock into both the addressed RAS cells, say, $R31$ and the redundant cell $Copy - R3$ when $y(1) = 1$ in Figure 6. In test mode, scan-in data updates the addressed cell and the redundant cell using test clock. Thus, in both cases the redundant RAS cell and addressed cell are synchronized for BISER operation.

B. Hardware Overhead Comparison

A circuit with n_{ff} FFs and n_g combinational gates has in all $n_g + 10 \times n_{ff}$ gates. This assumes that a master-slave flip-flip consists of 10 gates [6]. In the BISER-SS design all FFs are replaced by scan FFs, each with one additional 4-gate MUX. Also, all flip-flops must be duplicated for space redundancy so there will be additional n_{ff} scan flip-flops, each consisting of 14 gates. We also have n_{ff} c-elements and week keepers. Assume that a gate contains 4 transistors, the c-element is a single gate and a weak keeper contains two inverters. For 1:1 redundancy the BISER-SS employs two-input c-element. Thus,

BISER-SS Overhead

$$= \frac{21 \cdot n_{ff}}{n_g + 10 \cdot n_{ff}} \times 100\% \quad (5)$$

In the BISER-RAS design the number of row and column lines both equal $\sqrt{n_{ff}}$. So, there are $\sqrt{n_{ff}}$ c-elements added and one column of redundant FFs for redundancy is inserted. Each RAS FF consists of 2 MUXes, one AOI gate, one tri-state buffer and one edge-triggered FF. So, $20 \times \sqrt{n_{ff}}$ gates are required for redundant RAS FF. The encoder for scan-in and signal from combinational circuit has $2 \times n_{ff}$ additional gates. This number for the signal encoder can be lower if AOI gates are used for implementation. We add $\sqrt{n_{ff}}$ c-elements for BISER cells and$\sqrt{n_{ff}}$ gates to address decoder. Thus,

BISER-RAS Overhead

$$= \frac{22 \cdot \sqrt{n_{ff}} + 12 \cdot n_{ff}}{n_g + 10 \cdot n_{ff}} \times 100\% \quad (6)$$

From equations 5 and 6, whenever $n_{ff} > 6$, BISER-RAS will have less overhead than BISER-SS.

The analysis of hardware overheads for ISCAS'89 benchmarks is shown in Table II columns 4, 5 and 6. For s15850 with 534 FFs and 9772 combinational gates, with full implementation of (1:1) space redundancy in BISER-RAS and BISER-SS, the hardware overheads are 74.21% and 45.77%, respectively, showing a 28.44% reduction for BISER-RAS. Therefore, the proposed BISER-RAS has much smaller hardware overhead than BISER-SS. In addition, the proposed BISER-RAS structure also has better soft error tolerance than BISER-SS due to its

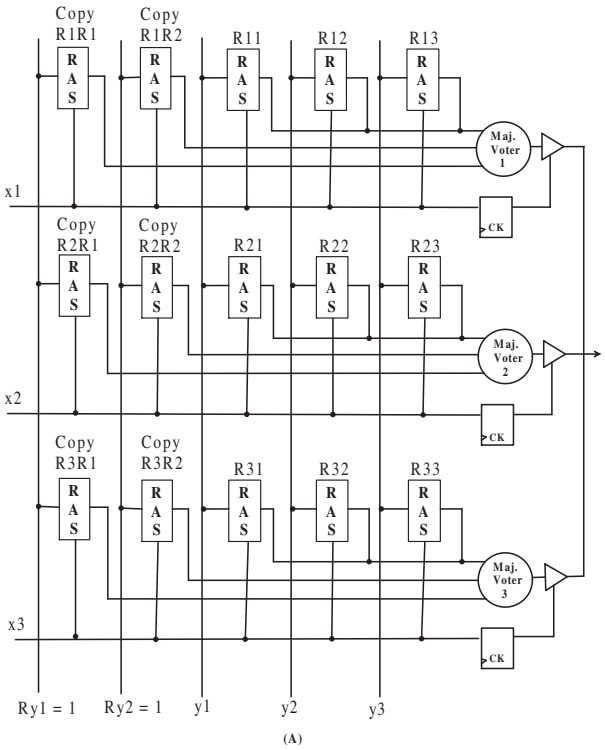


Fig. 7. Proposed fault tolerant TMR RAS.

natural error tolerant capability that was explained in Section III.

In Figure 7, we apply the traditional triple modular redundancy (TMR) to RAS. We call it TMR-RAS while the TMR applied to SS will be called TMR-SS. Two redundant columns of RAS-FFs, first and second columns in Figure 7, are added to the RAS structure for a TMR-RAS design. With additional $2 \times \sqrt{n_{ff}}$ RAS FFs, $\sqrt{n_{ff}}$ majority voters and some overhead in routing and decoder, a full TMR protection scheme is implemented. The hardware overhead is shown in Table II in columns 6, 7 and 8. Observe that TMR-RAS on an average has 179.29% lower overhead than the TMR-SS design.

V. Conclusion

The random access scan (RAS), known to reduce test time, test data volume and power, has a natural soft error tolerance capability that is inherited from its unique memory-like structure and clock gating scheme. In a circuit with n_{ff} FFs, the soft error rate (SER) for RAS can be nearly $1/n_{ff}$ that for serial scan (SS). We study error tolerance schemes using built-in soft error resilience (BISER) and triple modular redundancy (TMR). In both cases, RAS requires less overhead in comparison to similar schemes applied to serial scan. Our future work will include SER simulation experiments to verify the soft error tolerances determined by the present analysis and the robustness and costs of the RAS and serial scan schemes when the hardened flip-flops are implemented.

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References

[1] R. Adiga, A. Gandhi, V. Singh, K. Saluja, H. Fujiwara, and A. Singh, "On Minimization of Test Application Time for RAS," in *Proc. 23rd International Conf. on VLSI Design*, Jan. 2010. Paper A7.3.

[2] H. Ando, "Testing VLSI with Random Access Scan," in *Proc. COMPCON*, 1980, pp. 50–52.

[3] A. Avizienis, G. C. Gilley, F. P. Mathur, D. A. Rennels, J. A. Rohr, and D. K. Rubin, "The STAR (Self-Testing and Repairing) Computer: An Investigation of the Theory and Practice of Fault-Tolerant Computer Design," *IEEE Trans. Computers*, vol. C-20, no. 11, pp. 1312–1321, Nov. 1971.

[4] R. Baumann, "Technology Scaling Trends and Accelerated Testing for Soft Errors in Commercial Silicon Devices," in *Proc. 9th On-Line Testing Symp.*, 2003, pp. 4–6.

[5] D. Burnett, C. Lage, and A. Bormann, "Soft-Error-Rate Improvement in Advanced BiCMOS SRAMs," in *Proc. 31st Annual IEEE Reliability Physics Symp.*, Mar. 1993, pp. 156–160.

[6] M. L. Bushnell and V. D. Agrawal, *Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits*. Boston: Springer, 2000.

[7] P. Elakkumanan, K. Prasad, and R. Sridhar, "Time Redundancy Based Scan Flip-Flop Reuse To Reduce SER Of Combinational Logic," in *Proc. 7th Int. Symp. on Quality Electronic Des.*, 2006, pp. 617–624.

[8] R. Karri and M. Nicolaidis, "Online VLSI Testing," *IEEE Design & Test of Computers*, vol. 15, no. 4, pp. 12–16, 1998.

[9] F. L. Kastensmidt, L. Carro, and R. Reis, *Fault-Tolerance Techniques for SRAM-Based FPGAs*. Spinger, 2006.

[10] S. Mitra, Z. Ming, S. Waqas, N. Seifert, B. Gill, and K. S. Kim, "Combinational Logic Soft Error Correction," in *Proc. International Test Conference*, 2006.

[11] A. S. Mudlapur, V. D. Agrawal, and A. D. Singh, "A random access scans architecture to reduce hardware overhead," in *Proceedings IEEE International Test Conference*, 2005. Paper 15.1.

[12] H. T. Nguyen and Y. Yagil, "A Systematic Approach to SER Estimation and Solutions," in *Proc. 41st Annual IEEE International Reliability Physics Symposium*, 2003, pp. 60–70.

[13] M. Nicolaidis, "Time Redundancy Based Soft-Error Tolerance to Rescue Nanometer Technologies," in *Proc. 17th IEEE VLSI Test Symposium*, 1999, pp. 86–94.

[14] M. Omana, G. Papasso, D. Rossi, and C. Metra, "A Model for Transient Fault Propagation in Combinatorial Logic," in *Proc. 9th IEEE On-Line Testing Symp.*, 2003, pp. 111–115.

[15] N. Seifert and N. Tam, "Timing Vulnerability Factors of Sequentials," *IEEE Trans. Device and Materials Reliability*, vol. 4, no. 3, pp. 516–522, 2004.

[16] F. Wang and V. D. Agrawal, "Single Event Upset: An Embedded Tutorial," in *Proc. 21st Int. Conf. on VLSI Design*, 2008, pp. 429–434.

[17] F. Wang and V. D. Agrawal, "Soft Error Rate Determination for Nanometer CMOS VLSI Circuits," in *Proc. 40th Southeastern Symposium on System Theory*, Mar. 2008, pp. 324–328.

[18] F. Wang and V. D. Agrawal, "Soft Error Rates with Inertial and Logical Masking," in *Proc. 22nd Int. Conf. on VLSI Design*, Jan. 2009, pp. 459–464.

[19] M. Zhang, S. Mitra, T. M. Mak, N. Seifert, N. J. Wang, Q. Shi, K. S. Kim, N. R. Shanbhag, and S. J. Patel, "Sequential Element Design With Built-In Soft Error Resilience," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 14, no. 12, pp. 1368–1378, 2006.