

Fig. 7. Length of a random input sequence to be applied as a function of n and σ (given Q_D). Application to TTL integrated circuits.

responding to 0.1 s) is for the arithmetic logic unit SN74 181, noted by 181, with $n = 14$, $\sigma = 1$.

2) $\sigma/2^n$ is the probability of detecting the most difficult fault by one input vector. The length L is a function of this ratio. So it becomes reasonable to use random testing for large circuits if they have a great σ (we believe it is often true). The multiplexer, noted by 150, has 21 inputs. It is testable in less than 1 ms thanks to a great $\sigma = 2^{14}$.

3) The deciding factor in determining if random testing is shorter than exhaustive testing is σ . If $\sigma > \text{Log } 1/Q_D$ (where Log denotes natural logarithm) we get a length of random testing $L < 2^n$. This is the case for every circuit noted above the dotted line in Fig. 7 ($\sigma \geq 7$ for $Q_D = 10^{-3}$).

IV. CONCLUSION

A distinction between testing quality and detection quality has been introduced. These notions allow us to prove that only the probability of not detecting the fault which is most difficult to detect has to be considered. The detection surface of a combinational network is introduced, and two easy approaches to get a lower bound of this detection surface are given. These properties are applied to combinational TTL integrated circuits. It is shown that some of them are testable with a random input sequence shorter than an exhaustive test.

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On Monte Carlo Testing of Logic Tree Networks

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Abstract—It is shown that by a proper selection of the probabilities of 0 and 1 at the inputs, the efficiency of random test gen-

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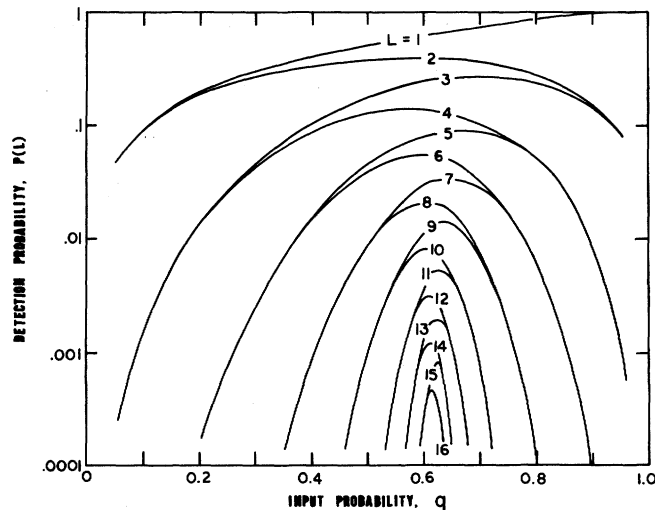


Fig. 1. Detection probability as a function of input probability for tree network of two-input NAND gates.

eration can be improved. This correspondence includes some results describing the testing of actual logic networks used in a computer.

Index Terms—Combinational tree networks, detection probability, fault detection, logic testing, random test generation.

INTRODUCTION

Several papers [1]–[4] have reported the use of the Monte Carlo method for logic testing. In this method, the tests are obtained from random inputs. The purpose of this correspondence is to show that in a combinational logic tree, the probability of detecting a fault can be optimized by a proper selection of the probabilities of 0 and 1 in the random inputs. This fact is used for improving the efficiency of test generation over the commonly employed heuristics of equiprobable 0 and 1. The results, which are derived from a probabilistic analysis of a NAND tree model [5], are much simpler than other approaches [6]–[8] when applied to large circuits. Experiments on actual logic boards of a computer show good agreement with the analysis.

SELECTION OF INPUT PROBABILITY

Consider a fan-out-free tree network of n -input NAND gates. Such a network was analyzed in [5] where the following results have been derived. The probabilities of logical 0 or 1 occurring on a line in the l th level are

$$p_l^0 = (p_{l-1}^1)^n = (1 - p_{l-1}^0)^n \quad (1)$$

and

$$p_l^1 = 1 - p_l^0 = 1 - (p_{l-1}^1)^n, \quad (2)$$

respectively, where the primary inputs are in the 0th level and all the n inputs of a gate are assumed to be in the same level. The detection probability, which is defined as the probability of sensitizing a path from a primary input to the primary output in the L -level circuit, is given by

$$P(L) = \prod_{l=0}^{L-1} (p_l^1)^{n-1}. \quad (3)$$

This probability can be computed from the input probability. For example, if all the gates have a fan-in $n = 2$, and the primary inputs are 1 with probability q and 0 with probability $1 - q$, then $P(L)$ is obtained from (3) by substituting the following:

$$\begin{aligned} p_0^1 &= q & p_0^0 &= 1 - q \\ p_1^1 &= 1 - q^2 & p_1^0 &= q^2 \\ p_2^1 &= 1 - (1 - q^2)^2 & p_2^0 &= (1 - q^2)^2 \\ p_3^1 &= 1 - [1 - (1 - q^2)^2]^2 & p_3^0 &= [1 - (1 - q^2)^2]^2 \\ &\dots & &\dots \end{aligned} \quad (4)$$

The detection probability $P(L)$ for various levels L is shown in Fig. 1 as a function of q . In a majority of the reported work on the Monte Carlo test generation, q is taken as 0.5, perhaps on the basis of simple intuition. Fig. 1, however, shows that a q somewhat greater than 0.5 will give better results due to the increased detection probability. For example, for a nine-level path, $q = 0.5$ gives a detection probability of approximately 0.001, which can be increased almost ten times by changing q to 0.64. A closer examination of (4) will reveal that, in general, for any value of q , the probabilities p_l^1 and p_l^0 fluctuate widely, attaining the values close to 0 and 1 in the alternate levels [5]. However, for optimum input probability, q_{opt} , these fluctuations subside and p_l^1 and p_l^0 remain constant for any l . This is particularly true for large logic chains. Thus for large L , q_{opt} can be obtained from the equation

$$q = 1 - q^n \quad (5)$$

for n -input gates. When $n = 2$, (5) gives $q_{opt} = 0.617$. This is, in fact, the value of q at which $P(L)$ peaks for large L (Fig. 1). Next, from (3), we have

$$P(L) = (q_{opt})^L. \quad (6)$$

There is no reason to believe that more frequent 1's than 0's at the primary inputs will give better results for all practical circuits. If a similar analysis of a NOR tree network is carried out, q_{opt} will turn out to be just the complement of the value obtained above. Similarly, a NOT gate at an input can also complement the input probability. For a practical circuit, therefore, one must try both the input probabilities, i.e., q_{opt} as given by (5) and $1 - q_{opt}$.

Further, the probability of sensitizing a path of L levels by at least one out of M independent input patterns is given by

$$P(L, M) = 1 - [1 - P(L)]^M. \quad (7)$$

Since it is most difficult to sensitize the longest path in a circuit, its detection probability being the lowest among all the paths, the number of patterns should be such as to make the probability $P(L, M)$ close to unity for the longest path. If L is

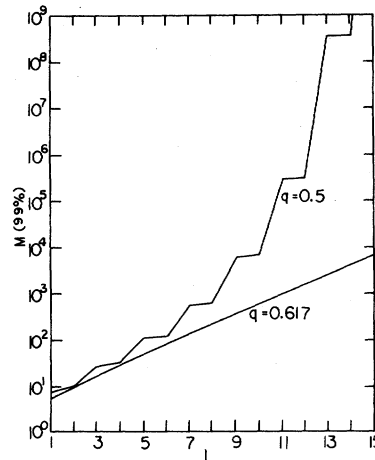


Fig. 2. $M(99 \text{ percent})$ as a function of levels for tree network of two-input NAND gates.

TABLE I
Results of Test Generation

Circuit	No. of Lines	No. of Levels	Input Prob.	No. of Random Patterns	No. of Tests Generated	Faults Undetected
Circuit 1	114	5	0.5	31	19	0
			0.7	17	7	0
Circuit 2	115	10	0.5	>1000	35	8 percent
			0.617	800	30	0

the maximum number of levels in a circuit, then for $P(L, M) = 0.99$, we have

$$M(99 \text{ percent}) = \ln(0.01) / \ln[1 - P(L)]. \quad (8)$$

Experimental results [5] have shown that $M(99 \text{ percent})$ as given by (8) provides a good estimate of the number of random input patterns required for test generation for practical combinational circuits having tree structure. If we use the optimum input probability, then for large L , (6) and (8) give

$$M(99 \text{ percent}) \approx 4.6(q_{\text{opt}})^{-L}. \quad (9)$$

This is shown in Fig. 2 for two-input gates (i.e., $n = 2$, $q_{\text{opt}} = 0.617$). For comparison, the corresponding curve for $q = 0.5$ is also given. As the number of levels increases, the need for using the optimum input probability becomes greater. For example, if $L = 13$, with $q = 0.5$ the number of patterns required is 300 million. This number reduces to 2000 if q is changed to 0.617.

EXPERIMENTAL RESULTS

A Monte Carlo test generation program, similar to the one described in [5], was used to generate tests for several of the processing unit circuit boards of the Illiac IV computer [1], [3]. Only the stuck type of faults on the input lines were considered, assuming that these require the sensitization of the longest paths and hence are the most difficult to detect. Inputs were determined by a random number generator which produced floating point numbers uniformly distributed in the interval $[0, 1]$. If the random number was less than q , the line

was set to 1; otherwise it was set to 0. All inputs were determined independently, but with the same q . A digital simulator then determined all the line values, and a TEST-DETECT program determined whether any of the input faults have been detected. As explained earlier, both the input probabilities q_{opt} and $1 - q_{\text{opt}}$ were tried. Pattern numbers 1, 3, 5, ... were generated with $q = q_{\text{opt}}$, and 2, 4, 6, ... with $q = 1 - q_{\text{opt}}$. The circuits had tree-type structures and consisted of {AND, OR, NOT} combinational logic. The fan-ins varied from 1 to 5, the average fan-in being about 2.2. It is well known that such circuits can be realized by NAND or by NOR gates alone, and therefore the analysis may be applicable to them. The results of test generation for two of the circuits are given in Table I and Fig. 3.

Circuit 1 had 5 levels, and from Fig. 1, $q_{\text{opt}} = 0.7$. All the faults were detected with 17 random patterns which gave 7 tests. This circuit had 47 primary inputs. When the test generation was repeated with $q = 0.5$, all faults were detected by a set of 19 tests generated by 31 random patterns. Circuit 2 had 10 levels and 56 primary inputs. Fig. 2 gives about 5000 patterns for $q = 0.5$. Indeed, the test generation was incomplete when the program was stopped after 1000 patterns, leaving 8 percent of the faults undetected. When q was changed to $q_{\text{opt}} = 0.617$, the test generation was completed after 800 patterns (Fig. 3). All the faults were detected by 30 tests as compared to the 35 generated in the former case.

The above results lead to two interesting observations. 1) Proper selection of the input probability can increase the efficiency of test generation, resulting in reduced computer time, and 2) since q_{opt} increases the detection probability, each pattern, on the average, detects a greater number of faults. This

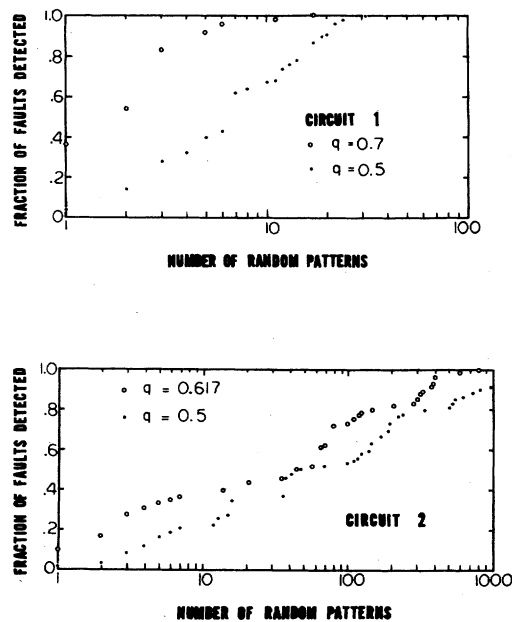


Fig. 3. Test generation for practical circuits.

results in a more compact test set as compared to the test set obtained by other input probabilities (Table I).

CONCLUSION

The optimal input probability q_{opt} for Monte Carlo test generation is found to be a function of the fan-ins of the gates and the number of levels in the circuit. For practical circuits, q_{opt} can be obtained by using the average fan-in. It appears that one should try random patterns with both probabilities q_{opt} and $1 - q_{opt}$ while testing practical forms of {AND, OR, NOT} logic when q_{opt} is obtained from the NAND model. Although the variation of the input probability has been suggested in earlier papers [6]–[8], the results of this correspondence are easier to apply to large circuits. A further application of this analysis is in logic testing without the prior test generation [2].

The present analysis is statistical, and hence may be applicable to large circuits only. Furthermore, the model used in the analysis [5] restricts its applicability to tree-type combinational networks.

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