CSV 881: Low-Power Design   
Fall 2013

Homework 1 Problems

Assigned 22/10/13, due 23/10/13

**Answer the following questions by circling or underlining exactly one choice.**

1. On an average how much power does a large Gray code counter consume in comparison to a binary counter?

Twice Same Half ¼ 1/n for n-bit counter

1. Power consumption of a high performance processor chip is:

10-100 W Less than 1W 500mW 1kW 0.5-1.0W

1. The inversion encoding for a reduced-power n-bit bus works as follows:

All 0 bits are inverted All 1 bits are inverted Bits are always inverted

All bits are inverted when number of transitions exceeds n/2 Only half the bits are inverted

1. A 1 microfarad capacitor is charged to a voltage 1 volt through a 100 kilo ohm series resistor. What is the energy dissipated in the resistor?

1 watt 1 calorie 1 microjoule half microjoule 1 microwatt

1. A digital circuit dissipates 2 nanojoule of energy per cycle. If the clock rate is 1GHz, what is the power consumption of the circuit?

1 joule 1 nanowatt 1 watt 2 watts 0.5 watt

1. Identify the largest component of power in a digital CMOS circuit:

Static Dynamic Short-circuit Leakage Glitch

1. How do glitches affect the power consumption of a digital circuit?

Increase static power Increase dynamic and short-circuit power

Only increase short-circuit power Have no influence on power consumption

Radiate energy

1. Short-circuit power can be reduced to zero if,

Gates are fast VDD is below the sum of threshold voltage magnitudes of p and n devices

Clock frequency is very low Circuit is kept cool Rise/fall times are small

1. Path balancing and glitch filtering are methods for,

Making circuit fast Reducing noise Improving Reliability

Reducing dynamic power Saving leakage of static power

1. What is the dynamic power consumption of a 1 million gate VLSI chip for which VDD = 1 volt, average gate capacitance = 1pF, average activity factor (counting both rising and falling transitions) = 10%, clock frequency = 2GHz?

100W 20W 10W 2W 1W

1. Which is the most effective method for reducing the power consumption of a CMOS logic circuit?

Increase threshold voltage Reduce threshold voltage Reduce clock frequency

Use body bias Reduce VDD

1. What determines the upper bound for VDD?

Device breakdown electric field Power consumption Power grid

Threshold voltage No limit

1. What determines the lower bound for VDD?

Device breakdown electric field Power consumption Power grid

Threshold voltage No limit

1. How much power does the clock signal consume in a typical CMOS circuit?

1W 10W approx. 10% 40-50% 90%

1. Clock gating reduces power consumption in:

Combinational logic Flip-flops Clock distribution network

Power grid Clock buffers