ELEC 6270-001: Low Power Design Class Projects, Spring 2015, **Assigned 4/13/15**

1. Design a ring oscillator in 32 nm CMOS technology and examine its frequency and power performance as a function of supply voltage ***(Finch).***
2. Design a ring oscillator in 32 nm CMOS technology and examine its frequency and power performance as a function of supply voltage ***(Masten).***
3. Design a 32-bit ALU with sleep mode for 22 nm technology ***(Sanders).***
4. Design a 32-bit ALU with sleep mode for 22 nm technology ***(Wright).***
5. Compare power consumption of 4-bit binary counters with various state encodings including gray and one-hot codes ***(Akula).***
6. Compare power consumption of 4-bit binary counters with various state encodings including gray and one-hot codes ***(Chen).***
7. Provide a conclusive study of power and performance of asynchronous processors ***(Conover).***
8. Design a 32-bit adder with reduced supply and parallelism for power saving ***(Duanmu).***
9. Design a 32-bit adder with reduced supply and parallelism for power saving ***(Gupta).***
10. Verify the alpha-power law by spice simulation of a CMOS inverter chain ***(Kannan).***
11. Verify the alpha-power law by spice simulation of a CMOS inverter chain ***(Kim).***
12. Minimize test power for c6288 in 32 nm CMOS by optimal ordering of vectors ***(Li).***
13. Minimize test power for c6288 in 32 nm CMOS by optimal ordering of vectors ***(Liu, J.).***
14. Examine low voltage (below threshold) operation of benchmark circuit c6288 in high leakage technology ***(Liu, X.).***
15. Examine low voltage (below threshold) operation of benchmark circuit c6288 in high leakage technology ***(Patva).***
16. Redesign non-critical path gates of a 32 bit adder for slower operation and estimate power saving ***(Ramaiahgari).***
17. Redesign non-critical path gates of a 32 bit adder for slower operation and estimate power saving ***(Ren).***
18. Use high threshold voltage for non-critical path gates of a 32 bit adder and estimate power saving ***(Richardson).***
19. For a power constrained 32-bit adder find the voltage that will allow highest performance ***(She).***
20. Use high threshold voltage for non-critical path gates of a 32 bit adder and estimate power saving ***(Smith).***
21. Use high threshold voltage for non-critical path gates of a 32 bit adder and estimate power saving ***(Tao).***
22. Redesign a 4-bit ALU circuit for glitch reduction and examine its power saving ***(Thorington).***
23. Redesign a 4-bit ALU circuit for glitch reduction and examine its power saving ***(Vuddagiri).***
24. Design s5378 in 32 nm CMOS for reduced scan mode activity ***(Wang).***
25. Design s5378 in 32 nm CMOS for reduced scan mode activity ***(Xia).***
26. Design a 32-bit adder for low voltage operation with level converters ***(Yelamanchili).***
27. Design a 32-bit adder for low voltage operation with level converters ***(Zhang, H.).***
28. Design a reduced power shift register with clock gating ***(Zhang, X.).***
29. Design a reduced power shift register with clock gating ***(Zhao).***
30. Low voltage operation of a 16 bit counter in 32 nm CMOS technology ***(Zhu, Y.).***
31. Low voltage operation of a 16 bit counter in 32 nm CMOS technology ***(Zhu, Z.).***

***Expected Results:***

1. Clear understanding of the problem.
2. To the point analysis.
3. Reliable (reproducible) data.
4. Meaningful conclusions usable by others.
5. Readable four to six page report (**due on 5/1/15**) written and formatted like a technical paper (PDF).