**ELEC 6200 Computer Architecture and Design**

**Project Part 6**

**Graduate student**

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**What did you learn from this project?**

This is my first time to design a hole CPU project. Although I had use Altera Quartus II and DE2 Manual to simulation when I was undergraduate, this simulation is different to I used did. The project let me know the construction and architecture of CPU clearly. And In my process I had try to use many different data-path, it can lead to different result of design of control unit. The data-path verification also let me know the control unit how to connect to each other instruction.

This project gives me a deep comprehend of CPU.

**What would you do differently next time?**

In this time I used multi-cycle data-path. For next time I may try to use single-cycle or pipelined data-paths. For these two data-paths need create a truth table listing all control signals and the values of each control signal required for executing each instruction, which I didn't do in this time. Also in following structure there will have a lot of difference. I think different way to do a project always have fun in process and it can help me learn more about the CPU.

**What is your advice to someone who is going to work on a similar project?**

The first two part of project is the basic part for CPU, but don't take lots of time on how to make a better ISA or data-path. Just keep going. Better ISA or data-path always depends on your control system or Data-path Verification. When you come to the part 3 or part 4 it also have time to adjust your ISA or Data-pass. At that time you will find which data-path is most suit for your design. Maybe it not most brief, but it can be most efficiency for your design.