Computer A&D Term Project Part 6

Aaron Vance

1. **What did I learn**

A better understanding of ISA as well as the process of designing a CPU using VHDL models, simulations and debugging.

1. **What would I do different next time**

Since I used a single-cycle datapath, I may choose either multicycle or pipelining just to further my understanding of a more complex CPU design. Our ISA only had 8 instructions since we wanted to have an easy project to simulate on test, but I would add more for programming convenience if this CPU was to actually be used. I would also start earlier, due to the fact that simulation and debugging takes a long time and can be frustrating.

1. **My advice to the one who is going for this project**

To have the least frustrating time with this project use, I suggest using a single-cycle design with memory for both instructions and data. If it fancies you, try to mimic an actual working CPU design since sometimes getting your feet off the ground is the hardest part. Before writing any VHDL code, make sure you label each connection on your CPU diagram. This labeling will save you a lot of headaches. Try to use as little instructions as possible as this allows easier simulation and debugging. Finally, start earlier since debugging tiny mistakes can be time consuming.