**CPU Design Project – Part 5**

**Xi Li**

1. **What did you learn from this project?**

As the datapath I designed is pipeline, I have learned more about the pipeline such as its architecture when I programming it by using VHDL, its working principle when I simulated every standard instruction cycle by cycle and so forth. Among those, the most significant thing that I have a profounder understanding about the hazard, especially the data hazard and control hazard, of pipeline when I tested a program. In order to avoid the data hazard, I used “stall” and code reordering when I wrote my test program.

1. **What would you do differently next time?**

Since there is no forwarding and hazard detection units in my design, I will add these two units in my datapath next time so that its performance will be improved.

1. **What is your advice to someone who is going to work on a similar project?**
2. Do not ignore any mistakes or bugs during every part of the whole project and try to exam every standard instruction once you finish the datapath; when you have some changes in the datapath, exam all those instructions again to make sure that they can run successfully and it will be better to have a copy of the original code.
3. Our TA is very helpful, she gave me lots of help on the project, especially on the memory, so do not hesitate to ask TA for help when you meet problem which you cannot solve on earth.
4. Do the project as early as possible because you really do not know how much time you will spend on tat.