**CPU Design Project – Part 6**

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**What did you learn from this project?**

This project is a design for the CPU. In it, I design the instructions of ISA, the structure of data path, the data path component VHDL design, the top-level design and whole system debugging. So that each parts of project makes me understand how the CPU work, how the instructions make CPU do different works. The whole project makes me understand the class better.

When I do the simulation and debugging for the project. I learn to use the software Quartus II and Modelsim. And in the simulation and debugging, I learn how to deal will timing problem and flaw in my design.

**What would you do differently next time?**

This time, I design data path in multi-cycle. Next I think I will try to design pipeline data path. The pipeline data path may have more hazard problems than multi-cycle data path. It will make me understand pipeline data path and hazard problem better. And I will try to simplify my state as much as possible that can make the data path execute more quickly.

**What is your advice to someone who is going to work on a similar project?**

First, I suggest do this project by only yourself. If you finish all parts of the project. You will learn more knowledge than you have a partner. You will have experience in the simulation and debugging.

Second, do it as early as possible. If you have enough time, you can do it before the due time. Because in the coding and debugging, there will be lots of problems which you need to fix it out. So that you need to speed much time on debugging. Especially for the timing problem, it is difficult for us to find it out. Because the simulate software cannot help you to find this kind of problems.

Third, be patient when you debug. Remember keeping each parts in you project is correct. And it is not difficult to design a small part and make it work. But for whole system, it is difficult to find the mistake out. So that, be patient and think more in each parts’ design.