CPU Design Project – Part 6 Report

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1. **What did you learn from this project?**

In this project, I learned how to build a multi-cycle datapath cpu. I learned more about a multi-cycle datapath by beginning with the initial design and gained more knowledge as the project went on. I also gained valuable experience with VHDL. I especially feel that this helped me understand how I might better use VHDL in the real world. I believe this entire project helped me take various things I have learned about in other classes, and tie all of them together in one project.

1. **What would you do differently next time?**

As others have suggested in previous semesters, I would try to implement a pipeline datapath. Although it initially seemed much more intimidating to implement, I believe it would have actually been more simple in the long run.

1. **What is your advice to someone who is going to work on a similar project?**

My first suggestion would be to follow the suggestion of Dr. Agrawal and read through all of the parts before starting. It would have helped tremendously to already have an idea what was going to be expected in the later parts. As an undergrad, it is not required to implement and demonstrate the project. If I were to have gotten ahead earlier on, I definitely would have tried to demonstrate my project and I believe I would have benefitted greatly from this.

My next suggestion would be to start as early as possible on the top level design. This was the biggest hurdle for me to overcome. I ran into many issues during this portion and had to spend lots of precious time trying to debug things that I could have been working on all along.