ELEC 5200 CPU Design Project Part 6 – Hardware Implementation and a Working Processor Demo

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The purpose of this CPU project is to design a RISC CPU in the VHDL modeling language, verify the design using Aldec “Active-HDL” simulator, and implement on an Altera DE2 FPGA board using Altera’s Quartus II software. Part 1 was to design an instruction set architecture (ISA) for a new 16-bit microprocessor (μP). The μP will be designed and modeled in VHDL in later parts. Your ISA is to be designed using RISC design principles, with the primary design goals being low cost and a minimal number of clock cycles per instruction. Some of the main requirements for the ISA was as follows. The ISA may contain no more than 16 unique instructions. However, you may have multiple formats for a given type of instruction, if necessary. Of the 16 instructions, at least one instruction should make your processor HALT. The ISA should contain appropriate numbers and types of user-programmable registers to support it.

Part 2 was to design the datapath of a CPU that will realize the instruction set architecture (ISA) designed in the previous part (including any “adjustments” made to the ISA). The datapath choose for my design was a single cycle datapath since it is the easiest to implement and with simple instructions the timing will be as quick as if I was using multi cycle. Part 3 was to develop and verify the VHDL model for each unique component within your datapath. Also, design and test a VHDL “behavioral” model of the control unit to realize the behavior described in your control signal table in part 2, including any instruction decoding. Part 4 was to combine all the components created in part 3 together into a new top-level component which will include both datapath and the control unit connected to each other. Part 5 was to complete the system design by adding Altera memory modules, and write a test program that contains all kinds of instructions in your ISA.

In conclusion, this project was a great design and programming practice. I was reminded that you must be thorough in your design process when each part is dependent on the part before it. This project was a great insight of what goes into developing a CPU and made me interesting in working in that field. As far as changes I would make if I could do this project differently, I would try to make the CPU as fast and efficient as possible. I would definitely do more research in simplifying the instruction set to its bare necessities and test different datapaths with my ISA. My advice for someone who is going to work on a similar project is to start early on the project, make sure you do research to gather ideas to implement in your design, and make sure you thoroughly understand each component in your design and test them thoroughly.