**CPU Design Project – Part 6 – Hardware Implementation and a Working Processor Demo**

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During the project, we’ve learn tons of knowledge. That includes getting understanding of how a CPU operate, what is the structure of a basic CPU and how it works in a FPGA board etc. In detail, since our design is multi-cycle datapath, which is quite different from single-cycle datapath and pipeline datapath. In multi-cycle, an instruction might take several cycles. Therefore we have to pay more attention to the slides that refers to multi-cycle datapath. Moreover, since we use VHDL code for designing this project. That is a good way to get more familiar with VHDL by using VHDL to design each components. Eventually, when we were doing project 5, we found there is an error if we don’t add a wait instruction after LW and SW instruction. So we realized there is a small difference between ideal design and actual design. In project 6, we have chance to download program to FPGA board, which renders us to get more understanding of this project.

If I do this project next time, I will choose pipeline datapath. That is simply because we had design multi-cycle datapath, and it is apparently slower than pipeline datapath but use less components. In pipeline datapath, it should be used more components to consist registers between each stages, hazard detection unit and forwarding unit, which is more complicated than multi-cycle datapath.

I strongly recommend new students to read requirements of all six projects before they actually do this project. In this project, we had changed some designs just because we did not read through all six projects requirement. Secondly, I don’t know if other people’s design, but in my multi-cycle design, it is sort of different to the design of slides. In my design, when execute instruction LW and SW, I have to insert a wait instruction to ensure it fully executes the instruction. And in project 5 and 6, please read through “Altera Quartus II and DE2 manual”, which a tutorial shows how to initialize Quartus II is. By the way, the version I used is Quartus II 13.0.