**Raphael Bendy**

**(a) What did you learn from this project?**

How to design a CPU from scratch using VHDL (Instruction Set Architecture, Datapath, VHDL Modeling), how to better use VHDL modeling and simulating tools, and working with the Altera DE2 FPGA. Among the individual components (registers, multiplexers, control unit) of the CPU, I learned the importance of having some devices becoming active on falling clock edges while others become active on rising clock edge in order to resolve timing issues and be able to get more done within the same clock period.

Designing each component by hand, putting them together according to a datapath, and then implementing the design on hardware and having it run custom code has really de-mystified CPUs.

**(b) What would you do differently next time?**

Maybe try to implement a pipeline architecture, which would offer improvements over a multicycle architecture. Also, adding another ALU so that some instructions (BEQ, BNE) can require less clock cycles because the one ALU doesn’t have to be shared.

I had to go back and modify my instruction set architecture after realizing that some of the instruction formats are not compatible with the way the data path is arranged. I didn’t discover the conflict until trying to simulate to design, but if I worked on a new design then these conflicts would already be accounted for.

There was a timing issue with the RAM that did not appear in simulation but does appear when the design is implemented on the FPGA. I would like to thoroughly debug the RAM in the design if I were to work on it some more.

**(c) What is your advice to someone who is going to work on a similar project?**

Start early on VHDL modeling because many bugs will appear that you didn’t account for when you go to simulate, and then even more bugs will appear when you implement your design on hardware. Create testbenches to facilitate simulation, especially for the control unit. You will have to tweak minor settings and re-launch the simulation of the control unit many times, in my experience.