ELEC 2200-002 Digital Logic Circuits   
Fall 2012

Classwork 2 Solution (answers shown in **bold**)

Assigned 8/29/12, due 8/29/12

**Answer the following questions, selecting just one answer per question.**

1. What types of electronic circuits does a transceiver of a cell phone contain?

1. Analog
2. Digital
3. Memory
4. Combination of digital, mixed-signal and RF
5. None of the above

2. What are the five building blocks of a digital computer?

1. Memory, logic, passive and active components
2. Datapath, control, memory, input and output
3. Display screen, keyboard, mouse, power supply and cooling fan
4. Transistors, chips, resistors, capacitors and inductors
5. Hardware, software, firmware, programmer and operator

3. What is the radix for binary numbers?

1. 1
2. 2
3. 4
4. 8
5. 10

4. What format does a modern digital computer use to represent integers?

1. Signed magnitude
2. Decimal
3. 1’s complement
4. IEEE 754 Standard format
5. 2’s complement

5. How can you tell whether a 2’s complement integer is positive or negative?

1. By complementing all bits
2. By complementing all bits and then adding 1
3. Negative only if adding the number to its magnitude produces 0
4. Positive if MSB = 0, negative if MSB = 1
5. Negative if MSB = 0, positive if MSB = 1

6. What is the negation rule for 2’s complement numbers?

1. Invert all bits
2. Invert all bits if MSB is 0
3. Invert all bits and add 1
4. Change MSB to 1
5. Invert all bits and subtract 1

7. What indicates overflow when two n-bit 2’s complement integers are added?

1. A carry of 1 is generated when MSB’s are added
2. Two numbers being added have opposite signs
3. Two numbers being added have the same sign
4. Two numbers have the same MSB, which differs from the MSB of sum
5. None of the above

8. What is the number of bits needed to hold the product of two n-bit 2’s complement integers?

1. n
2. More than n
3. 2n
4. n +1
5. n2

9. When two n-bit 2’complement integers are added, how should we handle the last carry bit generated from the addition of the MSBs?

1. Extend the sum to have n+1 bits
2. Declare overflow
3. Change the sign of the sum if the last carry bit is 1
4. Check the result if the last carry is 1, because it should always be 0
5. Just discard the last carry bit

10. Given a 2’s complement integer, x = 10000, what is – x?

1. 00000
2. 01111
3. 16 (decimal), which cannot be represented with 5 bits
4. 11111
5. – 10000

11. What is the correct answer for the signed-integer computation: 10101 + 01010 = ?

1. 00101 or 5 (decimal)
2. 11111 or – 0 (decimal)
3. 11111 or – 1 (decimal)

12. What is the correct answer for the 1’s complement computation: 10101 + 01010 = ?

1. 00101 or 5 (decimal)
2. 11111 or – 0 (decimal)
3. 11111 or – 1 (decimal)

13. What is the correct answer for the 2’s complement computation: 10101 + 01010 = ?

1. 00101 or 5 (decimal)
2. 11111 or – 0 (decimal)
3. 11111 or – 1 (decimal)

14. What causes overflow when computing using a digital circuit?

1. Electrical noise
2. Faulty circuit
3. Binary result needs more bits than the circuit is designed for
4. A mathematical problem
5. Design error

15. Overflow is impossible in binary addition of two integers if,

1. both integers are positive
2. two integers have opposite signs
3. both integers are negative
4. integers are too large
5. one integer is too large and the other too small

16. In case of overflow, the result is,

(a) almost correct

(b) wrong

(c) easily correctable

(d) correct in magnitude but has a wrong sign

17. Following table describes the function of a two-bit half adder (without a carry input). Complete the last two columns:

|  |  |  |  |
| --- | --- | --- | --- |
| Input bit a | Input bit b | Output sum a + b | Output carry |
| 0 | 0 |  |  |
| 0 | 1 |  |  |
| 1 | 0 |  |  |
| 1 | 1 |  |  |

18. Following table specifies the function of a circuit that detects overflow when two 32-bit 2’s complement integers are added. The most significant bits (MSB) of the two integers are a31 and b31 and that of the sum is s31. The output of the circuit is 1 only when there is an overflow. Complete the last column of the table.

|  |  |  |  |
| --- | --- | --- | --- |
| Inputs | | | Output  1 = overflow |
| a31 | b31 | s31 |
| 0 | 0 | 0 |  |
| 0 | 0 | 1 |  |
| 0 | 1 | 0 |  |
| 0 | 1 | 1 |  |
| 1 | 0 | 0 |  |
| 1 | 0 | 1 |  |
| 1 | 1 | 0 |  |
| 1 | 1 | 1 |  |

19. The following circuit is an adder built with full adder blocks (FA). It adds 2’s complement integers a and b. Each full adder block has a one unit of time delay. What is the critical path delay of the 32-bit adder?

Answer: Critical path delay is \_\_\_\_\_\_\_\_\_\_ units.

**0**

**a0**

**b0**

**sum0**

**FA**

**sum1**

**a1**

**b1**

**FA**

**sum2**

**a2**

**b2**

**FA**

**c31**

**a31**

**b31**

**sum31**

**FA**

20. Specify 32-bit 2’s complement integers a and b that will activate the critical path in the adder of Problem 19.

Answer: a = \_\_\_\_\_\_\_\_\_\_ (decimal), b = \_\_\_\_\_\_\_\_\_\_\_ (decimal), sum = \_\_\_\_\_\_\_\_\_\_\_

MSB LSB

a

b

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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