TABLE OF CONTENTS

PF	REFA	CE	xiii									
ΑI	BOUT	TTHE AUTHORS	χv									
ı	INT	RODUCTION TO TESTING	1									
1	INTRODUCTION											
	1.1	Testing Philosophy	4									
	1.2	Role of Testing	6									
	1.3	Digital and Analog VLSI Testing	7									
	1.4	VLSI Technology Trends Affecting Testing	9									
	1.5	Scope of this Book	15									
2	VLS	SI TESTING PROCESS AND TEST EQUIPMENT	17									
	2.1	How to Test Chips?	18									
		2.1.1 Types of Testing	18									
	2.2	Automatic Test Equipment	24									
		2.2.1 Advantest Model T6682 ATE	24									
		2.2.2 LTX Fusion ATE	28									
		2.2.3 Multi-Site Testing	29									
	2.3	Electrical Parametric Testing	30									
	2.4	Summary	34									
3	TES	ST ECONOMICS AND PRODUCT QUALITY	35									
	3.1	Test Economics	36									
		3.1.1 Defining Costs	36									
		3.1.2 Production	38									
		3.1.3 Benefit-Cost Analysis	41									
		3.1.4 Economics of Testable Design	42									
		3.1.5 The Rule of Ten	44									
	3.2	Yield	44									
	3.3	Defect Level as a Quality Measure	47									
		3.3.1 Test Data Analysis	48									
		3.3.2 Defect Level Estimation	50									

	3.4	Summ	ary {	53
4	FΔII	II T MO	DELING 5	57
7	4.1			,, 57
	4.2			59
	4.3		=	50 50
	$\frac{4.0}{4.4}$			30 30
	4.5		· ·	70
	1.0	4.5.1		72
		4.5.2	±	73
		4.5.3	1 8	74
		4.5.4		75
		4.5.5	_	78
II	TE	ST ME	THODS 8	31
5				33
	5.1		8	33
	5.2			38
	5.3		0	91
		5.3.1	O VI	91
		5.3.2	J F	93
		5.3.3	0	94
		5.3.4	8 8	96
	_ ,	5.3.5	0	98
	5.4	_)1
		5.4.1	Compiled-Code Simulation	
		5.4.2)3
	5.5	_)5
		5.5.1)6
		5.5.2	Parallel Fault Simulation	
		5.5.3)9
		5.5.4		13
		5.5.5	9	16
	r c	5.5.6		17
	5.6			20
	r 77	5.6.1	1 0	21
	5.7	Summ	ary	25
6			TY MEASURES 12	
	6.1		v v	31
		6.1.1		32
		6.1.2	Combinational Circuit Example	
		6.1.3	Sequential SCOAP Measures	40

T/	BLE	OF CONTENTS			vii				
		6.1.4 Sequential Circuit Example			142				
	6.2	High-Level Testability Measures			148				
	6.3	Summary			150				
7	CO	MBINATIONAL CIRCUIT TEST GENERATION			155				
•	7.1	Algorithms and Representations			156				
	1.1	7.1.1 Structural vs. Functional Test			156				
					$150 \\ 157$				
					157 158				
		1							
		7.1.4 Algorithm Completeness			159				
		7.1.6 Algebras			159				
	7.0	7.1.6 Algorithm Types			160				
	7.2	Redundancy Identification (RID)			168				
	7.3	Testing as a Global Problem			172				
	7.4	Definitions			172				
	7.5	Significant Combinational ATPG Algorithms			176				
		7.5.1 D-Calculus and D-Algorithm (Roth)			176				
		7.5.2 PODEM (Goel)			186				
		7.5.3 FAN (Fujiwara and Shimino)			192				
	5 0	7.5.4 Advanced Algorithms			197 204				
	7.6	v							
	7.7	Test Compaction			205				
	7.8	Summary		•	206				
8	SEC	QUENTIAL CIRCUIT TEST GENERATION			211				
	8.1	ATPG for Single-Clock Synchronous Circuits			212				
		8.1.1 A Simplified Problem			214				
	8.2	Time-Frame Expansion Method			214				
		8.2.1 Use of Nine-Valued Logic			216				
		8.2.2 Development of Time-Frame Expansion Methods			218				
		8.2.3 Approximate Methods			222				
		8.2.4 Implementation of Time-Frame Expansion Methods .			222				
		8.2.5 Complexity of Sequential ATPG			225				
		8.2.6 Cycle-Free Circuits			225				
		8.2.7 Cyclic Circuits			229				
		8.2.8 Clock Faults and Multiple-Clock Circuits			231				
		8.2.9 Asynchronous Circuits			232				
	8.3	Simulation-Based Sequential Circuit ATPG			238				
		8.3.1 CONTEST Algorithm			239				
		8.3.2 Genetic Algorithms			246				
	8.4	Summary			248				

9	MEN	ORY 1	TEST	253
	ry Density and Defect Trends	. 255		
	9.2		on	
	9.3	Faults		. 259
		9.3.1	Fault Manifestations	
		9.3.2	Failure Mechanisms	. 260
	9.4	Memo	ry Test Levels	. 261
	9.5	March	Test Notation	. 262
	9.6	Fault 1	Modeling	. 263
		9.6.1	Diagnosis Versus Testing Needs	. 265
		9.6.2	Reduced Functional Faults	. 266
		9.6.3	Relation Between Fault Models and Physical Defects	. 276
		9.6.4	Multiple Fault Models	
		9.6.5	Frequency of Faults	
	9.7	Memo	ry Testing	. 284
		9.7.1	Functional RAM Testing with March Tests	. 284
		9.7.2	Testing RAM Neighborhood Pattern-Sensitive Faults	. 286
		9.7.3	Testing RAM Technology and Layout-Related Faults	
		9.7.4	RAM Test Hierarchy	
		9.7.5	Cache RAM Chip Testing	. 296
		9.7.6	Functional ROM Chip Testing	. 300
		9.7.7	Electrical Parametric Testing	. 301
	9.8	Summ	ary	. 306
10	DSP	-BASE	D ANALOG AND MIXED-SIGNAL TEST	309
	10.1	Analog	g and Mixed-Signal Circuit Trends	. 309
	10.2	Defini	${ m tions}$. 314
	10.3	Functi	onal DSP-Based Testing	. 317
		10.3.1	Concept	. 317
		10.3.2	Mechanism of DSP-Based Testers	. 319
		10.3.3	Waveform Synthesis	. 320
		10.3.4	Waveform Sampling and Digitization	. 322
	10.4	Static	ADC and DAC Testing Methods	. 322
		10.4.1	Transmission vs. Intrinsic Parameters	. 323
		10.4.2	Uncertainty and Distortion in Ideal ADCs	. 325
		10.4.3	DAC Transfer Function Error	. 325
		10.4.4	ADC Transfer Function Error	. 326
		10.4.5	Flash ADC Testing Methods	. 327
			DAC Testing Methods	
	10.5		ing Emulated Instruments Using Fourier Transforms	
			Fourier Voltmeter	
		10.5.2	Testing of Analog Devices Using Non-Coherent Sampling .	
		10.5.3	Coherent Multi-Tone Testing	. 356
			ATE Vector Operations	

	10.6	CODEC Testing	366
	10.0		
		10.6.1 Considerations for CODEC Performance Tests	369
		10.6.2 CODEC Tests	372
		Dynamic Flash ADC Testing FFT Technique	376
	10.8	Advanced Topics	377
		10.8.1 Event Digitization	377
		10.8.2 Measuring Random Noise	380
	10.9	Summary	382
11	MOE	DEL-BASED ANALOG AND MIXED-SIGNAL TEST	385
		Analog Testing Difficulties	386
		Analog Fault Models	387
		Levels of Abstraction	389
		Types of Analog Testing	389
			390
	11.0	Analog Fault Simulation	
		11.5.1 Motivation	391
		11.5.2 DC Fault Simulation of Nonlinear Circuits	391
		11.5.3 Linear Analog Circuit AC Fault Simulation	395
		11.5.4 Monte-Carlo Simulation	397
	11.6	Analog Automatic Test-Pattern Generation	397
		11.6.1 ATPG Using Sensitivities	398
		11.6.2 ATPG Using Signal Flow Graphs	406
		11.6.3 Additional Methods	413
	11.7	Summary	413
12	DEL	AY TEST	417
		Delay Test Problem	417
		Path-Delay Test	420
	12.2	12.2.1 Test Generation for Combinational Circuits	424
		12.2.2 Number of Paths in a Circuit	427
	10.0	Transition Faults	$\frac{427}{428}$
	12.4	Delay Test Methodologies	429
		12.4.1 Slow-Clock Combinational Test	429
		12.4.2 Enhanced-Scan Test	430
		12.4.3 Normal-Scan Sequential Test	431
		12.4.4 Variable-Clock Non-Scan Sequential Test	432
		12.4.5 Rated-Clock Non-Scan Sequential Test	434
	12.5	Practical Considerations in Delay Testing	434
		12.5.1 At-Speed Testing	435
	12.6	Summary	436
13	יחחו	Q TEST	439
		Motivation	439
			441
		Faults Detected by I_{DDQ} Tests	441

		13.3.1 I_{DDQ} Fault Coverage Metrics	446
		13.3.2 I_{DDQ} Test Vector Selection from Stuck-Fault Vector Sets	448
		13.3.3 Instrumentation Problems	451
		13.3.4 Current Limit Setting	452
	13 4	Surveys of I_{DDQ} Testing Effectiveness	453
		Limitations of I_{DDQ} Testing	455
		Delta I_{DDQ} Testing	456
		I_{DDQ} Built-In Current Testing	458
		I_{DDQ} Design for Testability	460
		Summary	460
	10.5	Summary	100
Ш	DE	SIGN FOR TESTABILITY	463
14	DIGI	TAL DFT AND SCAN DESIGN	465
	14.1	Ad-Hoc DFT Methods	466
	14.2	Scan Design	467
		14.2.1 Scan Design Rules	469
		14.2.2 Tests for Scan Circuits	471
		14.2.3 Multiple Scan Registers	474
		14.2.4 Overheads of Scan Design	474
		14.2.5 Design Automation	477
		14.2.6 Physical Design and Timing Verification of Scan	479
	14.3	Partial-Scan Design	479
	14.4	Variations of Scan	483
	14.5	Summary	485
15	BUIL	LT-IN SELF-TEST	489
	15.1	The Economic Case for BIST	490
		15.1.1 Chip/Board Area Cost vs. Tester Cost	492
		15.1.2 Chip/Board Area Cost vs. System Downtime Cost	494
	15.2	Random Logic BIST	495
		15.2.1 Definitions	495
		15.2.2 BIST Process	496
		15.2.3 BIST Pattern Generation	498
		15.2.4 BIST Response Compaction	512
		15.2.5 Built-In Logic Block Observers	519
		15.2.6 Test-Per-Clock BIST Systems	521
		15.2.7 Test-Per-Scan BIST Systems	521
		15.2.8 Circular Self-Test Path System	525
		15.2.9 Circuit Initialization	526
		15.2.10 Device Level BIST	526
		15.2.11 Test Point Insertion	528
	15.3	Memory BIST	529
		15.3.1 Definitions	530

		15.3.2 March Test SRAM BIST	532
		15.3.3 SRAM BIST with MISR	534
		15.3.4 Neighborhood Pattern Sensitive Fault Test DRAM BIST	536
		15.3.5 Transparent Memory BIST Tests	539
		15.3.6 Complex Examples	539
	15.4	Delay Fault BIST	540
		Summary	543
40			5 40
16		INDARY SCAN STANDARD	549
	10.1	Motivation	550
	100	16.1.1 Purpose of Standard	552
	10.2	System Configuration with Boundary Scan	553 553
			557 557
		16.2.2 Boundary Scan Test Instructions	564
	16 9		$\frac{564}{569}$
	10.5	Boundary Scan Description Language	509 570
		16.3.2 Pin Descriptions	570
	16.4	Summary	$571 \\ 572$
	10.4	Summary	012
17	ANA	LOG TEST BUS STANDARD	575
		Analog Circuit Design for Testability	576
	17.2	Analog Test Bus (ATB)	576
		17.2.1 Targeted Analog Faults	577
		17.2.2 Analog Test Access Port (ATAP)	579
		17.2.3 Test Bus Interface Circuit (TBIC)	580
		17.2.4 Analog Boundary Module (ABM)	583
		17.2.5 Instructions for 1149.4 Standard	585
		17.2.6 Other 1149.4 Standard Features	589
	17.3	Summary	591
18	SYS	TEM TEST AND CORE-BASED DESIGN	595
	18.1	System Test Problem Defined	596
	18.2	Functional Test	597
		18.2.1 Microprocessor Test	598
	18.3	Diagnostic Test	598
		18.3.1 Fault Dictionary	599
		18.3.2 Diagnostic Tree	600
		18.3.3 A System Test Example	602
	18.4	Testable System Design	604
		Core-Based Design and Test-Wrapper	606
		A Test Architecture for System-on-a-Chip (SOC)	607
		An Integrated Design and Test Approach	608
	1 Ω Ω	Summary	610

TΛ	RI	LE	\cap	F	\sim	\cap	NIT	ΓF	NI-	ΓÇ
17	ı		u		•	9		_	ıvı	ı

v		
^		

19	THE FUTURE OF TESTING	613				
Α	CYCLIC REDUNDANCY CODE THEORY A.1 Polynomial Multiplier	615 616 617				
В	PRIMITIVE POLYNOMIALS OF DEGREE 1 TO 100	619				
C	BOOKS ON TESTING C.1 General and Tutorial C.2 Analog and Mixed-Signal Circuit Test C.3 ATE, Test Programming, and Production Test C.4 Board and MCM Test and Boundary Scan C.5 Built-In Self-Test C.6 Delay Fault Test C.7 Design for Testability C.8 Fault Modeling C.9 Fault Tolerance and Diagnosis C.10 Formal Verification C.11 High-Level Test and Verification C.12 IDDQ Test C.13 Memory Test C.14 Microprocessor Verification and Test C.15 Semiconductor Defect Mechanisms C.16 System Test C.17 Test Economics C.18 Test Evaluation C.19 Test Generation C.20 Periodicals C.21 Conferences and Workshops C.22 Web Sites	621 622 622 623 624 624 625 625 625 626 626 627 627 627 627 628 628 628 629 629				
BII	BIBLIOGRAPHY					
IN	DEX	671				