ELEC 4200 – DIGITAL SYSTEM DESIGN

Spring 2021 – Lecture: WF 1:00 p.m. - 1:50 p.m. in Broun 235
Lab in Broun 320: Section 001 Thursday, 8:00 a.m. – 10:50 a.m.
Section 002 Thursday, 12:30 p.m. – 3:20 p.m.

Bulletin Data: **ELEC 4200. Digital System Design (3)** LEC. 2. LAB. 3. Pr. ELEC 2210 and ELEC 2220. Hierarchical, modular design of digital systems; synchronous and asynchronous sequential circuit analysis and design, programmable logic devices and field programmable gate arrays, and circuit simulation for design verification and analysis.

Textbook: *Digital Logic Circuit Analysis and Design, 2nd Ed. (__Draft__)*, V. P. Nelson, B. D. Carroll, H. T. Nagle, J. D. Irwin, Pearson Education, Inc. 2020, PDF file posted on Canvas course page.

Reference Book: *Digital Design: With an Introduction to the Verilog HDL 5th Edition* by M. Morris R. Mano and Michael D. Ciletti, ISBN-13: 978-0132774208.

Course Webpage*:* http://www.eng.auburn.edu/~uguin/teaching/E4200_Spring_2021/course.html

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Course Goals:
1. To be able to analyze and design digital systems in a hierarchical, top-down manner.
2. To be able to model, simulate, verify, and synthesize digital systems using hardware description languages.
3. To be able to realize designs with programmable logic, including FPGAs

Prerequisites by topic:
1. Digital logic design and analysis
2. Digital electronics
3. Computer system organization and design

Course Outline:
1. Introduction: Modeling Digital Systems with VHDL and Verilog (Week 1)
2. Combinational Logic Circuits (Weeks 2-3)
3. Sequential Logic Circuits (Weeks 4-5)
4. Finite State Machines (Weeks 6-7)
5. Modeling for Synthesis of Register Transfer Level (RTL) Design (Weeks 8-10)
6. Modeling of Memory and Register Files (Weeks 11-12)
7. Design of Efficient Adders and Multipliers (Weeks 13-14)

Lab Outline:
1. Lab 0: Introduction to lab hardware and software
2. Lab 1: Modeling Concepts
3. Lab 2: Numbering Systems
4. Lab 3: Multi-Output Circuits: Encoders, Decoders, and Memories
5. Lab 4: Tasks, Functions, and Testbench
6. Lab 5: Modeling Latches and Flip-flops
7. Lab 6: Finite State Machines
8. Lab 7: Modeling Registers and Counters
9. Lab 8: Behavioral Modeling and Timing Constraints
10. Lab 9: Architectural Wizard, IP Catalog, Counters, Timers and Real-Time Clock
11. Lab 10: Sequential System Design Using ASM Charts
12. Lab 11: Design your own lab project

Typical methods for evaluating student performance:

Hour quizzes (2)	40%
Final exam	20%
Lab projects	40%

Grading Scale:

90-100	A
80-89	B
70-79	C
60-69	D
<60	F

Computer usage: VHDL modeling, simulation, and synthesis assignments will require the use of Mentor Graphics *Modelsim* and *Xilinx Vivado* computer-aided design (CAD) tools. Some information regarding these tools is available on the ELEC 4200 class web page link listed above. Designs will be downloaded and tested on Digilent/Xilinx Nexys4-DDR FPGA development boards.

Laboratory Assignments: All laboratory exercises are to be done individually. Each lab will be graded as described in the *ELEC 4200 Digital System Design Lab* document. Lab assignments (pre-lab and lab reports) and projects must be turned in on or before the designated date/time to receive credit. Pre-lab assignments will be checked at the start of each lab session. Lab reports are due at the beginning of the lab session following the scheduled date for that lab exercise.

Guidelines and format for lab reports: The required content and format of the lab reports is contained in the *ELEC 4200 Digital System Design Lab* handout, posted on the course web page.

Academic Honesty Policy: All portions of the Auburn University student academic honesty code (Title XII) found online at http://www.auburn.edu/academic/provost/academicHonesty.html apply to this class.

Each student is expected to do his/her own laboratory project. Discussion of various aspects of the project with fellow students is acceptable, provided that designs are not copied. Copied work will be considered a violation of the academic honesty code, and dealt with accordingly.

Class attendance: Students are expected to attend class regularly and on time as indicated by the Auburn University "Policy on Class Attendance". In case of absence, the student is responsible for all course business conducted in class. Make-up exams will be scheduled for excused absences covered by Paragraph 4 of the AU "Policy on Class Attendance".

Policy on unannounced quizzes: There will be no unannounced quizzes.

Accommodations: Students who need accommodations should initiate the process by first making an appointment with The Program for Students with Disabilities, 1244 Haley Center, 844-2096 (V/TT).

Contribution of course to meeting the professional component
> Engineering topics: 3 credits
>> 33% engineering science (1 credit)
>> 67% engineering design (2 credits)

Primary student outcomes related to the course ELEC 4200:
(1) an ability to apply knowledge of mathematics, science, and engineering
(2) an ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability
(3) an ability to communicate effectively
(6) an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.

Prepared by:_____Ujjwal Guin_____   Date:_ Jan 13, 2021