ELEC 4200 Digital System Design Lab

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Lab Points Breakdown: 50 possible points each week
Pre-Lab: 10 points
In-Lab: 20 points
Lab Report: 20 points

Final Project Points Breakdown: 100 possible points (plus possible "bonus" points*)
Pre-Lab: 20 points
In-Lab: 40 points
Lab Report: 40 points

* Bonuses of 15 to 30 points may also be available for enhancements to the final project, as specified in the final lab write-up. *The base project must be completed to be eligible for bonus points.*

Pre Lab:
Pre-labs will be checked at the **beginning** of every lab session and returned back to you immediately. Make sure you read each lab manual carefully because there may be multiple requirements. The pre-labs will be graded on completeness, however, it is always in your best interest to ensure they are correct as it will directly correlate to task you are completing in lab.

In Lab:
Each lab manual has one or more circuits that you must synthesize into the FPGA. It is your responsibility to make sure that I verify your completed working circuit(s) before you leave for the day as this will constitute 15 points of the in lab-grade with the other portion for individual lab performance.

Lab Reports:
Lab Reports will be due at the **beginning** of the following lab session in which the lab was completed. They will be graded and returned the following week.

Guidelines and format for lab reports: Lab reports are to be typed with figures, tables, and any hand drawings clearly labeled, attached, introduced and explained at the appropriate point in the typed text portion of the lab report. All lab reports should include:
1. Title and number of lab session.
2. Name(s) of person(s) in lab group.
3. Goal of the lab session – this section should describe in detail the objective of the lab session in terms of what was being designed and implemented and what skills are begin developed.
4. Design process – this section should describe in detail all of the steps of the process

used for the complete design and implementation including both pre-lab and lab exercises.

5. Detailed design – this section should present and describe the details of the design (i.e., K-maps, state diagrams/tables, logic equations, VHDL model). VHDL models should be described in terms of how and what each portion of the VHDL code does.

6. Design verification – this section should provide a detailed explanation of the steps performed to verify the design including **simulation results** as well as a detailed discussion of the thoroughness of the design verification process during simulation. This section should also include a discussion of the **design verification process on the FPGA board** and whether the design implementation worked in the FPGA once simulation based design verification was completed; if the design did not work, described why the design error was not detected during simulation and what modifications to the simulation stimuli must be made to detect and correct the design error.

7. Conclusions – this section should describe in detail what you learned from the lab session including what went right and/or wrong, as well as what you would have done differently if you had the chance to do the lab over again.

8. Answers to questions – this should discuss any questions posed in the lab writeup.