Efficient Strategies for Detection and Avoidance of Counterfeit ICs

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***Abstract*—With the advent of globalization and the resulting horizontal integration, present-day electronic component supply chain has become extremely complex and calls for immediate solutions to eliminate counterfeit integrated circuits (ICs). Such counterfeit ICs – recycled, remarked, overproduced, defective, and/or cloned – have raised serious concerns regarding the safety and security of our critical infrastructures, such as, military systems, financial infrastructures, transportation, communication, medical systems, and many more applications. Due to the lack of efficient detection and avoidance techniques, many more instances of counterfeit ICs evade detection than those that are actually detected. One of the major concern is the reliability of such ICs, and their application in a critical infrastructure may result a catastrophic failure. In addition, the cloned ICs may have additional features that could provide additional capabilities to an adversary to gain control of a system by bypassing security modules. In this paper, two different solutions are presented for detecting the complete spectrum of these counterfeit ICs. These solutions are efficient, low cost and resistant to various known attacks.**

I. Introduction

The growing incidents of counterfeiting and piracy pose a great concern to the Government and Industry because of the substantial resources that are being channelled into the illegal activities by violating law and order to disrupt society, and impose a negative impact on innovation, economic growth, and competitiveness. In addition, the safety and security of our day-to-day lives are at stake as counterfeiting results in inferior quality (low reliability) products. It also results in the loss of business from the trade in counterfeit products [1]. International Chamber of Commerce estimated that the cost of counterfeiting and piracy for G20 nations was as much as US$775 billion every year. However, it will grow at an astonishing rate to $1.7 trillion in 2015 [2].

A report from the Information Handling Services Inc. (Englewood, CO, USA) shows that reports of counterfeit parts have quadrupled since 2009 [3]. This data has been compiled from two reporting entities - The Electronic Resellers Association International (ERAI) Inc. (Naples, FL, USA) and the Government-Industry Data Exchange Program, GIDEP (Corona, CA, USA). It is mentioned that the five most commonly counterfeited components (e.g., analog ICs, microprocessor ICs, memory ICs, programmable logic ICs, and transistors) represent $169 billion in potential annual risk for the global electronics supply chain based on all reported counterfeit incidents in 2011 [4].

The widespread incidents of counterfeiting and piracy of ICs are mainly due to the globalization of semiconductor industry and manufactured in places with limited trust and visibility [5], [6]. Because of the persistent trend of device scaling and the resulting increase in the complexity of the fabrication process, most companies designing system-on-chip (SoC) no longer maintain a fabrication unit (or foundry) of their own. Costs for building and maintaining such foundries are reported to be more than several billions of dollars [7]. This leads to the adaptation of horizontal integration in the semiconductor industry where the SoC designers provide contracts to the foundries and assemblies for production.

II. Threat Space

The US Department of Commerce first proposed the definition for a counterfeit part [8]. As the definition does not cover all counterfeit types, Guin et al. [5], [6], [9]–[13] developed a comprehensive taxonomy of counterfeit types, which is adopted by AS6171 Test Methods Standard; General Requirements, Suspect/Counterfeit, Electrical, Electronic, and Electromechanical Parts [14]. Figure 1 shows the entire threat space that leads to the counterfeiting and piracy. The figure does not include tampered type as the detection pose a different set of challenges and is not included in this paper.

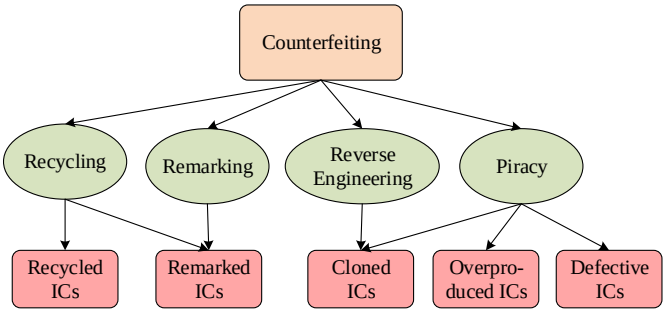

Figure 1: Threat space.

Recycling is a process by which the retired parts (may be functional, but, with reduced lifetime) are reclaimed from a discarded system. This rapid growth of IC recycling is due to the widely available electronic waste (e-waste). In the United States, only 25% of e-waste was properly recycled in 2009 [15]. However, this can be even worse for other countries. This huge resource of e-waste allows counterfeiters to pile

up an extremely large supply of counterfeit components. The reliability of recycled ICs is questionable as the reclaiming process (removal of ICs from a retired electronic system under a very high temperature, and then sanding, repackaging, and remarking) could damage the parts and produce many latent defects. On the other hand, a counterfeiter can remark a lower grade part to its higher grade counterpart mainly to gain larger profits. Similar to recycled parts, remarked ICs have reliability concerns as a space grade IC can withstand a wide range of temperatures, and radiation levels that would cause instant failure for a commercial grade component.

Reverse engineering (RE) is a process of extracting the design specification of the inner details of a product using advanced imaging instruments and powerful characterization tools. An untrusted foundry can extract gate-level netlist from the mask and layout information [16]. Once the foundry extracts the gate level netlist, it's a matter of time that full specification of an IC can be determined. In addition, untrusted foundries may sell illegal copies of the Graphic Database System II (GDSII) files that they receive from SoC designers for fabrication. A wide range of counterfeiters, from small entities to large organizations, can be involved in piracy in order to eliminate the large research and development (R&D) costs. A wide varieties of intellectual properties (IPs), such as register-transfer level (RTL) designs, netlists, and layouts can be pirated. The piracy leads to the cloning and overproduction of ICs. One can also source defective ICs in the market. In this paper, we describe a solution that enables forward trust between various entities in the semiconductor supply chain to prevent cloned, overproduced and defective ICs.

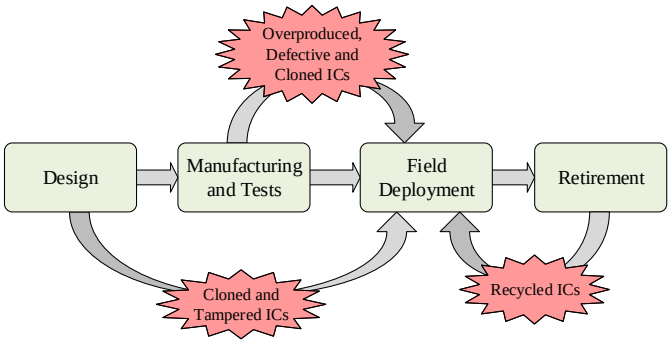

Figure 2: Supply chain vulnerabilities.

It is now important to analyze where these threats are originating from. In the design phase, complex integrated circuits are designed and assembled from RTL to GDSII, and the design steps are performed in many different places (even in different countries) mainly to reduce the development cost and time-to-market. Design reuse has also become an integral part of SoC design in the form of hard IPs (layout level designs), firm IPs (designers can optimize codes with parameterized constraints), and soft IPs (synthesizable RTL designs). In this stage, the counterfeiter can steal IPs to create clones, or tamper with codes to modify the functionality, create backdoors, etc., and sell in the open market (Field Deployment). During manufacturing, an untrusted foundry or assembly can illegally overproduce (more chips outside of the contract) ICs, sell defective chips, which should have been discarded, and manufacture clone ICs. Finally in the retirement stage, a counterfeiter can strip of parts from the retired electronic systems, and sell in the market as new.

III. Prior Approaches

A. Detection of Recycled and Remarked ICs

The detection and avoidance approaches are broadly classified into different categories. First, there are several standards [14], [17]–[19] in practice which recommend different physical and electrical tests to detect these ICs. The goal of these methods is to identify the defects and anomalies (see Chapter 3 of the book "Counterfeit Integrated Circuits: Detection and Avoidance" [6] for details) present in those recycled and remarked ICs, which are not typically present in authentic ones. However, prohibitively excessive test times, test costs, low detection capability and lack of automation make these test methods ineffective. Second, researchers have proposed several schemes based-on statistical data analysis [20]–[22]. Third, on-chip sensors have been proposed as an alternative to the conventional test methods [23]–[26]. Finally, DNA markings [27] are commercially available to provide traceability for electronic parts. Recycled and remarked ICs can be detected via fast or detailed authentication. In fast authentication, the marks fluoresce under UV light. A decision is taken regarding the authenticity of an IC based on the color produced. Detailed authentication is performed in specific laboratories, which is inefficient and costly [28]. Further, if counterfeiters add a different mechanism to the chip which can produce similar fluorescence, DNA marking will be ineffective for fast-authentication as it only observes the color. From the above discussion, it can be inferred that the on-chip sensors are the suitable candidates for detecting these ICs. In this paper, I will briefly describe different on-chip sensors that are proposed in [25], [26].

B. Avoidance of Overproduced, Cloned, and Defective ICs

The existing approaches aim to prevent IC piracy (see Figure 1) by attempting to give an SoC designer control over the number of ICs manufactured [29]–[35]. These approaches can be either passive or active. Passive approaches register all new authorized ICs by incorporating physically unclonable functions (PUFs) in each copy, and then storing their challenge-response pairs in a secure database. Later, any suspect ICs taken from the market can be checked for proper registration.

Active approaches are designed to automatically lock each new IC that is manufactured by a foundry until it is unlocked (activated) by the authorized SoC designers, which can be efficiently implemented though logic obfuscation [29]. This is a technique where a design is transformed to a different one to obfuscate the inner details of the original design. Only on the application of a programmed secret key is the transformation reversed, thus preserving the original functionality. Roy et

al. first proposed to obfuscate a netlist by using a set of XOR/XNOR gates (lock) which can only be unlocked by using a key. Unfortunately, this design is not resistant to reverse engineering as the key controlled gates are directly related to their key bits (XOR and XNOR gates indicate 0 and 1 at the key location, respectively) and vulnerable to key sensitization attacks [36]. Rajendran et al. addressed these problems by improving the original obfuscation technique [36]. However, Subramanyan et al. have shown that the key in an activated circuit can always be exposed using scan based manufacturing tests by SAT-based analysis, no matter what preventive measures one takes [37]. Different approaches have been proposed till date to mitigate SAT based attacks [38] [39] [40].

In this paper, I will briefly describe a technique to establish forward trust proposed in [35] to prevent overproduced, cloned, and defective ICs, getting into the electronic supply chain.

IV. On-Chip Sensors for Counterfeit Detection

On-chip sensors are used to detect recycled ICs, those have been used in the field. Recycled ICs are characterized by aging, i.e., prior usage has taken its toll on the components' life and performance. A shift in the components' parameters due to aging will occur when they are used in the field for some time, which leads to the development of parametric defects and anomalies in the component. Aging of a component used in the field can be attributed to two major, distinct phenomena (which are becoming more prevalent as the technology scales down). They are negative-bias temperature instability (NBTI) [41], [42] and hot carrier injection (HCI) [43], [44] which are prominent in PMOS and NMOS devices, respectively. NBTI occurs in p-channel MOS devices stressed with negative gate voltages and elevated temperatures due to the generation of interface traps at the $Si{-}SiO_2$ interface. Removal of the stress can anneal some of the interface traps, but not completely. As a result, it manifests as the increase in threshold voltage (V_{th}) and absolute off current (I_{off}) and the decrease of absolute drain current (I_{DSat}) and transconductance (g_m). HCI occurs in NMOS devices caused by the trapped interface charge at $Si - SiO_2$ surface near the drain end during switching. It results in non-recoverable V_{th} degradation. These two aging mechanisms lead to the increased delay in the components' internal paths, which ultimately reduces the component's operating speed.

To detect recycled ICs, we need to design a sensor that can take advantage of aging very efficiently. As we all know NBTI is one the major source of aging, our objective is to design a sensor that can expedite aging. The NBTI-aware on chip sensor [25] (see Figure 3 for details), can efficiently detect recycled ICs with little misprediction (predict a new IC as recycled and vice versa) when the chips are aged for a short period of time. We call this sensor as Combating Die and IC Recycling (CDIR) sensors. However, when the workload decreases, we require the chips to be used much longer for detection, which eventually results in a higher rate

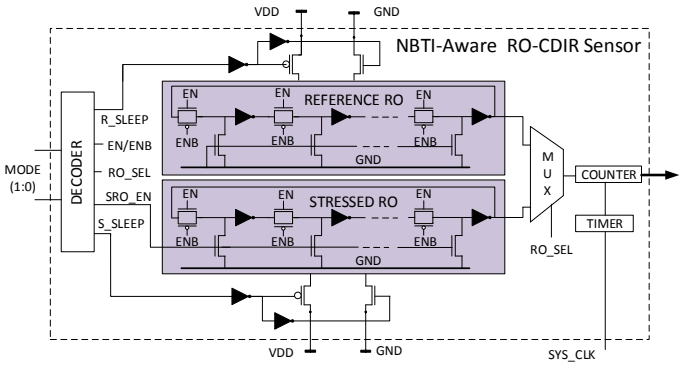

Figure 3: The NBTI-Aware RO-CDIR sensor [25]

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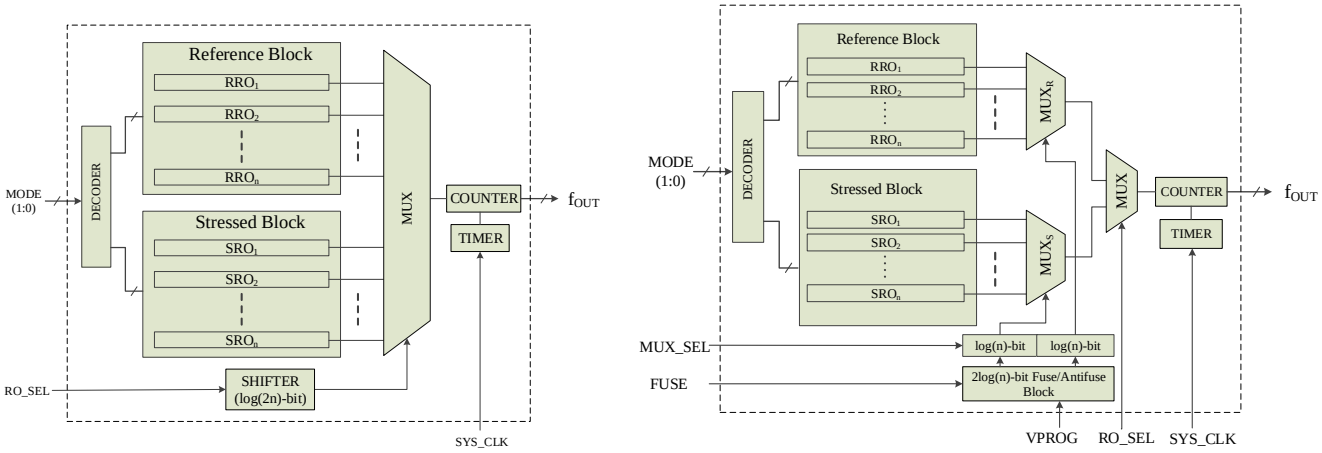
of misprediction. In addition, there may be a recycling activity from the overstock of electronic systems where the recyclers extract components from never used systems. The detection of these components can be performed with a CDIR that can detect a small amount of aging (for example, the amount of aging caused during the test of a system). When the application risk is critical [9] [6] [10], we do not have the luxury for any test escapes as the system failure due to using recycled chips could cause significant financial loss, as well as risks to safety and security. Thus, this necessitates further improvements of this simple CDIR.

To address these challenges, two different CDIR structures based on multiple ring oscillators have been proposed [26]. Here, we have multiple reference and stressed RO-pairs. An averaging approach was introduced to reduce the impact of process variations. This design provides a much better detection for ICs used for only few hours in the field with the cost of small misprediction. In addition, another modified design of multiple reference and stressed RO-pairs. In this case, a selection algorithm is used to find the best reference and stressed RO-pair. This CDIR with the best selected RO-pair, provides even better detection (no misprediction) of recycled ICs, even if they have been used only for a few hours, unlike the AN-CDIR. The details can be found in [26] [45].

V. Establishing Forward Trust for Counterfeit Avoidance

With increasing SoC design complexity, design reusability has become an integral part of the SoC design process, mainly to reduce manufacturing cost and time to market. Unfortunately, due to the lack of visibility and controllability of the manufacturing process, the trust becomes of the major concern among different entities in the semiconductor supply chain. An untrusted SoC designer can illegally use a third party IP in a different SoC and can also overuse it. In addition, SoC designers lose profits when an untrusted foundry or assembly overproduces chips and sells them under their name. Thus, forward trust is extremely important to the entities involved in the SoC design. Forward trust can be described as the trust on SoC designer from the IP owners, and foundry/assembly from the SoC designer/IP owners. Ensuring forward trust implies



(a) Multiple RO CDIR with averaging approach.

(b) Multiple RO CDIR with selection approach.

Figure 4: CDIR sensor with multiple ring oscillators [26].

that the IP owners does not need to trust the SoC designer, and SoC designers/IP owners to the foundries and assemblies. In this section, we present a comprehensive solution for establishing forward trust between the entities involved in SoC design and fabrication for protecting IPs and ICs.

Figure 5 shows the design flow for establishing forward trust between various entities involved with the SoC design process. The design flow is very similar to the existing IC design flow except for the lock insertion and functional activation steps. The design process starts with the insertion of locks by using a set of XOR/XNOR gates (we call them as key gates) using an existing secure logic encryption technique. The circuit produces functionally correct output when it receives a unlock key. The number of XOR or XNOR gates depends on the level of security one wants to achieve. It is important to enable manufacturing tests before the activation of chips.

Each 3PIP owner inserts key gates to lock their design and then generates test patterns. The SoC designer receives all these locked IPs and integrates them in the design. The SoC designer also inserts a lock in one of the in-house IP to protect against IC overproduction. The SoC designer collects all the test patterns from different IP owners and stores them in a pattern repository for future wafer and package tests.

The GDSII file corresponding to the SoC design is now sent to the foundry. The foundry first processes wafers, which generally contains hundreds of dies in a single wafer. Foundry then performs wafer test to inspect dies to find gross defects. If there are too many dies on a wafer that are defective, the foundry sometimes rejects the whole wafer. After wafer tests, the defect-free dies are sent to assembly for packaging. The good chips are then sorted out by using package tests and the chips that have been damaged during the packaging process are discarded. Finally, each chip is unlocked using the valid key by the entity who perform the final manufacturing test (foundry, assembly, or SoC designer) before supplied to the market. To protect this key from SoC designers, foundries and assemblies, a secure encrypted communication protocol is used. The interested readers can find more details in [35].

VI. Conclusion

Integrated circuits are becoming increasingly vulnerable to counterfeiting and piracy due to the lack of visibility and trust in the semiconductor manufacturing process. To address this trust issue, we have presented two different solutions for detecting the complete spectrum of counterfeit ICs to ensure the trustworthiness, security, and reliability of different ICs in the semiconductor supply chain.

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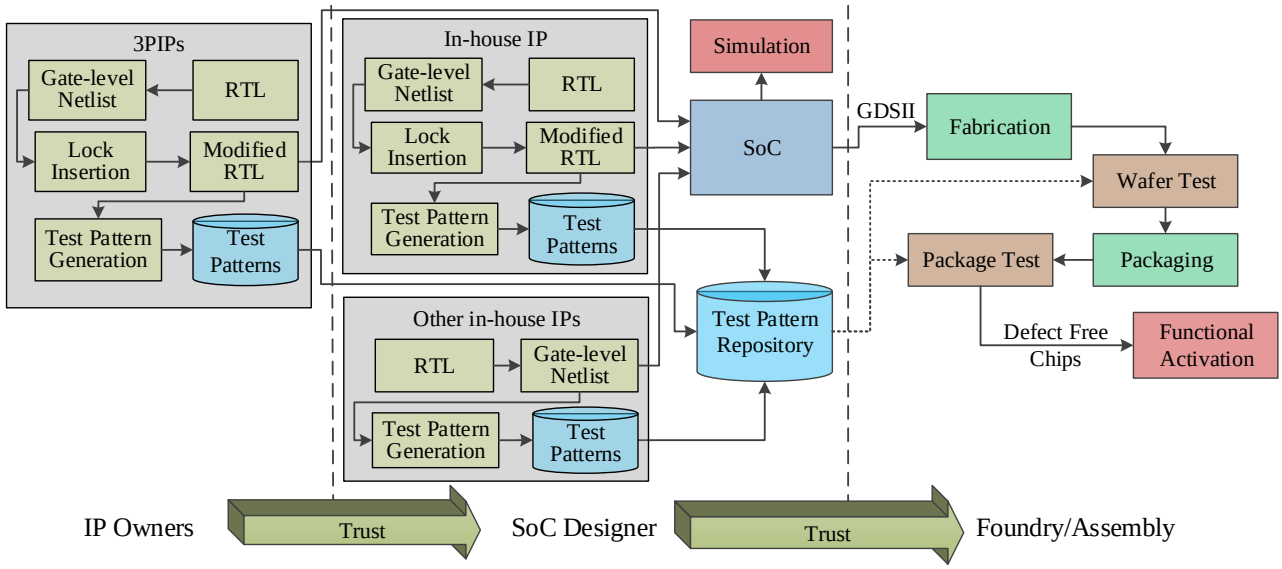

Figure 5: Flow for enabling forward trust in the SoC manufacturing process [35].

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