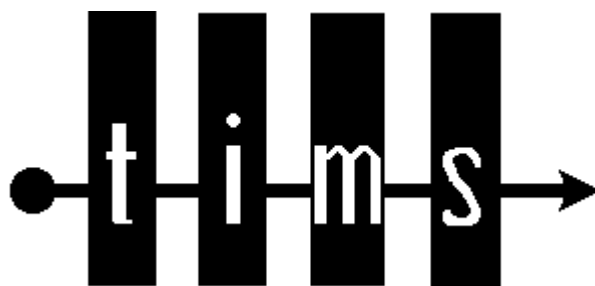


Communication Systems Modelling

with

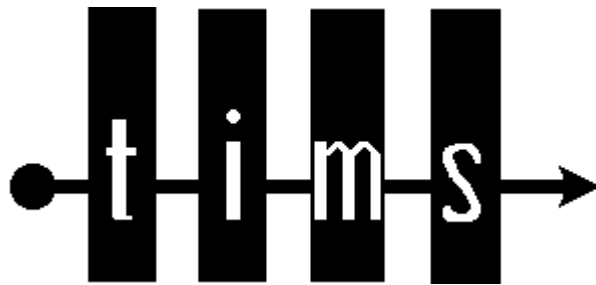


***Volume D1
Fundamental Digital
Experiments***

Tim Hooper

Communication Systems Modelling

with



Volume D1 Fundamental Digital Experiments

*Emona Instruments Pty Ltd
ABN 79 069-417-563
86 Parramatta Road
Camperdown NSW 2050
Sydney AUSTRALIA*



*is a registered trademark of
Amberley Holdings Pty Ltd
ACN 001-080-093
a company incorporated in
the State of NSW
AUSTRALIA*

WHAT IS TIMS ?

TIMS is a Telecommunications Instructional Modelling System. It models telecommunication systems.

Text books on telecommunications abound with block diagrams. These diagrams illustrate the subject being discussed by the author. Generally they are small sub-systems of a larger system. Their behaviour is described by the author with the help of mathematical equations, and with drawings or photographs of the signal waveforms expected to be present.

TIMS brings alive the block diagram of the text book with a working model, recreating the waveforms on an oscilloscope.

How can TIMS be expected to accommodate such a large number of models ?

There may be hundreds of block diagrams in a text book, but only a relatively few individual block *types*. These block diagrams achieve their individuality because of the many ways a relatively few element *types* can be connected in different *combinations*.

TIMS contains a collection of these block types, or *modules*, and there are very few block diagrams which it cannot model.

PURPOSE OF TIMS

TIMS can support courses in Telecommunications at all levels - from Technical Colleges through to graduate degree courses at Universities.

This text is directed towards using TIMS as support for a course given at any level of teaching.

Most early experiments are concerned with illustrating a small part of a larger system. Two or more of these sub-systems can be combined to build up a larger system.

The list of possible experiments is limitless. Each instructor will have his or her own favourite collection - some of them are sure to be found herein.

Naturally, for a full appreciation of the phenomena being investigated, there is no limit to the depth of mathematical analysis that can be undertaken. But most experiments can be performed successfully with

little or no mathematical support. It is up to the instructor to decide the level of understanding that is required.

EXPERIMENT AIMS

The experiments in this Volume are concerned with introductory digital communications.

The experiments have been written with the idea that each model examined could eventually become part of a larger telecommunications system, the aim of this large system being to transmit a *message* from input to output. The origin of this message (for the digital experiments in Volumes D1 and D2) is generally a pseudo random binary sequence. For the analog experiments (Volumes A1 and A2) it would ultimately be speech. But for test and measurement purposes a sine wave, or perhaps two sinewaves (as in the two-tone test signal) are generally substituted.

The experiments are designed to be completed in about two hours, with say one hour of preparation prior to the laboratory session.

The four Volumes of *Communication Systems Modelling with TIMS* are:

A1 - Fundamental Analog Experiments

A2 - Further & Advanced Analog Experiments

D1 - Fundamental Digital Experiments

D2 - Further & Advanced Digital Experiments

Contents

PRBS generation	1
Eye patterns	13
The noisy channel model.....	21
Detection with the DECISION MAKER	33
Line coding.....	41
ASK - amplitude shift keying.....	49
FSK - frequency shift keying.....	59
BPSK - binary phase shift keying	69
Signal constellations.....	79
Sampling with SAMPLE & HOLD.....	89
PCM encoding.....	97
PCM decoding.....	109
Delta modulation.....	121
Delta demodulation	135
Adaptive delta modulation	141
Delta-sigma modulation	149

PRBS GENERATION

PREPARATION	2
digital messages	2
random binary sequences	2
viewing	3
applications	4
bit clock acquisition	4
EXPERIMENT	4
the ‘snapshot’ display	4
band limiting	6
two generator alignment	7
two sequence alignment	8
the sliding window correlator	9
the model	10
TUTORIAL QUESTIONS	11
APPENDIX	12
PRBS generator - sequence length	12
error counting utilities - X-OR	12
TRUNKS	12

PRBS GENERATION

ACHIEVEMENTS: *introduction to the pseudo random binary sequence (PRBS) generator; time domain viewing: snap shot and eye patterns; two generator synchronization and alignment with the 'sliding window correlator'*

PREREQUISITES: *none*

EXTRA MODULES: *a second SEQUENCE GENERATOR, ERROR COUNTING UTILITIES.*

PREPARATION

digital messages

In analog work the standard test message is the sine wave, followed by the two-tone signal¹ for more rigorous tests. The property being optimized is generally signal-to-noise ratio (SNR). Speech is interesting, but does not lend itself easily to mathematical analysis, or measurement.

In digital work a binary sequence, with a known pattern of '1' and '0', is common. It is more common to measure bit error rates (BER) than SNR, and this is simplified by the fact that known binary sequences are easy to generate and reproduce.

A common sequence is the pseudo random binary sequence.

random binary sequences

The output from a pseudo random binary sequence generator is a bit stream of binary pulses; ie., a sequence of 1's (**HI**) or 0's (**LO**), of a *known* and *reproducible* pattern.

The bit *rate*, or number of bits per second, is determined by the frequency of an external *clock*, which is used to drive the generator. For each clock period a single

¹ see the experiment entitled *Amplifier overload* in Volume A2.

bit is emitted from the generator; either at the '1' or '0' level, and of a width equal to the clock period. For this reason the external clock is referred to as a *bit clock*.

For a long sequence the 1's and 0's are distributed in a (pseudo) random manner.

The sequence pattern *repeats* after a defined number of clock periods. In a typical generator the *length* of the sequence may be set to 2^n clock periods, where n is an integer. In the TMS SEQUENCE GENERATOR (which provides two, independent sequences, X and Y) the value of n may be switched to one of three values, namely 2, 5, or 11. There are *two* switch positions for the case $n = 5$, giving different patterns. The SYNCH output provides a reference pulse generated once per sequence repetition period.

This is *the start-of-sequence* pulse. It is *invaluable as a trigger source* for an oscilloscope.

viewing

There are two important methods of viewing a sequence in the time domain.

the snapshot

A short section, about 16 clock periods of a TTL sequence, is illustrated in Figure 1 below.

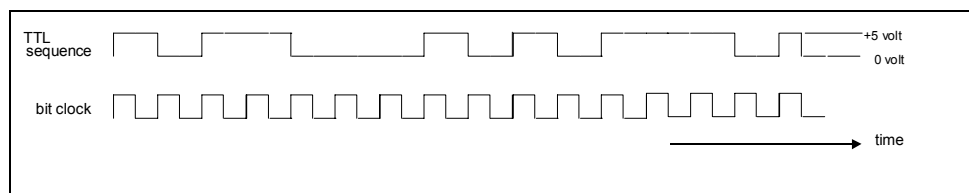


Figure 1: a sequence of length 16 bits

Suppose the output of the generator which produced the TTL sequence, of which this is a part, was viewed with an oscilloscope, with the horizontal sweep triggered by the display itself.

The display will not be that of Figure 1 above ! Of course not, for how would the oscilloscope know which section of the display was wanted ?

Consider just what the oscilloscope might show !

Specific sections of a sequence *can* be displayed on a general purpose oscilloscope, but the sequence generator needs to provide some help to do this.

As stated above, it gives a *start-of-sequence* pulse at the *beginning* of the sequence. This can be used to *start* (trigger) the oscilloscope sweep. At the end of the sweep the oscilloscope will wait until the next start-of-sequence is received before being triggered to give the next sweep.

Thus the beginning 'n' bits of the sequence are displayed, where 'n' is determined by the sweep speed.

For a sequence length of many-times-n bits, there would be a long delay between sweeps. The persistence of the screen of a general purpose oscilloscope would be

too short to show a steady display, so it will blink. You will see the effect during the experiment.

the eye pattern

A long sequence is useful for examining ‘eye patterns’. These are defined and examined in the experiment entitled *Eye patterns* in this Volume.

applications

One important application of the PRBS is for supplying a known binary sequence. This is used as a test signal (message) when making bit error rate (BER) measurements.

For this purpose a perfect *copy* of the *transmitted* sequence is required at the receiver, for direct comparison with the *received* sequence. This perfect copy is obtained from a second, identical, PRBS generator.

The second generator requires:

1. bit clock information, so that it runs at the same rate as the first
2. a method of aligning its output sequence with the received sequence. Due to transmission through a bandlimited channel, it will be delayed in time with respect to the sequence at the transmitter.

bit clock acquisition

In a laboratory environment it is a simple matter to use a ‘stolen carrier’ for bit clock synchronization purposes, and this will be done in most TIMS experiments. In commercial practice this bit clock must be regenerated from the received signal. Methods of bit clock recovery are investigated in a later experiment.

EXPERIMENT

the ‘snapshot’ display

Examine a SEQUENCE GENERATOR module, and read about it in the *TIMS User Manual*.

A suitable arrangement for the examination of a SEQUENCE GENERATOR is illustrated in Figure 2.

Notice that the length of the sequence is controlled by the settings of a DIP switch, SW2, *located on the circuit board*. See the Appendix to this experiment for details.

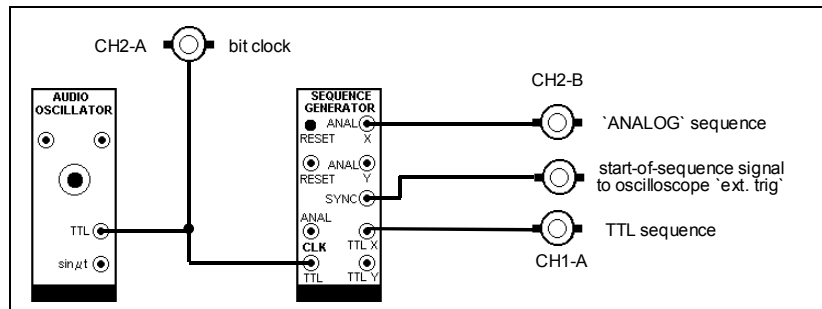


Figure 2: examination of a SEQUENCE GENERATOR

- T1** before inserting the SEQUENCE GENERATOR set the on-board DIP switch SW2 to generate a short sequence. Then patch up the model of Figure 2 above. Set the AUDIO OSCILLATOR, acting as the bit clock, to about 2 kHz. Set the oscilloscope sweep speed to suit; say about 1 ms/cm.
- T2** observe the TTL sequence on CH1-A. Try triggering the oscilloscope to the sequence itself (CH1-A). Notice that you may be able to obtain a stable picture, but it may change when the re-set button is pressed (this re-starts the sequence each time from the same point, referred to as the 'start of sequence').
- T3** try triggering off the bit clock. Notice that it is difficult (impossible ?) to obtain a stable display of the sequence.
- T4** change the mode of oscilloscope triggering. Instead of using the signal itself, use the start-of-sequence SYNC signal from the SEQUENCE GENERATOR, connected to 'ext. trig' of the oscilloscope. Reproduce the type of display of Figure 1 (CH1-A).
- T5** increase the sequence length by re-setting the on-board switch SW2. Re-establish synchronization using the start-of-sequence SYNC signal connected to the 'ext. trig' of the oscilloscope. Notice the effect upon the display. See Tutorial Question Q8.
- T6** have a look with your oscilloscope at a yellow analog output from the SEQUENCE GENERATOR. The DC offset has been removed, and the amplitude is now suitable for processing by analog modules (eg., by a filter representing an analog channel - see the experiment entitled **The noisy channel model** in this Volume). Observe also that the polarity has been reversed with respect to the TTL version. This is just a consequence of the internal circuitry; if not noticed it can cause misunderstandings !

band limiting

The displays you have seen on the oscilloscope are probably as you would have expected them to be ! That is, either 'HI' or 'LO' with sharp, almost invisible, transitions between them. This implies that there was no band limiting between the signal and the viewing instrument.

If transmitted via a lowpass filter, which could represent a bandlimited (baseband) channel, then there will be some modification of the shape, as viewed in the time domain.

For this part of the experiment you will use a TUNEABLE LPF to limit, and vary, the bandwidth. Because the sequence will be going to an analog module it will be necessary to select an 'analog' output from the SEQUENCE GENERATOR.

T7 select a short sequence from the SEQUENCE GENERATOR.

T8 connect an analog version of the sequence (YELLOW) to the input of a TUNEABLE LPF.

T9 on the front panel of the TUNEABLE LPF set the toggle switch to the WIDE position. Obtain the widest bandwidth by rotating the TUNE control fully clockwise.

T10 with the oscilloscope still triggered by the 'start-of-sequence' SYNC signal, observe both the filter input and output on separate oscilloscope channels. Adjust the gain control on the TUNEABLE LPF so the amplitudes are approximately equal.

T11 monitor the filter corner frequency, by measuring the CLK signal from the TUNEABLE LPF with the FREQUENCY COUNTER ². Slowly reduce the bandwidth, and compare the difference between the two displays. Notice that, with reducing bandwidth:

a) identification of individual bits becomes more difficult

b) there is an increasing delay between input and output

Remember that the characteristics of the filter will influence the results of the last Task.

² divide by 880 (normal) or 360 (wide). For detail see the TIMS User Manual.

two generator alignment

In an experiment entitled *BER measurement in the noisy channel* (within *Volume D2 - Further & Advanced Digital Experiments*) you will find out *why* it is important to be able to align two sequences. In this experiment you will find out *how* to do it.

Two SEQUENCE GENERATOR modules may be coupled so that they deliver two identical, *aligned*, sequences.

- that they should deliver the *same sequence* it is sufficient that the generator circuitry be identical
- that they be at the *same rate* it is necessary that they share a common bit clock
- that they be *aligned* requires that they start at the same time.

TIMS SEQUENCE GENERATOR modules (and those available commercially) have inbuilt facilities to simplify the alignment operation. One method will be examined with the scheme illustrated in block diagram form in Figure 3 below.

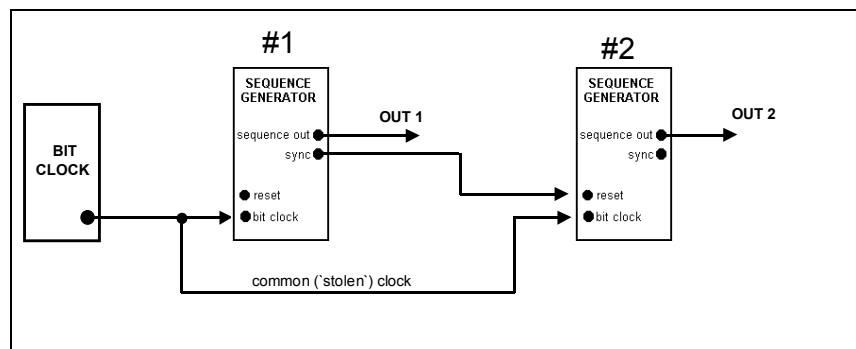


Figure 3: aligning two identical generators

The scheme of Figure 3 is shown modelled with TIMS in Figure 4 below.

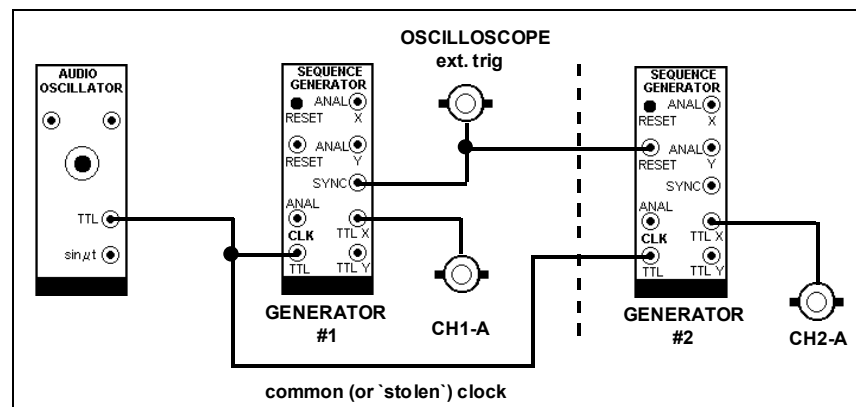


Figure 4: TIMS model of the block diagram of Figure 3.

You will now investigate the scheme. Selecting short sequences will greatly assist during the setting-up procedures, by making the viewing of sequences on the oscilloscope much easier.

T12 before plugging in the SEQUENCE GENERATOR modules, set them both to the same short sequence.

T13 patch together as above, but omit the link from the 'GENERATOR #1' SYNC to 'GENERATOR #2' RESET. Do not forget to connect the 'start-of-sequence' SYNC signal of the GENERATOR #1 to the 'ext. trig' of the oscilloscope.

T14 press the 'GENERATOR #2' RESET push button several times. Observe on the oscilloscope that the two output sequences are synchronised in time but the data bits do not line-up correctly. Try to synchronise the sequences manually by repeating this exercise many times. It is a hit-and-miss operation, and is likely to be successful only irregularly.

*T15 connect the SYNC of the 'GENERATOR #1' to the RESET of the 'GENERATOR #2'. Observe on the oscilloscope that the two output sequences are now synchronised in time and their data are **aligned**.*

T16 break the synchronizing path between the two generators. What happens to the alignment ?

*Once the two generators are aligned, **they will remain aligned**, even after the alignment link between them is broken. The bit clock will keep them in step.*

The above scheme has demonstrated a method of aligning two generators, and was seen to perform satisfactorily. But it was in a somewhat over simplified environment.

What if the two generators had been separated some distance, with the result that there was a delay between sending the SYNC pulse from GENERATOR #1 and its reception at GENERATOR #2 ?

The sequences would be offset by the time delay

In other words, the sequences would *not* be aligned.

two sequence alignment

In the previous section two PRBS generators were synchronized in what might be called a 'local' situation. There were two signal paths between them:

1. one connection for the bit clock
2. another connection for the start-of-sequence command

Consider a transmitter and a receiver separated by a transmission medium. Then:

1. there would be an inevitable transmission time delay
2. the two signal paths are not conveniently available

It may be difficult (impossible ?) to align the two generators, at remote sites. But it is possible, and frequently required, that a local *generator* can be aligned with a received *sequence* (from a similar generator).

The *sliding window correlator* is an example of an arrangement which can achieve this end.

the sliding window correlator

Consider the arrangement shown in block diagram form in Figure 5 below.

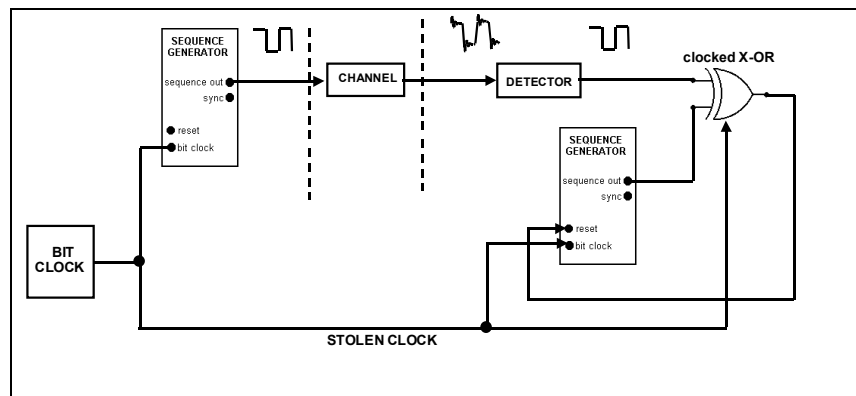


Figure 5 - the sliding window correlator

The detector is present to re-generate TTL pulses from the bandlimited received signal. We will assume this regeneration is successful.

The regenerated received sequence (which matches, but is a delayed version of the transmitted sequence) is connected to one input of a clocked X-OR logic gate.

The receiver PRBS generator (using a stolen bit clock in the example) is set to generate the same sequence as its counterpart at the transmitter. Its output is connected to the other input of the clocked X-OR gate. The clock ensures that the comparison is made at an appropriate instant within a bit clock period.

At each bit clock period there is an output from the X-OR gate only if the bits differ. In this case the receiver generator will be *RESET to the beginning of the sequence*.

This resetting will take place repeatedly until there are no errors. Thus every bit must be aligned. There will then be no further output from the X-OR gate.

*Once alignment has been achieved, it will be **maintained** even when the RESET signal to the receiver generator is broken.*

It is the common bit clock which maintains the alignment. Because of the nature of this X-OR comparison technique the arrangement is called a *sliding window correlator*.

the model

You will now model the block diagram of Figure 5. In later experiments you will meet the channel and the detector, but in this experiment we will omit them both. Thus there will in fact be no delay, *but that does not in any way influence the operation of the sliding window correlator*.

The patching arrangement to model Figure 5 is shown in Figure 6 below.

This model will regenerate, at the receiver, an identical sequence to that sent from the transmitter. To avoid additional complications a stolen carrier is used.

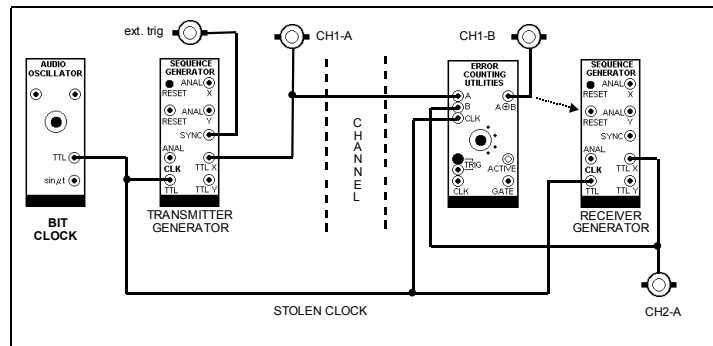


Figure 6: modelling the sliding window correlator

T17 before patching up select the shortest length sequence on each SEQUENCE GENERATOR.

T18 patch together as above. Do not close the link from the X-OR output of the ERROR COUNTING UTILITIES³ module to the RESET of the RECEIVER GENERATOR.

T19 view CH1-A and CH2-A simultaneously. The two output sequences are synchronised in time but the data bits are probably not aligned. Press the RESET push button of the RECEIVER GENERATOR repeatedly. Notice that once in a while it is possible to achieve alignment. With a longer sequence this would be a rare event indeed.

T20 switch to CH1-B; observe the error sequence produced by the X-OR operation on the two data sequences.

T21 now close the alignment link by connecting the error signal at the X-OR output to the RESET input of the RECEIVER GENERATOR.

³ see the Appendix to this experiment for some information about the ERROR COUNTING UTILITIES module.

T22 confirm that the error sequence is now zero. Confirm that, if the RESET push button of the RECEIVER GENERATOR is repeatedly pressed, the error signal appears for a short time and then disappears.

T23 repeat the previous Task with a long sequence. Note that the system takes a longer time to acquire alignment.

T24 having achieved alignment, disconnect the error signal from the RESET input of the RECEIVER GENERATOR, and observe that the two sequences remain in alignment.

Future experiments will assume familiarity with the operation of the SEQUENCE GENERATOR, and the alignment of two sequences using the *sliding window correlator*. So, before you finish this experiment, make sure you have looked at as many aspects of this arrangement as you have time for.

TUTORIAL QUESTIONS

Q1 you have seen the first 'n' bits of a sequence, using the start-of-sequence signal to initiate the oscilloscope sweep. How could you show the next 'n' bits of the same sequence? Can you demonstrate your method with TIMS?

Q2 estimate the bandwidth of the sequence as a function of bit rate clock frequency. Describe a method for estimating the maximum rate at which a binary sequence can be transmitted through a lowpass filter. Relate its predictions with your observations.

Q3 explain what is meant when two sequences are 'synchronized' and 'aligned'.

Q4 was there any obvious misalignment between the TTL sequence input to, and the bandlimited sequence output from, the TUNEABLE LPF? Explain.

Q5 in the last model examined, explain why the sequence alignment takes longer when the sequence length is increased.

Q6 suppose the TIMS SEQUENCE GENERATOR is driven by an 8.333 kHz TTL clock. What would the TIMS FREQUENCY COUNTER read if connected to the output sequence? Explain.

Q7 what should an rms meter read if connected to a TTL pseudo random binary sequence?

Q8 with a 2.083 kHz clock what is the delay, for a 2048 bit sequence, between consecutive displays?

APPENDIX

PRBS generator - sequence length

The length of the sequences from the SEQUENCE GENERATOR can be set with the DIP switch SW2 located *on the circuit board*.

See Table A-1 below.

<i>LH toggle</i>	<i>RH toggle</i>	<i>n</i>	<i>sequence length</i>
UP	UP	5	32
UP	DOWN	8	256
DOWN	UP	8	256
DOWN	DOWN	11	2048

Table A-1: on-board switch SW2 settings

There are two sequences of length 256 bits. These sequences are different.

error counting utilities - x-or

This is the first time the ERROR COUNTING UTILITIES module has been used. It contains two independent sub-systems, only one of which (X-OR) is required in this experiment.

A complete description of its characteristics and behaviour can be obtained from the *TIMS Advanced Modules User Manual*.

A condensed description of the X-OR function, suitable for this experiment, is given in the experiment entitled *Digital utility sub-systems* (within *Volume D2 - Further & Advanced Digital Experiments*), under the heading *Exclusive-OR*.

EYE PATTERNS

PREPARATION	14
pulse transmission	14
maximum transmission rate assessment.....	15
EXPERIMENT	16
snap-shot assessment.....	17
eye pattern assessment.....	17
your conclusions.....	19
TUTORIAL QUESTIONS	20

EYE PATTERNS

ACHIEVEMENTS: *understanding the Nyquist I criterion; transmission rates via bandlimited channels; comparison of the 'snap shot' display with the 'eye patterns'.*

PREREQUISITES: *some acquaintance with basic notions of digital transmission*

ADVANCED MODULES: *BASEBAND CHANNEL FILTERS*

PREPARATION

pulse transmission

It is well known that, when a signal passes via a bandlimited channel it will suffer waveform distortion. As an example, refer to Figure 1. As the data rate increases the waveform distortion increases, until transmission becomes impossible.

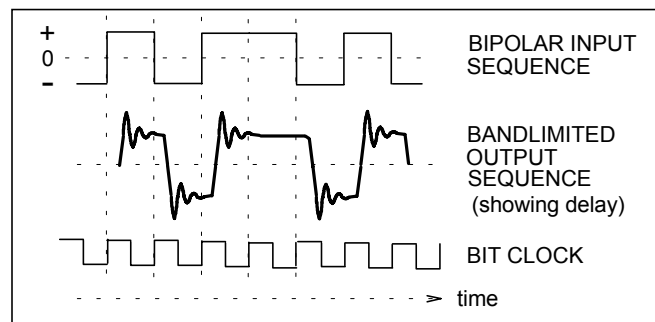


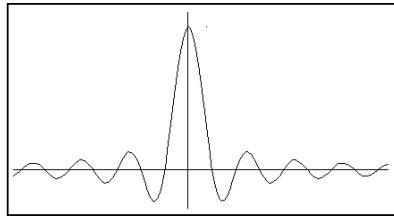
Figure 1: waveforms before and after moderate bandlimiting

In this experiment you will be introduced to some important aspects of pulse transmission which are relevant to digital and data communication applications.

Issues of interest include:

- In the 1920s Harry Nyquist proposed a clever method now known as Nyquist's first criterion, that makes possible the transmission of telegraphic signals over channels with limited bandwidth without degrading signal

quality. This idea has withstood the test of time. It is very useful for digital and data communications.



The method relies on the exploitation of pulses that look like $\sin(x)/x$ - see the Figure opposite. The trick is that zero crossings always fall at equally spaced points. Pulses of this type are known as 'Nyquist I' (there is also Nyquist II and III).

- In practical communication channels distortion causes the dislocation of the zero crossings of Nyquist pulses, and results in *intersymbol interference* (ISI) ¹. Eye patterns provide a practical and very convenient method of assessing the extent of ISI degradation. A major advantage of eye patterns is that they can be used 'on-line' in real-time. There is no need to interrupt normal system operation.
- The effect of ISI becomes apparent at the receiver when the incoming signal has to be 'read' and decoded; ie., a detector decides whether the value at a certain time instant is, say, 'HI' or 'LO' (in a binary decision situation). A decision error may occur as a result of noise. Even though ISI may not itself cause an error in the absence of noise, it is nevertheless undesirable because it decreases the margin relative to the decision threshold, ie., a given level of noise, that may be harmless in the absence of ISI, may lead to a high error rate when ISI is present.
- Another issue of importance in the decision process is *timing jitter*. Even if there is no ISI at the nominal decision instant, timing jitter in the reconstituted bit clock results in decisions being made too early or too late relative to the ideal point. As you will discover in this experiment, channels that are highly bandwidth efficient are more sensitive to timing jitter.

maximum transmission rate assessment

This is what is going to be done:

1. first, set up a pseudorandom sequence. To start you will use the shortest available sequence, so that you can easily observe it with an oscilloscope. Very long sequences are not easy to observe because the time elapsed between trigger pulses is too long. The oscilloscope will be triggered to the start of sequence signal. The display has been defined as a 'snap shot' ².
2. next you will pass this sequence through a selection of filters. Three are available in the BASEBAND CHANNEL FILTERS module, and a fourth will be the TUNEABLE LPF module. You will observe the effect of the filters on the shape of the sequence, at various pulse rates.
3. then the above observations will be repeated, but this time the oscilloscope will be triggered by the bit clock, giving what is defined as an *eye pattern*.
4. finally you will compare the performance of the various cases in terms of achievable transmission rate and 'eye opening'.

¹ ie., 'inter-pulse' interference.

² see the experiment entitled *PRBS generation*.

EXPERIMENT

T1 set up the model of Figure 2. The AUDIO OSCILLATOR serves as the bit clock for the SEQUENCE GENERATOR. A convenient rate to start with is 2 kHz. Select CHANNEL #1. Select a short sequence (both toggles of the on-board switch SW2 UP)

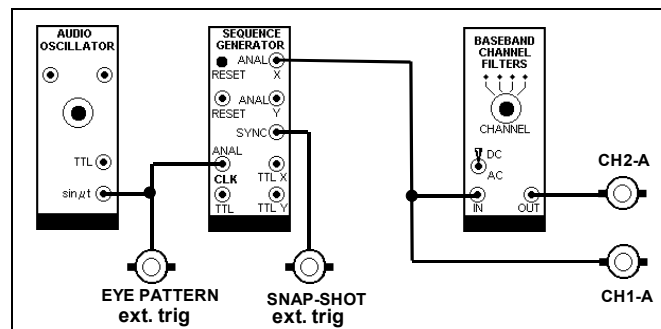


Figure 2: viewing snap shots and eye patterns

T2 synchronize the oscilloscope to the 'start-of-sequence' synchronizing signal from the SEQUENCE GENERATOR. Set the sweep speed to display between 10 and 20 sequence pulses (say 1 ms/cm). This is the 'snap shot' mode. Both traces should be displaying the same picture, since CHANNEL #1 is a 'straight through' connection.

The remaining three channels (#2, #3, and #4) in the BASEBAND CHANNEL FILTERS module represent channels having the same slot bandwidth³ (40 dB stopband attenuation at 4 kHz), but otherwise different transmission characteristics, and, in particular, different 3 dB frequencies. Graphs of these characteristics are shown in Appendix A.

You should also prepare a TUNEABLE LPF to use as a fourth channel, giving it a 40 dB attenuation at 4 kHz. To do this:

T3 using a sinusoidal output from an AUDIO OSCILLATOR as a test input:

a) set the TUNE and GAIN controls of the TUNEABLE LPF fully clockwise. Select the NORM bandwidth mode.

³ see Appendix A to Volume A1 for a definition of slotband.

- b) set the AUDIO OSCILLATOR to a frequency of, say, 1 kHz. This is well within the current filter passband.*
- c) note the output amplitude on the oscilloscope.*
- d) increase the frequency of the AUDIO OSCILLATOR to 4 kHz.*
- e) reduce the bandwidth of the TUNEABLE LPF (rotate the TUNE control anti-clockwise) until the output amplitude falls 100 times. This is a 40 dB reduction relative to the passband gain.*

snap-shot assessment

Now it is your task to make an assessment of the maximum rate, controlled by the frequency of the AUDIO OSCILLATOR, at which a sequence of pulses can be transmitted through each filter before they suffer unacceptable distortion. The criterion for judging the maximum possible pulse rate will be your opinion that you can recognise the output sequence as being similar to that at the input.

It is important to remember that the four filters have the same *slot bandwidth* (ie., 4 kHz, where the attenuation is 40 dB) but different *3 dB bandwidths*.

To relate the situation to a practical communication system you should consider the filters to represent the total of all the filtering effects at various stages of the transmission chain, ie., transmitter, channel, and the receiver right up to the input of the decision device.

T4 record your assessment of the maximum practical data rate through each of the four channels.

At the very least your report will be a record of the four maximum transmission rates. But it is also interesting to compare these rates with the characteristics of the filters. Perhaps you might expect the filter with the widest passband to provide the highest acceptable transmission rate ?

eye pattern assessment

Now you will repeat the previous exercise, but, instead of observing the sequence as a single trace, you will use *eye patterns*. The set-up will remain the same except for the oscilloscope usage and sequence length.

So far you have used a short sequence, since this was convenient for the snapshot display. But for eye pattern displays a longer sequence is preferable, since this generates a greater number of patterns. Try it.

*T5 change the oscilloscope synchronizing signal from the **start-of-sequence SYNC** output of the SEQUENCE GENERATOR to the sequence **bit clock**. Increase the sequence length (both toggles of the on-board switch SW2 DOWN). Make sure the oscilloscope is set to pass DC. Why ? Try AC coupling, and see if you notice any difference.*

T6 select CHANNEL #2. Use a data rate of about 2 kHz. You should have a display on CH2-A similar to that of Figure 3 below.

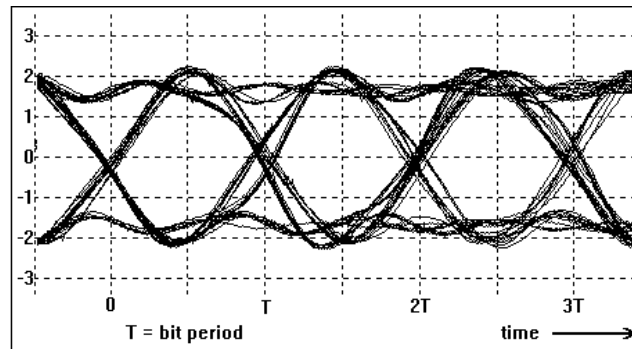


Figure 3: a 'good' eye pattern

T7 increase the data rate until the eye starts to close. Figure 4 shows an eye not nearly as clearly defined as that of Figure 3.

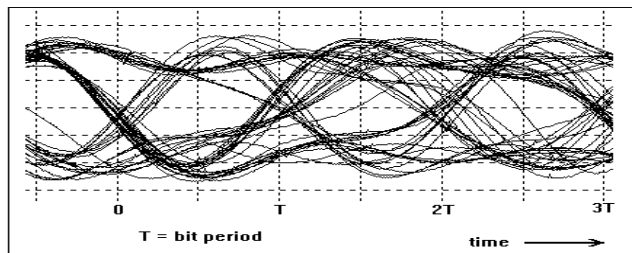


Figure 4: compare with Figure 3; a faster data rate

T8 take some time to examine the display, and consider what it is you are looking at ! There is one 'eye' per bit period. Those shown in Figure 3 are considered to be 'wide open'. But as the data rate increases the eye begins to close.

The actual shape of an eye is determined (in a linear system) primarily by the filter (channel) amplitude and phase characteristics (for a given input waveform).

Timing jitter will have an influence too. See the experiment entitled *Bit clock regeneration* (within *Volume D2 - Further & Advanced Digital Experiments*).

The detector must make a decision, at an appropriate moment in the bit period, as to whether or not the signal is above or below a certain voltage level. If above it decides the current bit is a HI, otherwise a LO. By studying the eye you can make that decision. Should it not be made at the point where the eye is wide open, clear of any trace ? The moment when the vertical opening is largest ?

You can judge, by the thickness of the bunch of traces at the top and bottom of the eye, compared with the vertical opening, the degree-of-difficulty in making this decision.

T9 *determine the highest data rate for which you consider you would always be able to make the correct decision (HI or LO). Note that the actual moment to make the decision will be the same for all bits, and relatively easy to distinguish. Record this rate for each of the four filters.*

You have now seen two different displays, the snapshot and the eye pattern.

It is generally accepted that the eye pattern gives a better indication of the appropriate instant the HI or LO decision should be made, and its probable success, than does the snapshot display. Do you agree ?

Noise and other impairments will produce the occasional transition which will produce a trace within the apparently trace-free eye. This may not be visible on the oscilloscope, but will none-the-less cause an error. Turning up the oscilloscope brilliance may reveal some of these transitions.

Such a trace is present in the eye pattern of Figure 4.

An oscilloscope, with storage and other features (including in-built signal analysis !), will reveal even more information.

It does not follow that the degradation of the eye worsens as the clock rate is increased. Filters can be designed for optimum performance at a specific clock rate, and performance can degrade if the clock rate is increased *or* reduced.

The present experiment was aimed at giving you a 'feel' and appreciation of the technique in a non-quantitative manner.

In later experiments you will make quantitative measurements of error rates, as data is transmitted through these filters, with added noise.

your conclusions

Theory predicts a maximum transmission rate of 2 pulses per Hz of baseband bandwidth available. On the basis of your results, what do you think ?

TUTORIAL QUESTIONS

- Q1** explain why it is important to have the oscilloscope switched to 'DC' when viewing eye patterns. Explain the meaning, and possible causes of, 'baseline wander'.*
- Q2** why have the filters in the BASEBAND CHANNEL FILTERS module got common slotband widths (instead, for example, of having common passband widths) ?*
- Q3** why would a storage oscilloscope provide a more reliable eye pattern display ?*
- Q4** why is a long sequence preferable for eye pattern displays ?*
- Q5** how would timing jitter show up in an eye pattern ?*

THE NOISY CHANNEL MODEL

PREPARATION	22
lowpass (or baseband) channels	22
bandpass channels	22
over simplification	23
noise	23
the noisy channel model	23
diagrammatic representation	24
channel gain	25
noise level	25
revision	26
EXPERIMENT	26
filter amplitude response	26
signal to noise ratio	28
speech-plus-noise	30
group delay	31
TUTORIAL QUESTIONS	31

THE NOISY CHANNEL MODEL

ACHIEVEMENTS: *definition of the macro CHANNEL MODEL module. Ability to set up a noisy bandlimited channel for subsequent experiments; measurement of filter characteristics; measurement of signal-to-noise ratio with the WIDEBAND TRUE RMS METER. Observation of different levels of signal-to-noise ratio with speech.*

PREREQUISITES: *none*

EXTRA MODULES: *WIDEBAND TRUE RMS METER, NOISE GENERATOR, BASEBAND CHANNEL FILTERS module; 100 kHz CHANNEL FILTERS module optional.*

PREPARATION

Since TMS is about modelling communication systems it is not surprising that it can model a communications channel.

Two types of channels are frequently required, namely *lowpass* and *bandpass*.

lowpass (or baseband) channels

A *lowpass* channel by definition should have a bandwidth extending from DC to some upper frequency limit. Thus it would have the characteristics of a lowpass filter.

A speech channel is often referred to as a lowpass channel, although it does not necessarily extend down to DC. More commonly it is called a *baseband* channel.

bandpass channels

A *bandpass* channel by definition should have a bandwidth covering a range of frequencies not including DC. Thus it would have the characteristics of a bandpass filter.

Typically its bandwidth is often much less than an octave, but this restriction is not mandatory. Such a channel has been called narrow band.

Strictly an analog voice channel is a bandpass channel, rather than lowpass, as suggested above, since it does not extend down to DC. So the distinction between baseband and bandpass channels can be blurred on occasion.

Designers of active circuits often prefer bandpass channels, since there is no need to be concerned with the minimization of DC offsets.

For more information refer to the chapter entitled *Introduction to modelling with TMS*, within *Volume A1 - Fundamental Analog Experiments*, in the section entitled 'bandwidths and spectra'.

over simplification

The above description is an oversimplification of a practical system. It has concentrated all the bandlimiting in the channel, and introduced no intentional pulse shaping. In practice the bandlimiting, and pulse shaping, is distributed between filters in the transmitter and the receiver, and the channel itself. The transmitter and receiver filters are designed, knowing the characteristics of the channel. The signal reaches the detector having the desired characteristics.

noise

Whole books have been written about the analysis, measurement, and optimization of signal-to-noise ratio (SNR).

SNR is usually quoted as a power ratio, expressed in decibels. But remember the measuring instrument in this experiment is an *rms voltmeter*, not a *power* meter. See Tutorial Question Q6.

Although, in a measurement situation, it is the magnitude of the ratio S/N which is commonly sought, it is more often the $\frac{(S+N)}{N}$ which is available. In other words, in a non-laboratory environment, if the signal is present then so is the noise; the signal is not available alone.

In this, and most other laboratory environments, the noise is under our control, and can be removed if necessary. So that $\left(\frac{S}{N}\right)$, rather than $\frac{(S+N)}{N}$, can be measured directly.

For high SNRs there is little difference between the two measures.

the noisy channel model

A representative noisy, bandlimited channel model is shown in block diagram form in Figure 1 of the following page.

Band limitation is implemented by any appropriate filter.

The noise is added before the filter so that it becomes bandlimited by the same filter that band limits the signal. If this is not acceptable then the adder can be moved to the output of the filter, or perhaps the noise can have its own bandlimiting filter.

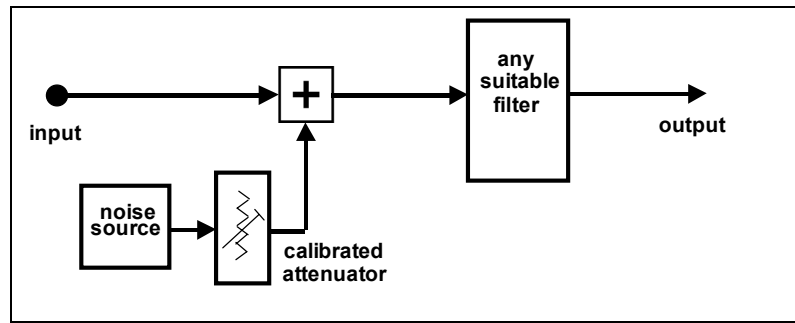


Figure 1: channel model block diagram

Controllable amounts of random noise, from the noise source, can be inserted into the channel model, using the calibrated attenuator. This is non signal-dependent noise.

For lowpass channels lowpass filters are used.

For bandpass channels bandpass filters are used.

Signal dependent noise is typically introduced by channel non-linearities, and includes intermodulation noise between different signals sharing the channel (cross talk). Unless expressly stated otherwise, in TIMS experiments signal dependent noise is considered negligible. That is, the systems must be operated under *linear* conditions. An exception is examined in the experiment entitled *Amplifier overload* (within *Volume A2 - Further & Advanced Analog Experiments*).

diagrammatic representation

In patching diagrams, if it is necessary to save space, the noisy channel will be represented by the block illustrated in Figure 2 below.

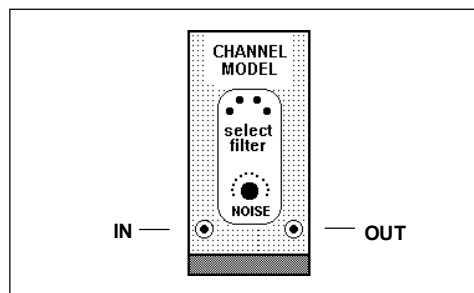


Figure 2: the macro CHANNEL MODEL module

Note it is illustrated as a channel model *module*. Please do not look for a physical TIMS module when patching up a system with this *macro module* included. This macro module is modelled with five *real* TIMS modules, namely:

1. an INPUT ADDER module.
2. a NOISE GENERATOR module.
3. a bandlimiting module. For example, it could be:
 - a. any single filter module; such as a TUNEABLE LPF (for a baseband channel).

- b. a BASEBAND CHANNEL FILTERS module, in which case it contains three filters, as well as a direct through connection. Any of these four paths may be selected by a front panel switch. Each path has a gain of unity. This module can be used in a *baseband* channel. The filters all have the same *slot* bandwidth (40 dB at 4 kHz), but differing passband widths and phase characteristics.
- c. a 100 kHz CHANNEL FILTERS module, in which case it contains two filters, as well as a direct through connection. Any of these three paths may be selected by a front panel switch. Each path has a gain of unity. This module can be used in a *bandpass* channel.

Definition of filter terms, and details of each filter module characteristic, are described in Appendix A to this text.

4. an OUTPUT ADDER module, not shown in Figure 1, to compensate for any accumulated DC offsets, or to match the DECISION MAKER module threshold.
5. a source of DC, from the VARIABLE DC module. This is a *fixed module*, so does not require a slot in the system frame.

Thus the CHANNEL MODEL is built according to the patching diagram illustrated in Figure 3 below, and (noting *item 5* above) requires *four* slots in a system unit.

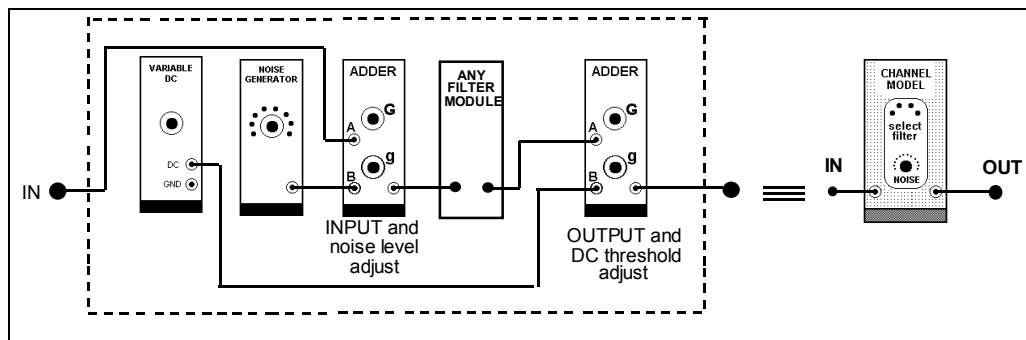


Figure 3: details of the macro CHANNEL MODEL module

channel gain

Typically, in a TIMS model, the gain through the channel would be set to unity. This requires that the upper gain control, 'G', of both ADDER modules, be set to unity. Both the BASEBAND CHANNEL FILTER module and the 100 kHz CHANNEL FILTER module have fixed gains of unity. If the TUNEABLE LPF is used, then its adjustable gain must also be set to about unity.

However, in particular instances, these gains may be set otherwise.

noise level

The noise level is adjusted by both the lower gain control 'g' of the INPUT ADDER, and the front panel calibrated attenuator of the NOISE GENERATOR module. Typically the gain would be set to zero [g fully anti-clockwise] until noise is required. Then the general noise level is set by g, and *changes* of precise magnitude introduced by the calibrated attenuator.

Theory often suggests to us the means of making small improvements to SNR in a particular system. Although small, they can be of value, especially when combined

with other small improvements implemented elsewhere. An improvement of 6 dB in received SNR can mean a doubling of the range for reception from a satellite, for example.

revision

You should look now at the Tutorial Questions, as important preparation for the experiment.

EXPERIMENT

filter amplitude response

These days even the most modest laboratory is equipped with computer controlled apparatus which makes the measurement of a filter response in a few seconds, and provides the output result in great detail. At the very least this is in the form of amplitude, phase, and group delay responses in both soft and hard copy.

It is instructive, however, to make at least one such measurement using what might be called ‘first principles’. In this experiment you will make a measurement of the amplitude-versus-frequency response of one of the BASEBAND CHANNEL FILTERS.

A typical measurement arrangement is illustrated in Figure 4 below.

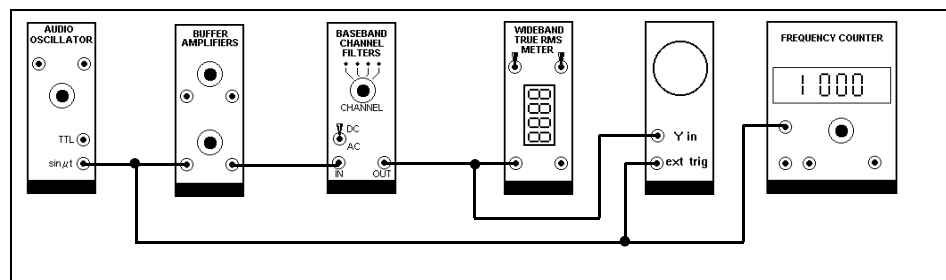


Figure 4: measurement of filter amplitude response

In the arrangement of Figure 4:

- the audio oscillator provides the input to the filter, at the TMS ANALOG REFERENCE LEVEL, and over a frequency range suitable for the filter being measured.
- the BUFFER allows fine adjustment of the signal amplitude into the filter. It is always convenient to make the measurement with a constant amplitude signal at the input to the device being measured. The TMS AUDIO OSCILLATOR

output amplitude is reasonably constant as the frequency changes, but should be monitored in this sort of measurement situation.

- the filter can be selected from the three in the module by the front panel switch (positions #2, #3, and #4). Each has a gain in the passband of around unity. Remember there is a 'straight through' path - switch position #1.
- the WIDEBAND TRUE RMS METER will measure the amplitude of the output voltage
- the FREQUENCY COUNTER will indicate the frequency of measurement
- the OSCILLOSCOPE will monitor the output waveform. With TMS there is unlikely to be any overloading of the filter if analog signals remain below the TMS ANALOG REFERENCE LEVEL; but it is always a good idea in a less controlled situation to keep a constant check that the analog system is operating in a linear manner - not too big and not too small an input signal. This is not immediately obvious by looking at the WIDEBAND TRUE RMS METER reading alone (see Tutorial Q2). Note that the oscilloscope is externally triggered from the constant amplitude source of the input signal.

The measuring procedure is:

***T1** decide upon a frequency range, and the approximate frequency increments to be made over this range. A preliminary sweep is useful. It could locate the corner frequency, and the frequency increments you choose near the corner (where the amplitude-frequency change is fastest) could be closer together.*

***T2** set the AUDIO OSCILLATOR frequency to the low end of the sweep range. Set the filter input voltage to a convenient value using the BUFFER AMPLIFIER. A round figure is often chosen to make subsequent calculations easier - say 1 volt rms. Note that the input voltage can be read, without the need to change patching leads, by switching the front panel switch on the BASEBAND CHANNEL FILTERS module to the straight-through condition - position #1. Record the chosen input voltage amplitude.*

***T3** switch back to the chosen filter, and record the output voltage amplitude and the frequency*

***T4** tune to the next frequency. Check that the input amplitude has remained constant; adjust, if necessary, with the BUFFER AMPLIFIER. Record the output voltage amplitude and the measurement frequency.*

***T5** repeat the previous Task until the full frequency range has been covered.*

The measurements have been recorded. The next step is usually to display them graphically. This you might like to do using your favourite software graphics package. But it is also instructive - at least once in your career - to make a plot by hand, since, instead of some software deciding upon the axis ranges, you will need to make this decision yourself !

Conventional engineering practice is to plot amplitude in decibels on a linear scale, and to use a logarithmic frequency scale. Why ? See Tutorial Question **Q1**.

A decibel amplitude scale requires that a reference voltage be chosen. This will be your recorded input voltage. Since the response curve is shown as a ratio, there is no way of telling what this voltage was from most response plots, so it is good practice to note it somewhere on the graph.

T6 make a graph of your results. Choose your scales wisely. Compare with the theoretical response (in Appendix A).

signal to noise ratio

This next part of the experiment will introduce you to some of the problems and techniques of signal-to-noise ratio measurements.

The maximum output amplitude available from the NOISE GENERATOR is about the TIMS ANALOG REFERENCE LEVEL when measured over a wide bandwidth - that is, wide in the TIMS environment, or say about 1 MHz. This means that, as soon as the noise is bandlimited, as it will be in this experiment, the rms value will drop significantly ¹.

You will measure both $\left(\frac{S}{N}\right)$, (ie, SNR) and $\frac{(S+N)}{N}$, and compare calculations of one from a measurement of the other.

The uncalibrated gain control of the ADDER is used for the adjustment of noise level to give a specific SNR. The TIMS NOISE GENERATOR module has a calibrated attenuator which allows the noise level to be *changed in small calibrated steps*.

Within the test set up you will use the macro CHANNEL MODEL module already defined. It is shown embedded in the test setup in Figure 5 below.

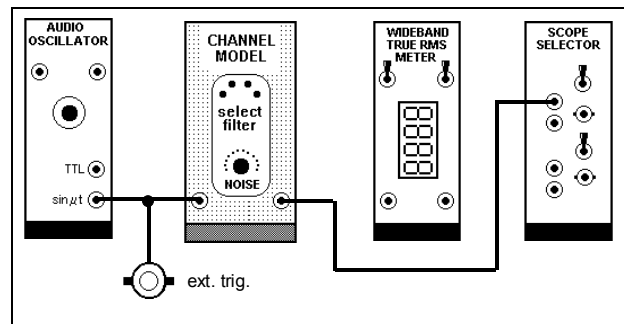


Figure 5: measurement of signal-to-noise ratio

As in the filter response measurement, the oscilloscope is not essential, but certainly good practice, in an analog environment. It is used to monitor waveforms, as a check that overload is not occurring.

The oscilloscope display will also give you an appreciation of what signals look like with random noise added.

¹ to overcome the problem the noise could first be bandlimited, then amplified

T7 set up the arrangement of Figure 5 above. Use the channel model of Figure 3. In this experiment use a BASEBAND CHANNEL FILTERS module (select, say, filter #3).

You are now going to set up independent levels of signal and noise, as recorded by the WIDEBAND TRUE RMS METER., and then predict the meter reading when they are present together. After bandlimiting there will be only a small rms noise voltage available, so this will be set up first.

T8 reduce to zero the amplitude of the sinusoidal signal into the channel, using the 'G' gain control of the INPUT ADDER.

T9 set the front panel attenuator of the NOISE GENERATOR to maximum output.

T10 adjust the gain control 'g' of the INPUT ADDER to maximum. Adjust the 'G' control of the OUTPUT ADDER for about 1 volt rms. Record the reading. The level of signal **into** the BASEBAND CHANNEL FILTERS module may exceed the TIMS ANALOG REFERENCE LEVEL, and be close to overloading it - but we need as much noise out as possible. If you suspect overloading, then reduce the noise 2 dB with the attenuator, and check that the expected change is reflected by the rms meter reading. If not, use the INPUT ADDER to reduce the level a little, and check again.

Before commencing the experiment proper have a look at the noise alone; first wideband, then filtered.

T11 switch the BASEBAND CHANNEL FILTERS module to the straight-through connection - switch position #1. Look at the noise on the oscilloscope.

T12 switch the BASEBAND CHANNEL FILTERS module to any or all of the lowpass characteristics. Look at the noise on the oscilloscope.

Probably you saw what you expected when the channel was not bandlimiting the noise - an approximation to wideband white noise.

But when the noise was severely bandlimited there is quite a large change. For example:

- a. the amplitude dropped significantly. Knowing the filter bandwidth you could make an estimate of the noise bandwidth before bandlimiting ?
- b. the appearance of the noise in the time domain changed quite significantly. You might like to repeat the last two tasks, using different sweep speeds, and having a closer look at the noise under these two different conditions.

Record your observations. When satisfied:

- T13 reduce to zero the amplitude of the noise into the channel by removing its patch cord from the INPUT ADDER, thus not disturbing the ADDER adjustment.*
- T14 set the AUDIO OSCILLATOR to any convenient frequency within the passband of the channel. Adjust the gain 'G' of the INPUT ADDER until the WIDEBAND TRUE RMS METER reads the same value as it did earlier for the noise level.*
- T15 turn to your note book, and calculate what the WIDEBAND TRUE RMS METER will read when the noise is reconnected.*
- T16 replace the noise patch cord into the INPUT ADDER. Record what the meter reads.*
- T17 calculate and record the signal-to-noise ratio in dB.*
- T18 measure the signal-plus-noise, then the noise alone, and calculate the SNR in dB. Compare with the result of the previous Task.*
- T19 increase the signal level, thus changing the SNR. Measure both $\left(\frac{S}{N}\right)$, and $\frac{(S+N)}{N}$, and predict each from the measurement of the other. Repeat for different SNR.*

speech-plus-noise

It is interesting to listen to speech corrupted by noise. You will be able to obtain a qualitative idea of various levels of signal-to-noise ratios.

- T20 obtain speech either from TRUNKS or a SPEECH MODULE. Listen to it using the HEADPHONE AMPLIFIER alone. Switch the in-built LPF in and out and observe any change of the speech quality. Comment. The filter has a cut-off of 3 kHz - confirm this by measurement.*
- T21 pass the speech through the macro CHANNEL MODEL module, using the BASEBAND CHANNEL FILTERS module as the band limiter. Add noise and observe, qualitatively, the sound of different levels of signal-to-noise ratio.*
- T22 what can you say about the intelligibility of the speech when corrupted by noise? If you are using bandlimited speech, but wideband noise, you can make observations about the effect upon intelligibility of restricting the noise to the same bandwidth as the speech. Do this, and report your conclusions.*

T23 how easy is it to measure the signal power, when it is speech ? Comment.
Remember: it is easy to introduce a precise change to the SNR (how ?), but with speech the measurement of absolute level of SNR is not as straightforward as with a sinusoidal message.

group delay

How might you have measured, or estimated, or at least demonstrated the existence of, a time delay through any of the filters ?

hint: try using the SEQUENCE GENERATOR on a short sequence.

TUTORIAL QUESTIONS

Q1 when plotting filter amplitude responses it is customary to use decibel scales for the amplitude, versus a logarithmic frequency scale. Discuss some of the advantages of this form of presentation over alternatives.

Q2 an analog channel is overloaded with a single sinewave test signal. Is this always immediately obvious if examined with an oscilloscope ?

Is it obvious with:

- a) a single measurement using a voltmeter ?
- b) two or more measurements with a voltmeter ?

Explain you answers to (a) and (b).

Q3 suppose an rms voltmeter reads 1 volt at the output of a noisy channel when the signal is removed from the input. What would it read if the bandwidth was halved ? State any assumptions which were necessary for this answer.

Q4 a sinusoidal waveform has a peak-to-peak amplitude of 5 volts. What is its rms value ?

Q5 what would an rms meter read if connected to a square wave:

- a) alternating between 0 and 5 volt ?
- b) alternating between ± 5 volt ?

Q6 the measuring instrument used in this experiment was an rms volt meter. Could you derive a conversion factor so that the instrument could be used as a direct reading (relative) power meter ?

Q7 suppose a meter is reading 1 volt rms on a pure tone. Wideband noise is now added until the meter reading increases by 10%.

- a: what would be the signal-to-noise ratio in dB ?
- b: what would the rms volt meter read on noise alone ?
This answer is meant to show that measuring small changes to signal-to-noise ratios is difficult unless the signal-to-noise ratio is already small. Do you agree ?
How small ² ?

Q8 wideband white noise is passed through a lowpass filter to a meter. If the filter bandwidth is decreased by one half, what would be the change of the reading of the meter if:

- a) it responds to power - answer in dB
- b) it is a true rms volt meter - give the percent change

Q9 explain how you might measure, or at least demonstrate the existence of, a time delay through any of the filters ?

² this is a value judgement, so answers may vary between your colleagues. But it is not 40 dB, for example. Do you agree ?

DETECTION WITH THE DECISION MAKER

PREPARATION	34
EXPERIMENT	36
the test signal	36
signal regeneration	37
using the COMPARATOR	38
signal levels	38
DC threshold	38
using the DECISION MAKER:	38
error counting	40
summing up	40
TUTORIAL QUESTIONS	40

DETECTION WITH THE DECISION MAKER

ACHIEVEMENTS: familiarization with the *DECISION MAKER* module, to be used in later experiments. Demonstration of the superiority of a gated detector compared with a simple comparator.

PREREQUISITES: familiarity with the *SEQUENCE GENERATOR* and eye patterns; completion of the experiment entitled **PRBS generation** in this Volume.

EXTRA MODULES: *DECISION MAKER*.

PREPARATION

The shape of a binary sequence waveform is affected by transmission through a noisy, bandlimited channel. Since the aim of a transmission system is to deliver a perfect copy of the input to the output, the received sequence needs to be restored to its original shape, or *regenerated*.

The regeneration process is performed by what we will call a *detector*.

You should refer to your text book to see the wide range of circuits which has been devised for performing this regeneration process, from the simple amplitude limiter, or the comparator, to extremely sophisticated and intelligent schemes.

As an example of moderate wave shaping, refer to Figure 1, which shows the waveshape changes suffered by a sequence after passage through a bandlimited channel.

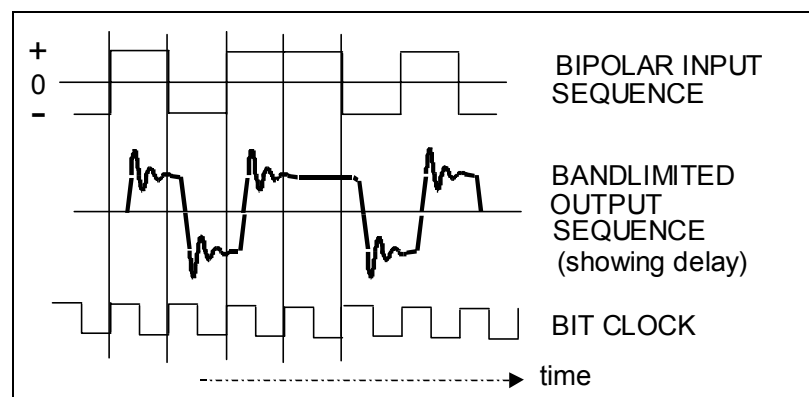


Figure 1: waveforms before and after moderate bandlimiting

If the bandlimited bipolar output waveform of Figure 1 is connected to a comparator, whose reference is zero volts, then the output will be HI (say +V volt) whilst the waveform is above zero volts, and LO (say -V volt) when it is below. Visual inspection leads us to believe that it is unlikely the comparator would make any mistakes. Examination of the eye pattern of the same waveform would confirm this.

If there was noise, and perhaps further bandlimiting, the comparator would eventually start to fail. But other, more sophisticated circuits, operating on the same waveform, might still succeed in regenerating a perfect copy of the original.

To be fair to the comparator, it is competent to decide whether the signal is *above* (a HI), or *below* (a LO) a reference. Provided the signal-to-noise ratio (SNR) is not too low then this will be during the HI and LO bits. As the SNR reduces the comparator output may not match favourably the input, especially as regards pulse width. Finally its performance as a *detector* will deteriorate, and extra pulses (or 'bits') will appear, as indicated in Figure 2 below. But note that it is still operating faithfully as a *comparator*.

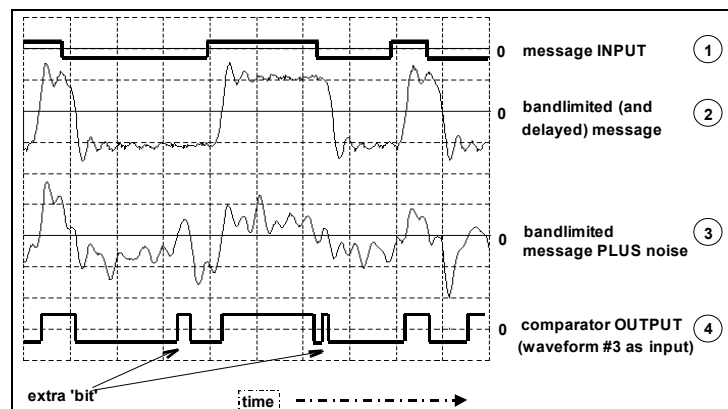


Figure 2: deterioration of comparator output with noise.

Additional circuitry, using the bit clock as a guide, could be implemented to restore the bit width of the regenerated sequence. This, and more, has been done with the TIMS DECISION MAKER.

The DECISION MAKER is fed a copy of the corrupted sequence, and also a copy of the bit clock. It examines the incoming sequence at a specified *instant* within each bit period. This best *sampling instant* may be chosen by you, after inspection of the eye pattern. With additional external circuitry, this could be automated, or made adaptive.

The DECISION MAKER makes its decision at the instant you have specified within each bit period, and outputs either a HI or a LO. It makes each HI or LO last for a bit period. It also outputs a new bit clock, shifted in time relative to the input bit clock, so that the new clock is aligned with the regenerated bit stream.

The sampling instant, specified by you in this experiment, is set by a front panel control, and is indicated on the oscilloscope waveform by a high intensity spot. The appropriate waveform to be viewing, when selecting the sampling instant, is the *eye pattern*.

For more details about the DECISION MAKER module refer to the ***TIMS User Manual***. You will have an opportunity to become acquainted with it in this experiment. Please note that the circuitry of the DECISION MAKER has been optimized for a clock rate in the region of 2 kHz, so it is unwise to use it at clock rates too far removed from this.

EXPERIMENT

You will examine the decision process applied to a noisy bandlimited bipolar waveform using two methods: a basic COMPARATOR (ungated), and the TIMS DECISION MAKER module. In later experiments you will count actual errors, but in this experiment evaluation will be by visual comparison of the device output and the original sequence.

the test signal

The test signal will come from a SEQUENCE GENERATOR via a noisy, bandlimited channel. The bandlimiting of the channel will be adjustable. This is illustrated in block form in Figure 3 below.

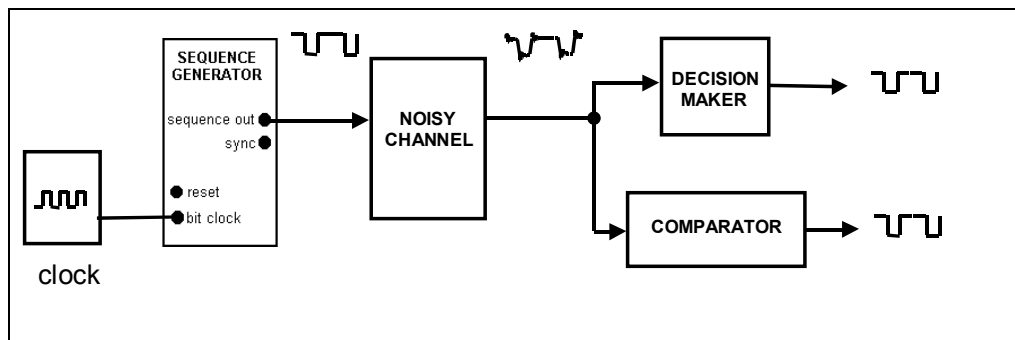


Figure 3: system to demonstrate sequence regeneration

A model of the block diagram of Figure 3 is shown in Figure 4 below. It uses the macro CHANNEL MODEL module.

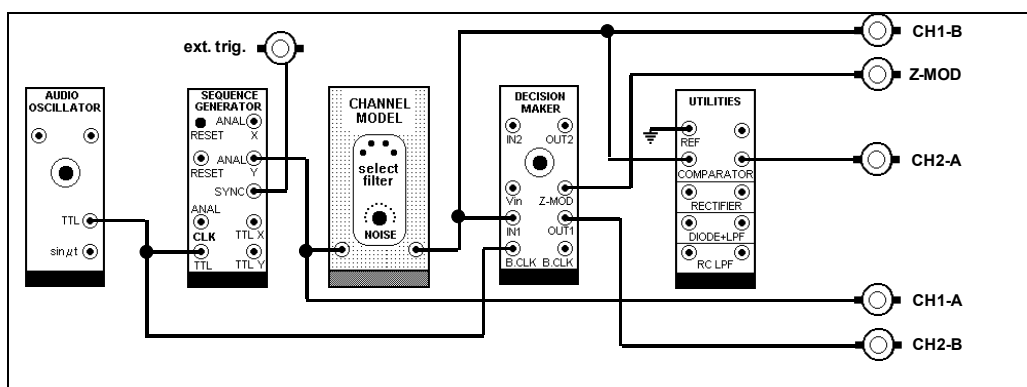


Figure 4: the COMPARATOR and DECISION MAKER as regenerators

The macro CHANNEL MODEL module was introduced in the experiment entitled *The noisy channel model* (within this Volume). It is used for inserting noise, bandlimiting, and adjusting signal levels. As a reminder the model is reproduced here as Figure 5. To provide an adjustable bandwidth, it uses the TUNEABLE LPF as the bandlimiting module.

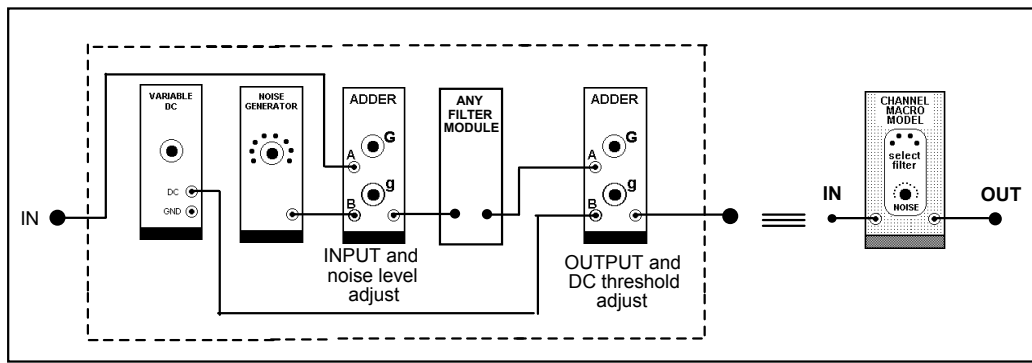


Figure 5: details of the macro CHANNEL MODEL module

signal regeneration

First patch up the complete system, according to the block diagram of Figure 3, shown modelled in Figure 4.

note that:

- for selecting the best sampling instant the *eye pattern* is preferred. The oscilloscope is triggered externally by the bit clock.
- to check, visually, that the recovered sequence is error free, you need the *snapshot*. The oscilloscope is triggered externally by the SYNC pulse of the SEQUENCE GENERATOR.

Ideally, for *visual* evaluation, the first of these requires a *long* sequence, and the second a *short* sequence. For convenience, however, you may find it acceptable to use *short* sequence for both observations.

T1 before plugging in the SEQUENCE GENERATOR module select the minimum length sequence with the on-board switch SW2 (both toggles UP).

T2 model the complete system illustrated in Figure 4, except for the DECISION MAKER.

T3 set the AUDIO OSCILLATOR to about 2 kHz. This will suit the DECISION MAKER, which has been designed for operation with clock rates of this order.

T4 ensure the oscilloscope is triggering on the SYNC signal from the SEQUENCE GENERATOR. Check the sequence on CH1-A.

using the COMPARATOR

T5 set the TUNEABLE LPF to its widest bandwidth. Check the signal on CH1-B is roughly of the same shape as shown in Figure 1. The COMPARATOR should have no trouble regenerating this sequence.

T6 check the COMPARATOR output against the original sequence by looking at CH1-A and CH2-A simultaneously. Satisfy yourself that regeneration is acceptable.

T7 now carry out some observations of the COMPARATOR output as either or both the channel bandwidth is varied and noise is added. Get some appreciation of the limitations of the COMPARATOR as a regenerator.

signal levels

No mention was made above about the signal levels at the various interfaces. You should be experienced enough now to realize how important these are. Although this may seem to be a *digital-style* experiment, most of the modules are processing *analog-level* signals. So the signal levels at their (yellow) interfaces should be adjusted appropriately. That is, they should be at about the TIMS ANALOG REFERENCE LEVEL, or 4 volt peak-to-peak. Check back that this was achieved.

DC threshold

You can investigate the purpose of the DC threshold adjustment provided in the CHANNEL MODEL. Slowly reduce the channel output amplitude, whilst monitoring the COMPARATOR output. Eventually, as the signal amplitude is progressively decreased, the COMPARATOR output will be all HI or all LO. Fine adjustment of the DC level from the channel ¹ will re-position the sequence with respect to the COMPARATOR reference level (nominally zero, or ground) and allow operation for even smaller input levels.

using the DECISION MAKER:

T8 read about the DECISION MAKER module in the TIMS User Manual. Before plugging it in, ensure that:

a) the on-board switch SW2 is switched to 'INT'

b) the 'NRZ-L' waveform is selected with on-board switch SW1 (upper rear of board). This configures the DECISION MAKER to

¹ set the gain 'g' of the ADDER to some small, finite value, and use the VARIABLE DC front panel control to adjust the voltage. This allows a finer adjustment.

accept bipolar non-return-to-zero waveforms, as you have from the analog output of the SEQUENCE GENERATOR.

T9 *change the oscilloscope triggering, and display an eye pattern.*

T10 *patch the DECISION MAKER into the system, including the Z-MOD connection to the oscilloscope.*

T11 *rotate the front panel DECISION POINT control knob of the DECISION MAKER. There should be a highlighted point moving across both oscilloscope traces. If the spot cannot be seen, try varying the oscilloscope intensity control. If still no spot, seek help from your Laboratory Manager. As a last resort (!) refer to the **TIMS User Manual** and the oscilloscope User Manual. There are settings on the DECISION MAKER circuit board to suit most oscilloscopes, and once set (by the Laboratory Manager) they require no further adjustment.*

note: *make sure a TTL bit clock is connected to B.CLK in.*

T12 *locate the high intensity spot on the oscilloscope display. This shows the sampling instant.*

T13 *adjust the front panel control of the DECISION MAKER so that the sampling instant is positioned at the best decision point within the bit period; ie, where the vertical eye opening is greatest.*

T14 *the regenerated sequence will be displayed on CH2-B. Compare it with the input sequence on CH1-A. There will, of course, be a time offset between the two, due to the delay introduced by the filter, and the regeneration process itself.*

Note that the DECISION MAKER provides a new bit clock, aligned with the regenerated sequence. This is essential for later processing of the regenerated sequence (eg, by the error counter - see later).

You will now make some more demanding tests of the DECISION MAKER.

Changing from one display to the other involves a little more than changing the connection to the **ext trig** of the oscilloscope, as generally the sweep speed needs some slight adjustment. Ideally, also, the snapshot needs a short sequence, and the eye a long sequence. But for these tests a short sequence should be acceptable for both.

What you will have to do, each time you make a test, is:

1. lower the bandwidth a little
2. re-position the sampling instant
3. check the sequences for equality

You can develop your own visual scheme for comparing sequences.

T15 now carry out some observations of the DECISION MAKER output, as you did for the COMPARATOR output, as either or both the channel bandwidth is varied and noise is added. Get some idea of the performance of the DECISION MAKER, as compared with that of the simple COMPARATOR, as a regenerator.

error counting

During the above observations you may have been saying ‘*there must be a better way to judge performance ?*’ And, of course, there is !

A visual check for errors provides a quick method for comparing short sequences, but it is a qualitative check only; something quantitative is then required for serious measurements.

More systematic methods are introduced in the experiment entitled *BER measurement in the noisy channel* in Volume D2 - *Further and Advanced Digital Experiments*.

summing up

The DECISION MAKER module will be used in many more experiments, so it is important to have a good understanding of its capabilities and limitations.

TUTORIAL QUESTIONS

Q1 explain why a strobed decision process can be expected to result in a lower incidence of errors, compared to an ungated (instantaneous) comparator.

Q2 familiarize yourself with the terms ‘timing jitter’ and ‘baseline wander’. Explain, via the eye pattern, how these affect the satisfactory operation of the detection device.

Q3 in this experiment we use a ‘stolen clock’ to generate the strobe clock at the receiver. Refer to your text book and describe the essence of a clock recovery process in a commercial application.

LINE CODING

PREPARATION	42
why line coding ?	42
the modules	43
terminology	44
available line codes	44
NRZ-L	44
NRZ-M	44
UNI-RZ	45
BIP-RZ	45
RZ-AMI	45
Bi ϕ -L	45
DICODE-NRZ	45
band limiting	46
duobinary encoding	46
EXPERIMENT	47
procedure	47
TUTORIAL QUESTIONS	48

LINE CODING

ACHIEVEMENTS: familiarity with the properties of the LINE-CODE ENCODER and LINE-CODE DECODER modules, and the codes they generate.

PREREQUISITES: an appreciation of the purpose behind line coding.

EXTRA MODULES: LINE-CODE ENCODER and LINE-CODE DECODER

PREPARATION

This ‘experiment’ is tutorial in nature, and serves to introduce two new modules.

In your course work you should have covered the topic of line coding at what ever level is appropriate for you. TMS has a pair of modules, one of which can perform a number of line code transformations on a binary TTL sequence. The other performs decoding.

why line coding ?

There are many reasons for using line coding. Each of the line codes you will be examining offers one or more of the following advantages:

spectrum shaping and relocation without modulation or filtering. This is important in telephone line applications, for example, where the transfer characteristic has heavy attenuation below 300 Hz.

bit clock recovery can be simplified.

DC component can be eliminated; this allows AC (capacitor or transformer) coupling between stages (as in telephone lines). Can control baseline wander (baseline wander shifts the position of the signal waveform relative to the detector threshold and leads to severe erosion of noise margin).

error detection capabilities.

bandwidth usage; the possibility of transmitting at a higher rate than other schemes over the same bandwidth.

At the very least the LINE-CODE ENCODER serves as an interface between the TTL level signals of the transmitter and those of the analog channel. Likewise, the

LINE-CODE DECODER serves as an interface between the analog signals of the channel and the TTL level signals required by the digital receiver.

the modules

The two new modules to be introduced are the LINE-CODE ENCODER and the LINE-CODE DECODER.

You will not be concerned with how the coding and decoding is performed.

You should examine the waveforms, using the original TTL sequence as a reference.

In a digital transmission system line encoding is the final digital processing performed on the signal before it is connected to the analog channel, although there may be simultaneous bandlimiting and wave shaping.

Thus in TIMS the LINE-CODE ENCODER accepts a TTL input, and the output is suitable for transmission via an analog channel.

At the channel output is a signal at the TIMS ANALOG REFERENCE LEVEL, or less. It could be corrupted by noise. Here it is re-generated by a *detector*. The TIMS detector is the DECISION MAKER module (already examined in the experiment entitled *Detection with the DECISION MAKER* in this Volume). Finally the TIMS LINE-CODE DECODER module accepts the output from the DECISION MAKER and decodes it back to the binary TTL format.

Preceding the line code encoder may be a source encoder with a matching decoder at the receiver. These are included in the block diagram of Figure 1, which is of a typical baseband digital transmission system. It shows the disposition of the LINE-CODE ENCODER and LINE-CODE DECODER. All bandlimiting is shown concentrated in the channel itself, but could be distributed between the transmitter, channel, and receiver.

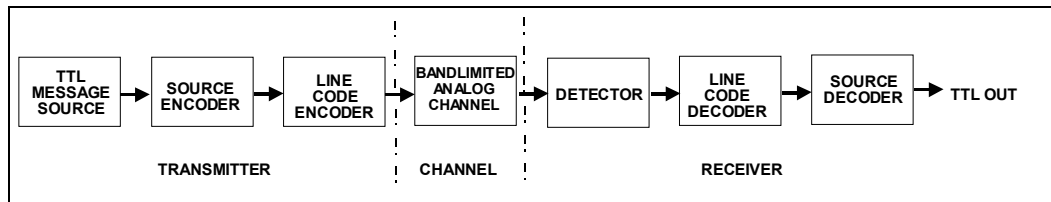


Figure 1: baseband transmission system

The LINE-CODE ENCODER serves as a source of the system bit clock. It is driven by a *master clock* at 8.333 kHz (from the TIMS MASTER SIGNALS module). It divides this by a factor of four, in order to derive some necessary internal timing signals at a rate of 2.083 kHz. This then becomes a convenient source of a 2.083 kHz TTL signal for use as the *system bit clock*.

Because the LINE-CODE DECODER has some processing to do, it introduces a time delay. To allow for this, it provides a re-timed clock if required by any further digital processing circuits (eg, for decoding, or error counting modules).

terminology

- the word *mark*, and its converse *space*, often appear in a description of a binary waveform. This is an historical reference to the mark and space of the telegraphist. In modern day digital terminology these have become HI and LO, or '1' and '0', as appropriate.
- *unipolar signalling*: where a '1' is represented with a finite voltage V volts, and a '0' with zero voltage. This seems to be a generally agreed-to definition.
- those who treat *polar* and *bipolar* as identical define these as signalling where a '1' is sent as +V, and '0' as -V. They append AMI when referring to three-level signals which use +V and -V alternately for a '1', and zero for '0' (an alternative name is pseudoternary).

You will see the above usage in the *TIMS Advanced Modules User Manual*, as well as in this text.

However, others make a distinction. Thus:

- *polar signalling*: where a '1' is represented with a finite voltage +V volts, and a '0' with -V volts.
- *bipolar signalling*: where a '1' is represented alternately by +V and -V, and a '0' by zero voltage.
- the term 'RZ' is an abbreviation of 'return to zero'. This implies that the particular waveform will return to zero for a finite part of each data '1' (typically half the interval). The term 'NRZ' is an abbreviation for 'non-return to zero', and this waveform will not return to zero during the bit interval representing a data '1'.
- the use of 'L' and 'M' would seem to be somewhat illogical (or inconsistent) with each other. For example, see how your text book justifies the use of the 'L' and the 'M' in NRZ-L and NRZ-M.
- two sinusoids are said to be antipodal if they are 180^0 out of phase.

available line codes

For a TTL input signal the following output formats are available from the LINE-CODE ENCODER.

NRZ-L

Non return to zero - level (bipolar): this is a simple scale and level shift of the input TTL waveform.

NRZ-M

Non return to zero - mark (bipolar): there is a transition at the beginning of each '1', and no change for a '0'. The 'M' refers to 'inversion on mark'. This is a

differential code. The decoder will give the correct output independently of the polarity of the input.

UNI-RZ

Uni-polar - return to zero (uni-polar): there is a half-width output pulse if the input is a '1'; no output if the input is a '0'. This waveform has a significant DC component.

BIP-RZ

Bipolar return to zero (3-level): there is a half-width +ve output pulse if the input is a '1'; or a half-width -ve output pulse if the input is a '0'. There is a return-to-zero for the second half of each bit period.

RZ-AMI

Return to zero - alternate mark inversion (3-level): there is a half-width output pulse if the input is a '1'; no output if the input is a '0'. This would be the same as UNI-RZ. But, *in addition*, there is a polarity inversion of every alternate output pulse.

Bi ϕ -L

Biphase - level (Manchester): bipolar $\pm V$ volts. For each input '1' there is a transition from +V to -V in the middle of the bit-period. For each input '0' there is a transition from -V to +V in the middle of the bit period.

DICODE-NRZ

Di-code non-return to zero (3-level): for each transition of the input there is an output pulse, of opposite polarity from the preceding pulse. For no transition between input pulses there is no output.

The codes offered by the line-code encoder are illustrated in Figure 2 below. These have been copied from the *Advanced Module Users Manual*, where more detail is provided.

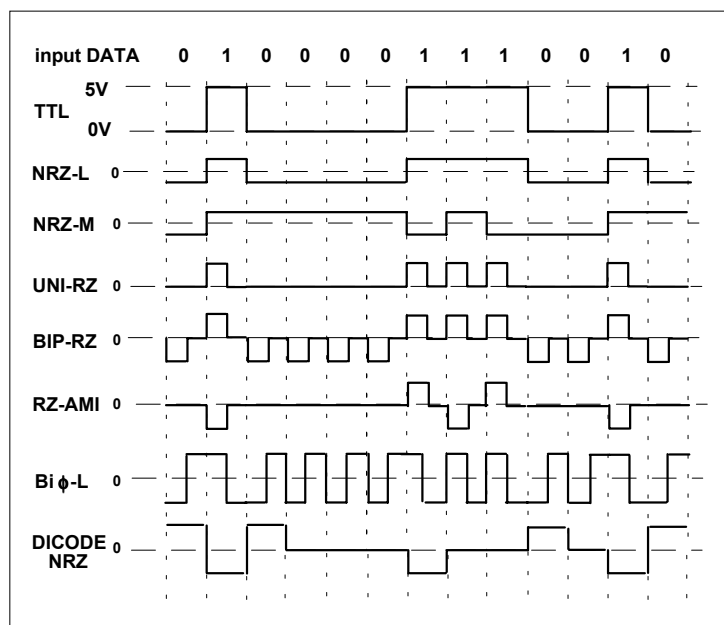


Figure 2: TIMS line codes

The output waveforms, apart from being encoded, have all had their amplitudes adjusted to suit a TIMS analog channel (not explicitly shown in Figure 2).

When connected to the input of the LINE-CODE DECODER these waveforms are de-coded back to the original TTL sequence.

band limiting

No matter what the line code in use, it is not uncommon to bandlimit these waveforms before they are sent to line, or used to modulate a carrier.

As soon as bandlimiting is invoked individual pulses will spread out (in the time domain) and interfere with adjacent pulses. This raises the issue of inter-symbol interference (ISI).

A study of ISI is outside the intended scope of this text, but it cannot be ignored in practice. Bandlimiting (by pulse shaping) can be effected and ISI controlled by appropriate filter design.

An alternative approach, duobinary encoding, was invented by Lender ¹.

duobinary encoding

A duobinary encoder (and decoder) is included in the line code modules.

Duobinary encoding is also called correlative coding, or partial response signalling.

The precoded duobinary encoding model implemented in the LINE-CODE ENCODER module is described in the *TIMS Advanced Modules User Manual*.

¹ Lender, A. "The Duobinary Technique for High Speed Data Transmission", IEEE Trans. Comm. Electron, vol 82, pp. 214-218, May 1963

EXPERIMENT

Figure 3 shows a simplified model of Figure 1. There is no source encoding or decoding, no baseband channel, and no detection. For the purpose of the experiment this is sufficient to confirm the operation of the line code modules.

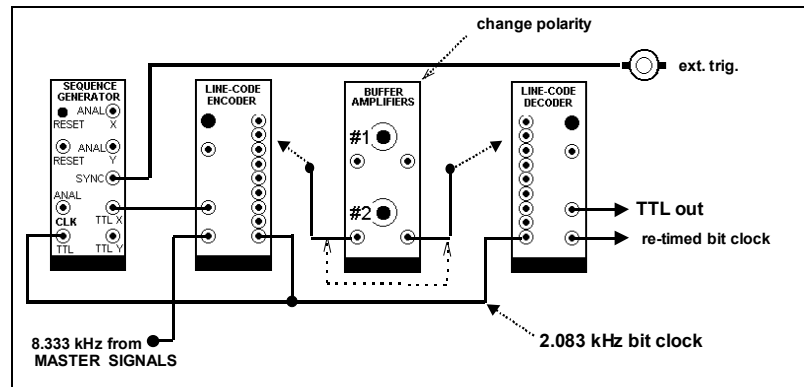


Figure 3: simplified model of Figure 1

When a particular code has been set up, and the message successfully decoded without error, the BUFFER should be included in the transmission path. By patching it in or out it will introduce a polarity change in the channel.

If there is no change to the message output, then the code in use is insensitive to polarity reversals.

Note that the LINE-CODE DECODER requires, for successful decoding, an input signal of amplitude near the TMS ANALOG REFERENCE LEVEL (± 2 volt pp). In normal applications this is assured, since it will obtain its input from the DECISION MAKER.

procedure

There are no step-by-step Tasks for you to perform. Instead, it is left to you to ensure that (in the approximate order indicated):

1. you read the *TIMS Advanced Modules User Manual* for more details of the LINE-CODE ENCODER and LINE-CODE DECODER modules than is included here.
2. you select a short sequence from the transmitter message source

3. at least initially you synchronize the oscilloscope to show a snapshot of the transmitter sequence. Later you may be interested in eye patterns ?
4. examine each code in turn from the encoder, confirming the transformation from TTL is as expected. On the other hand, and far more challenging, is to determine what the law of each transformation is without help from a Textbook or other reference.
5. of significant interest would be an examination of the power spectra of each of the coded signals. For this you would need data capturing facilities, and software to perform spectral analysis.
6. and so on

resetting

Resetting of the LINE-CODE ENCODER and the LINE-CODE DECODER after the master clock is connected, or after any clock interruption, is strictly not necessary for *all* codes. But it is easier to do it for *all* codes rather than remember for which codes it is essential.

For more details refer to the *TIMS Advanced Modules User Manual*.

TUTORIAL QUESTIONS

- Q1** *why introduce the complications of line encoding in a digital transmission system ?*
- Q2** *apart from the inevitable delay introduced by the analog filter, did you notice any other delays in the system ? You may need this information when debugging later experiments.*
- Q3** *an important function of many line encoders is the elimination of the DC component. When is this desirable ?*

ASK - AMPLITUDE SHIFT KEYING

PREPARATION	50
generation	50
bandwidth modification	51
demodulation methods	52
bandwidth estimation	53
EXPERIMENT	53
T1.0 generation.....	53
T1.1 modelling with a DUAL ANALOG SWITCH.....	54
T1.2 modelling with a MULTIPLIER.....	54
T2.0 bandwidth measurement	55
T3.0 demodulation	56
T3.1 envelope demodulation	56
T3.2 synchronous demodulation	56
T3.3 post-demodulation processing	56
T4.0 carrier acquisition	57
TUTORIAL QUESTIONS	58

ASK - AMPLITUDE SHIFT KEYING

ACHIEVEMENTS: *generation and demodulation of an amplitude shift keyed (ASK) signal.*

PREREQUISITES: *it would be advantageous to have completed some of the experiments in **Volume A1** involving linear modulation and demodulation.*

EXTRA MODULES: *DECISION MAKER*

PREPARATION

generation

Amplitude shift keying - ASK - in the context of digital communications is a modulation process which imparts to a sinusoid two or more discrete amplitude levels ¹. These are related to the number of levels adopted by the digital message.

For a binary message sequence there are two levels, one of which is typically zero.

Thus the modulated waveform consists of bursts of a sinusoid.

Figure 1 illustrates a binary ASK signal (lower), together with the binary sequence which initiated it (upper). Neither signal has been bandlimited.

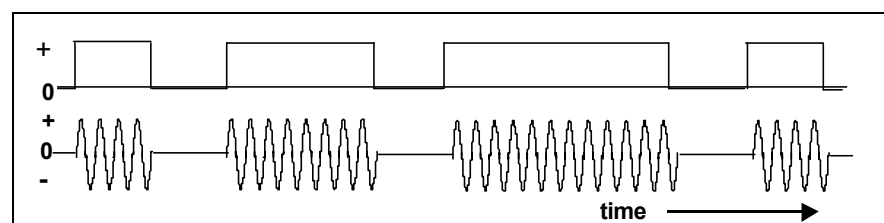


Figure 1: an ASK signal (below) and the message (above)

¹ also called on-off keying - OOK

There are sharp discontinuities shown at the transition points. These result in the signal having an unnecessarily wide bandwidth. Bandlimiting is generally introduced before transmission, in which case these discontinuities would be 'rounded off'. The bandlimiting may be applied to the digital message, or the modulated signal itself.

The data rate is often made a sub-multiple of the carrier frequency. This has been done in the waveform of Figure 1.

One of the disadvantages of ASK, compared with FSK and PSK, for example, is that it has not got a constant envelope. This makes its processing (eg, power amplification) more difficult, since linearity becomes an important factor. However, it does make for ease of demodulation with an envelope detector.

A block diagram of a basic ASK generator is shown in Figure 2. This shows bandlimiting following modulation.

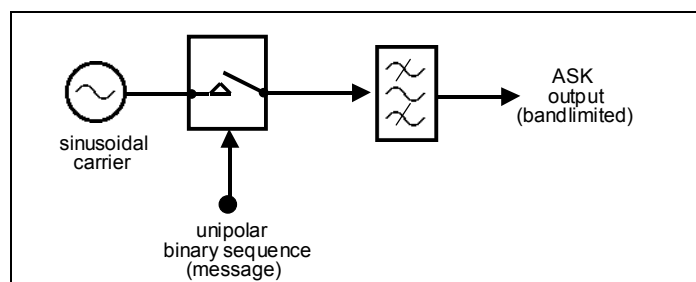


Figure 2: the principle of ASK generation

The switch is opened and closed by the unipolar binary sequence.

bandwidth modification

As already indicated, the sharp discontinuities in the ASK waveform of Figure 1 imply a wide bandwidth. A significant reduction can be accepted before errors at the receiver increase unacceptably. This can be brought about by bandlimiting (pulse shaping) the message *before* modulation, or bandlimiting the ASK signal itself *after* generation.

Both these options are illustrated in Figure 3, which shows one of the generators you will be modelling in this experiment.

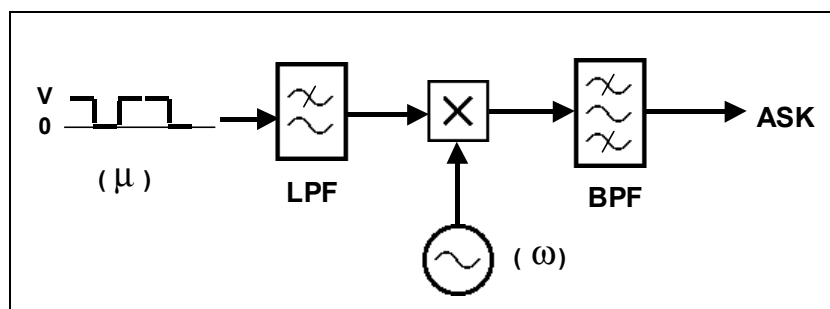


Figure 3: ASK bandlimiting, with a LPF or a BPF.

Figure 4 shows the signals present in a model of Figure 3, where the message has been bandlimited. The shape, after bandlimiting, depends naturally enough upon the amplitude and phase characteristics of the bandlimiting filter.

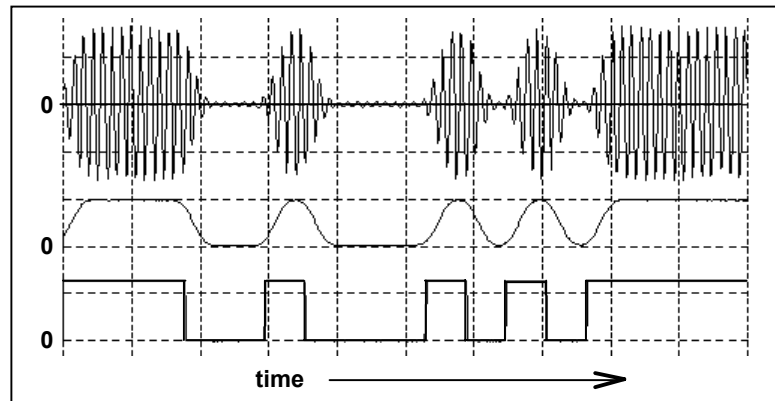


Figure 4: original TTL message (lower), bandlimited message (centre), and ASK (above)

You can approximate these waveforms with a SEQUENCE GENERATOR clocked at about 2 kHz, filter #3 of the BASEBAND CHANNEL FILTERS, and a 10 kHz carrier from a VCO.

demodulation methods

It is apparent from Figures 1 and 4 that the ASK signal has a well defined envelope. Thus it is amenable to demodulation by an envelope detector.

A synchronous demodulator would also be appropriate.

Note that:

- envelope detection circuitry is simple.
- synchronous demodulation requires a phase-locked local carrier and therefore carrier acquisition circuitry.

With bandlimiting of the transmitted ASK neither of these demodulation methods would recover the original binary sequence; instead, their outputs would be a bandlimited version. Thus further processing - by some sort of decision-making circuitry for example - would be necessary.

Thus demodulation is a two-stage process:

1. recovery of the bandlimited bit stream
2. regeneration of the binary bit stream

Figure 5 illustrates.

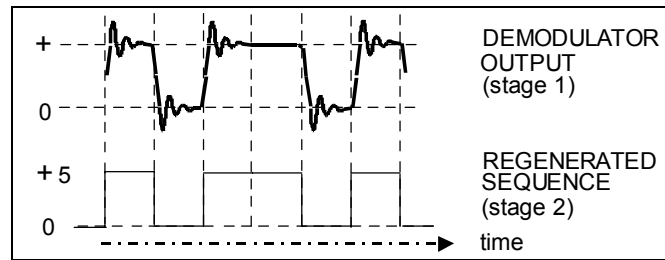


Figure 5: the two stages of the demodulation process

bandwidth estimation

It is easy to estimate the bandwidth of an ASK signal. Refer to the block diagram of Figure 3. This is a DSB transmitter. It is an example of linear modulation. If we know the message bandwidth, then the ASK bandwidth is twice this, centred on the 'carrier' frequency.

Using the analogy of the DSB generator, the binary sequence is the message (bit rate ' μ '), and the sinewave being switched is the carrier (' ω ').

Even though you may not have an analytical expression for the bandwidth of a pseudo random binary sequence, you can estimate that it will be of the same order as that of a square, or perhaps a rectangular, wave.

For the special case of a binary sequence of alternate ones and zeros the spectrum will:

- be symmetrical about the frequency of the carrier ' ω '
- have a component at ' ω ', because there will be a DC term in the message
- have sidebands spaced at odd multiples of ' μ ' either side of the carrier
- have sideband amplitudes which will decrease either side of the carrier (proportional to $1/n$, where ' n ' is the order of the term).

If you accept the spectrum is symmetrical around the carrier then you can measure its effective bandwidth by passing it through a tuneable lowpass filter. A method is suggested in the experiment below.

You can discuss this when answering Tutorial Question Q2.

EXPERIMENT

T1.0 generation

There are many methods of modelling an ASK generator with TIMS. For any of them the binary message sequence is best obtained from a SEQUENCE GENERATOR, clocked at an appropriate speed. Depending upon the generator

configuration, either the data bit stream can be bandlimited, or the ASK itself can be bandpass filtered.

Suggestions for modelling the ASK generators are:

T1.1 modelling with a DUAL ANALOG SWITCH

It is possible to model the rather basic generator shown in Figure 2.

The switch can be modelled by one half of a DUAL ANALOG SWITCH module. Being an *analog* switch, the carrier frequency would need to be in the audio range. For example, 15 kHz from a VCO. The TTL output from the SEQUENCE GENERATOR is connected directly to the CONTROL input of the DUAL ANALOG SWITCH. For a synchronous carrier and message use the 8.333 kHz TTL sample clock (filtered by a TUNEABLE LPF) and the 2.083 kHz sinusoidal message from the MASTER SIGNALS module.

If you need the TUNEABLE LPF for bandlimiting of the ASK, use the sinusoidal output from an AUDIO OSCILLATOR as the carrier. For a synchronized message as above, tune the oscillator close to 8.333 kHz, and lock it there with the sample clock connected to its SYNCH input.

This arrangement is shown modelled in Figure 6.

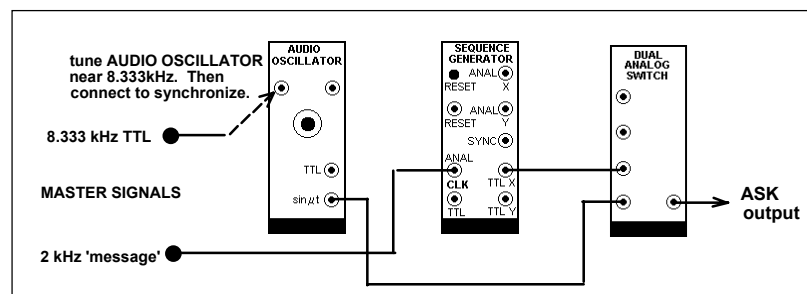


Figure 6: modelling ASK with the arrangement of Figure 2

Bandlimiting can be implemented with a filter at the output of the ANALOG SWITCH.

T1.2 modelling with a MULTIPLIER

A MULTIPLIER module can be used as the switch. The carrier can come from any suitable sinusoidal source. It could be at any available TIMS frequency.

The other input to the MULTIPLIER needs to be the message sequence.

Neither the TTL nor the analog sequence is at an appropriate voltage level. Each requires amplitude scaling. This can be implemented in an ADDER, which will invert the sequence polarity. DC from the VARIABLE DC module can be used to re-set the DC level. The required signal will be at a level of either 0 V or +2 V, the latter being optimum for the (analog) MULTIPLIER.

This arrangement is shown modelled in Figure 7.

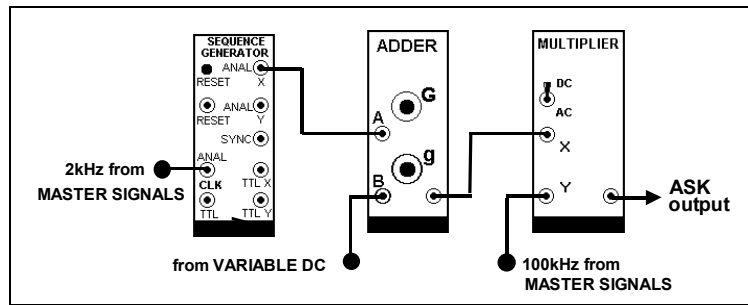


Figure 7: modelling ASK with the arrangement of Figure 3.

The operating frequency of the modulator of Figure 7 is not restricted to audio frequencies. Any carrier frequency available within TIMS may be used, but remember to keep the data rate below that of the carrier frequency.

For a synchronous system (ie, message and carrier rates related, so as to give 'stable' oscilloscope displays):

- clock the SEQUENCE GENERATOR from the 2 kHz message (as shown), or the 8.333 kHz sample clock.
- use a 100 kHz carrier (as shown), or an AUDIO OSCILLATOR locked to the 8.333 kHz sample clock.

Any other combination of data clock and carrier frequency, synchronous or otherwise, is possible (with this model); but not all combinations will generate an ASK signal. Try it !

Bandlimiting can be implemented with a filter at the MULTIPLIER output (a 100 kHz CHANNEL FILTERS module), or the bit sequence itself can be bandlimited (BASEBAND CHANNEL FILTERS module).

T2.0 bandwidth measurement

Having generated an ASK signal, an estimate of its bandwidth can be made using an arrangement such as illustrated in Figure 8. The bandwidth of the lowpass filter is reduced until you consider that the envelope can no longer be identified.

This will indicate the *upper* frequency limit of the signal. Do you think it reasonable to then make a declaration regarding the *lower* frequency limit ?

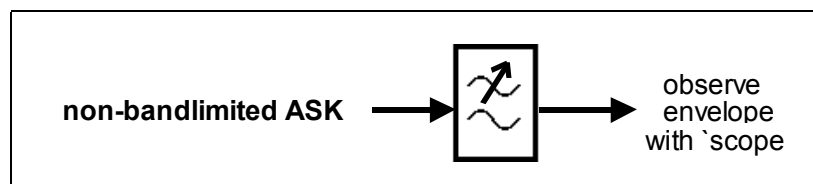


Figure 8: ASK bandwidth estimation

The arrangement of Figure 8 is easy to model with TIMS. Use the TUNEABLE LPF. But remember to select appropriate ASK frequencies.

T3.0 demodulation

Both asynchronous and synchronous demodulation methods are used for the demodulation of ASK signals.

T3.1 envelope demodulation

Having a very definite envelope, an envelope detector can be used as the first step in recovering the original sequence. Further processing can be employed to regenerate the true binary waveform.

Figure 9 is a model for envelope recovery from a baseband FSK signal.

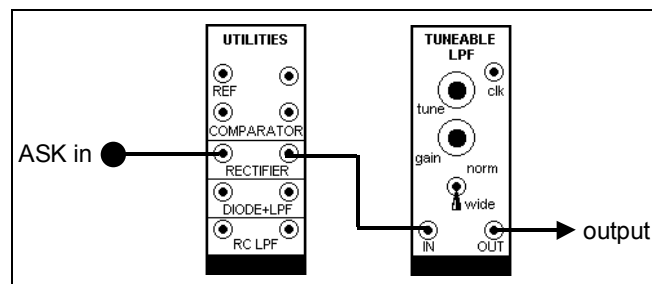


Figure 9: envelope demodulation of baseband ASK

If you choose to evaluate the model of Figure 9, remember there is a relationship between bit rate and the lowpass filter bandwidth. Select your frequencies wisely.

T3.2 synchronous demodulation

A synchronous demodulator can be used for demodulation, as shown in Figure 10. In the laboratory you can use a stolen carrier, as shown.

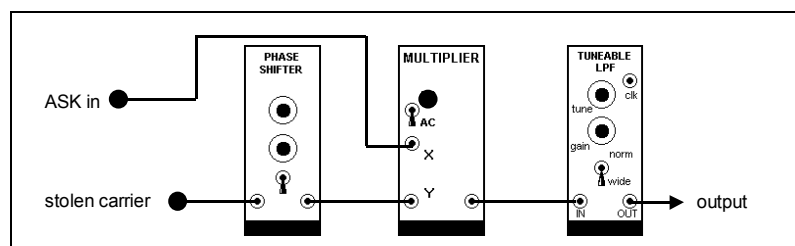


Figure 10: synchronous demodulation of ASK

T3.3 post-demodulation processing

The output from both of the above demodulators will not be a copy of the binary sequence TTL waveform. Bandlimiting will have shaped it, as (for example) illustrated in Figure 4.

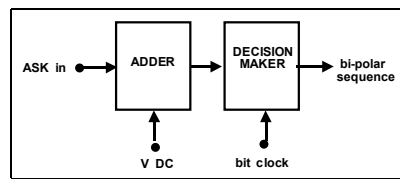


Figure 11

Some sort of decision device is then required to regenerate the original binary sequence. The DECISION MAKER module could be employed, with associated processing, if required. This is illustrated in block diagram form in Figure 11 (opposite).

This model will regenerate a bi-polar sequence from the recovered envelope.

Figure 12 shows the model of the block diagram of Figure 11.

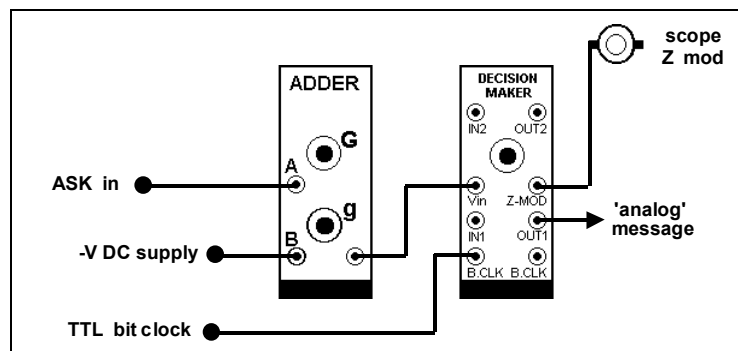


Figure 12: regeneration to a bi-polar sequence

Remember to:

- convert the uni-polar, bandlimited output of the envelope detector to bi-polar (using the ADDER), to suit the DECISION MAKER.
- set the on-board switch SW1, of the DECISION MAKER, to NRZ-L. This configures it to accept bi-polar inputs.
- adjust the decision point of the DECISION MAKER
- in the first instance, use a stolen carrier and bit clock

The output will be the regenerated message waveform. Coming from a YELLOW analog output socket, it is bi-polar ± 2 V (not TTL).

The same regenerator can be used to process the output from the synchronous demodulator of Figure 10.

T4.0 carrier acquisition

Rather than using a stolen carrier and bit clock you might like to try recovering these from the received ASK signal.

TUTORIAL QUESTIONS

Q1 *suggest an advantage of making the data rate a sub-multiple of the carrier rate.*

Q2 *discuss your methods of measuring and/or estimating the bandwidth of the ASK signal. Estimate the maximum amount of bandwidth limiting possible, and the trade-offs involved.*

Q3 *the ASK waveform of Figure 1 is 'special' in that:*

- a) the bit rate is a sub-multiple of the carrier*
- b) the phasing of the message ensures that each 'burst' of carrier starts and ends at zero amplitude.*

If these special conditions are changed, consider the shape of the waveform at the beginning and end of each burst of carrier. What effect, if any, will this have on the bandwidth of the ASK signal ?

FSK - FREQUENCY SHIFT KEYING

PREPARATION	60
generation	60
bandwidth	61
demodulation	61
asynchronous	62
synchronous	62
phase locked loop	63
post-demodulation processing	63
comments	63
EXPERIMENT	64
T1.0 generation	64
T1.1 scheme #1	64
T1.1 scheme #2	65
T1.0 demodulation	65
T1.1 signals for demodulation	66
T1.1 asynchronous receiver	66
T1.1 synchronous receiver	67
T1.1 PLL - phase locked loop	67
TUTORIAL QUESTIONS	68

FSK - FREQUENCY SHIFT KEYING

ACHIEVEMENTS: *generation and demodulation of a binary FSK signal.*

PREREQUISITES: *it would be advantageous to have completed some of the Part I experiments involving linear modulation and demodulation.*

EXTRA MODULES: *a second VCO, BIT CLOCK REGEN. Optionally, a UTILITIES and a TUNEABLE LPF.*

PREPARATION

generation

As its name suggests, a frequency shift keyed transmitter has its frequency shifted by the message.

Although there could be more than two frequencies involved in an FSK signal, in this experiment the message will be a binary bit stream, and so only two frequencies will be involved.

The word 'keyed' suggests that the message is of the 'on-off' (mark-space) variety, such as one (historically) generated by a morse key, or more likely in the present context, a binary sequence. The output from such a generator is illustrated in Figure 1 below.

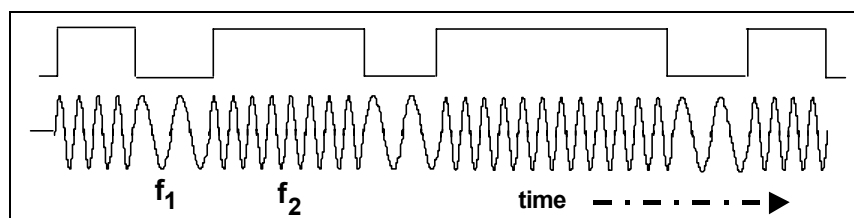


Figure 1: an FSK waveform, derived from a binary message

Conceptually, and in fact, the transmitter could consist of two oscillators (on frequencies f_1 and f_2), with only one being connected to the output at any one time. This is shown in block diagram form in Figure 2 below.

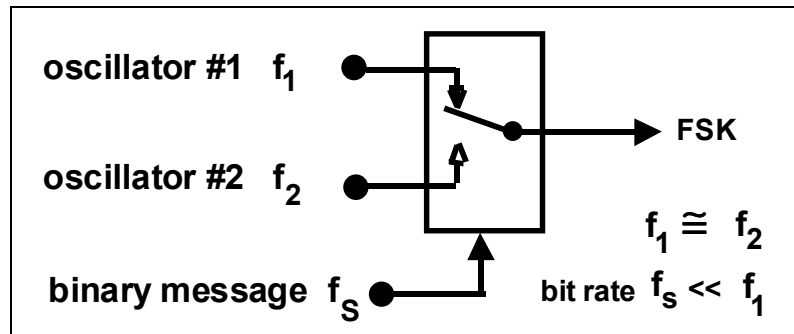


Figure 2: an FSK transmitter

Unless there are special relationships between the two oscillator frequencies and the bit clock there will be abrupt phase discontinuities of the output waveform during transitions of the message.

bandwidth

Practice is for the tones f_1 and f_2 to bear special inter-relationships, and to be integer multiples of the bit rate. This leads to the possibility of continuous phase, which offers advantages, especially with respect to bandwidth control.

Alternatively the frequency of a single oscillator (VCO) can be switched between two values, thus guaranteeing continuous phase - CPFSK. See Tutorial Question Q2.

The continuous phase advantage of the VCO is not accompanied by an ability to ensure that f_1 and f_2 are integer multiples of the bit rate. This would be difficult (impossible ?) to implement with a VCO. See Tutorial Question Q3.

Being an example of non-linear modulation, calculation of the bandwidth of an FSK signal is a non-trivial exercise. It will not be attempted here.

See Tutorial Question Q1.

FSK signals can be generated at baseband, and transmitted over telephone lines (for example). In this case, both f_1 and f_2 (of Figure 2) would be audio frequencies. Alternatively, this signal could be translated to a higher frequency. Yet again, it may be generated directly at 'carrier' frequencies.

demodulation

There are different methods of demodulating FSK. A natural classification is into synchronous (coherent) or asynchronous (non-coherent).

Representative demodulators of these two types are the following:

asynchronous

A close look at the waveform of Figure 1 reveals that it is the sum of two amplitude shift keyed (ASK) signals. These signals were examined in the experiment entitled *ASK - amplitude shift keying* in this Volume.

The receiver of Figure 3 takes advantage of this. The FSK signal has been separated into two parts by bandpass filters (BPF) tuned to the MARK and SPACE frequencies.

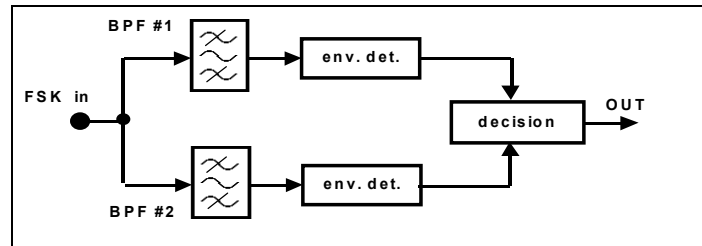


Figure 3: demodulation by conversion-to-ASK

The output from each BPF looks like an amplitude shift keyed (ASK) signal.

These can be demodulated asynchronously, using the envelope. The envelope detector is examined in the experiment entitled *Envelope recovery* within *Volume A1 - Fundamental Analog Experiments*.

The decision circuit, to which the outputs of the envelope detectors are presented, selects the output which is the most likely one of the two inputs. It also re-shapes the waveform from a bandlimited to a rectangular form.

This is, in effect, a two channel receiver. The bandwidth of each is dependent on the message bit rate. There will be a minimum frequency separation required of the two tones.

hint

You are advised to read ahead, *before* attempting the experiment, to consider the modelling of this demodulator. Unlike most TIMS models, you are *not* free to choose parameters - particularly frequencies. If they are to be tuned to *different* frequencies, then one of these frequencies must be 2.083 kHz (defined as the MARK frequency). This is a restriction imposed by the BIT CLOCK REGEN module, of which the BPF are sub-systems. As a result of this, most other frequencies involved are predetermined. Make sure you appreciate why this is so, then decide upon:

- bit clock rate
- SPACE frequency
- envelope detector LPF characteristics

synchronous

In the block diagram of Figure 4 two local carriers, on each of the two frequencies of the binary FSK signal, are used in two synchronous demodulators. A decision circuit examines the two outputs, and decides which is the most likely.

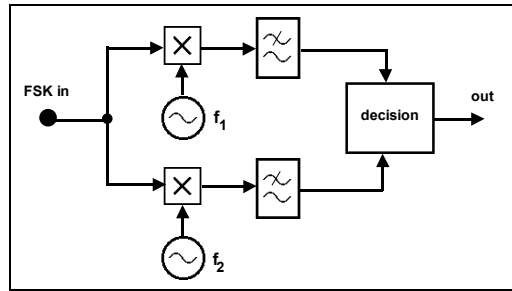


Figure 4: synchronous demodulation

This is, in effect, a two channel receiver. The bandwidth of each is dependent on the message bit rate. There will be a minimum frequency separation required of the two tones. This demodulator is more complex than most asynchronous demodulators.

phase locked loop

A phase locked loop is a well known method of demodulating an FM signal. It is thus capable of demodulating an FSK signal. It is examined in the experiment entitled *FM demodulation with the PLL* within *Volume A2 - Further & Advanced Analog Experiments*. It is shown, in block diagram form, in Figure 5 below.

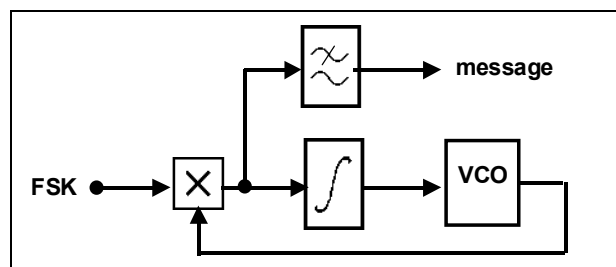


Figure 5: phase locked loop demodulator

The control signal, which forces the lock, is a bandlimited copy of the message sequence. Depending upon the bandwidth of the loop integrator, a separate LPF will probably be required (as shown) to recover the message.

post-demodulation processing

The output of a demodulator will typically be a bandlimited version of the original binary sequence. Some sort of decision device is then required to regenerate the original binary sequence. This is shown in the block diagrams above, but has not been implemented in the TIMS models to follow.

comments

One might imply, from all of the above, that the generation and demodulation of an FSK signal is relatively trivial, and that there is not a lot more to know about its properties. Such is not the case.

Extensive research has been carried out into the properties of an FSK signal. This includes the determination of the optimum relationship between the frequencies of the two tones and the data rate. You should refer to your text book for more information.

EXPERIMENT

This experiment is not typical. There are no specific tasks to be completed. Instead you are invited to investigate any or all of the models below in your own way.

Various methods of FSK generation are possible with TIMS, and some suggestions follow.

In all of the modulation schemes the message will be derived from a pseudo random binary SEQUENCE GENERATOR.

T1.0 generation

T1.1 scheme #1

A VCO module is ideally suited for the generation of a continuous phase FSK signal, as shown in Figure 6.

In FSK mode the VCO is keyed by the message TTL sequence. Internal circuitry results in a TTL HI switching the VCO to frequency f_1 , while a TTL LO switches it to frequency f_2 . These two frequencies may be in the audio range (front panel toggle switch LO), or in the 100 kHz range (front panel toggle switch HI).

The frequencies f_1 and f_2 are set by the on-board variable resistors RV8 and RV7 respectively, while a continuous TTL HI or a TTL LO is connected to the DATA input socket. See Tutorial Question Q6.

In FSK mode neither of the front panel rotary controls of the VCO is in operation.

See Tutorial Question Q2.

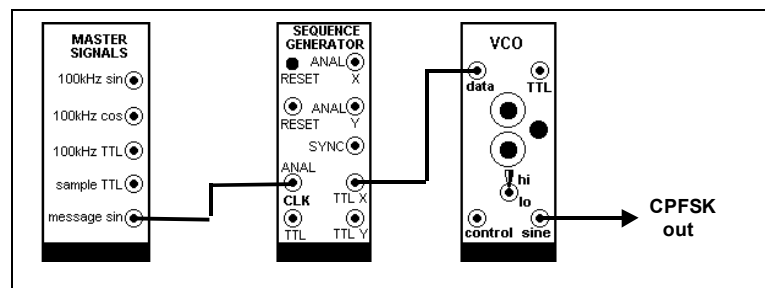


Figure 6: CPFSK

T1.2 scheme #2

Figure 7 shows a model of the arrangement of Figure 2. It switches either one of two tones to the output, in response to the message sequence.

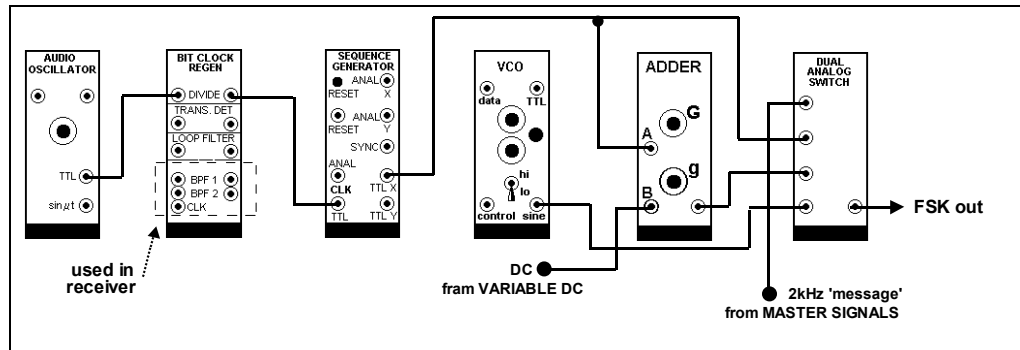


Figure 7: a model of the arrangement of Figure 2

The binary sequence is shown clocked by a divided-by-8 version of the output of an AUDIO OSCILLATOR. This oscillator cannot itself be tuned to this relatively low (for T1.2) frequency. The DIVIDE-BY-8 sub-system is in the BIT CLOCK REGEN module (set the on-board switch SW2 with both toggles DOWN).

The signals at f_1 and f_2 are provided by the 2.083 kHz MESSAGE from the MASTER SIGNALS module, and a VCO, respectively¹. The DUAL AUDIO SWITCH module is used to switch between them.

- one of the two ANALOG SWITCHES is driven directly by the TTL binary message sequence.
- the other ANALOG SWITCH is driven by the same TTL sequence, reversed in polarity, and then DC shifted by +5 volts. The reversal and DC shift is performed by the ADDER, with a maximum -ve output from the VARIABLE DC module. Although 5 volt signals exceed the T1.2 ANALOG REFERENCE LEVEL the ADDER design is such that it will not be overloaded.

Unless there is already an FSK signal available at TRUNKS, this transmitter is to be used in conjunction with an asynchronous demodulator, of the type illustrated in Figure 3, and modelled in Figure 8 - so don't strip it down unnecessarily.

T2.0 demodulation

In the receivers described below it is assumed there is no bandlimiting (or noise) introduced by a channel. In the case of poor signal-to-noise ratio the MARK and SPACE signals would need to be compared in a decision circuit and the most likely one presented to the output.

¹ one or more of the above signals may be available at TRUNKS.

T2.1 signals for demodulation

The demodulators to be examined will require FSK signals as inputs. These may exist at TRUNKS - check.

If not, then you will need to generate your own.

For a suitable FSK test signal you could use the model of Figure 7. The MARK signal is pre-set to 2.083 kHz; initially set the SPACE to about 3 kHz.

T2.2 asynchronous receiver

An example of this is the demodulator of Figure 3, shown modelled in Figure 8.

The demodulator requires two bandpass (BPF) filters, tuned to the MARK and SPACE frequencies. Suitable filters exist as sub-systems in the BIT CLOCK REGEN module. These are described in the experiment entitled *Digital utility sub-systems* (within *Volume D2 - Further & Advanced Digital Experiments*).

To prepare the filters it is necessary to set the on-board switch SW1. Put the left hand toggle UP, and right hand toggle DOWN. This tunes BPF1 to 2.083 kHz, and BPF2 anywhere in the range $1 < f_0 < 5$ kHz, depending on the VCO (the filter centre frequency will be 1/50 of the VCO frequency).

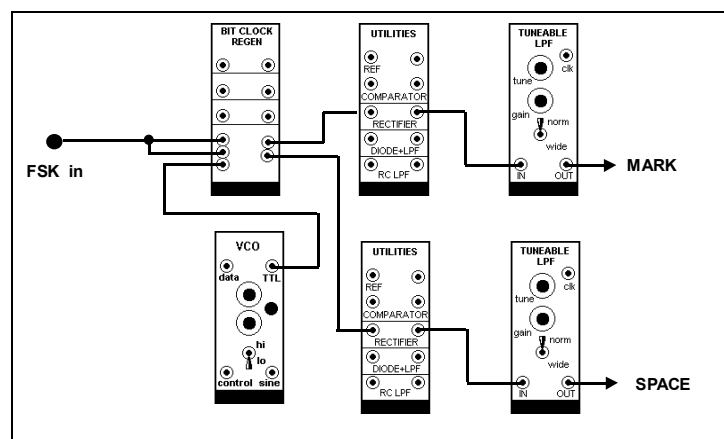


Figure 8: a model of the receiver of Figure 3

If you do not have extra UTILITIES and TUNEABLE LPF modules, then complete just one arm of the demodulator.

Alignment requires the BPFs to be tuned to the MARK and SPACE frequencies. The first is already done (2.083 kHz is already pre-set with SW1); the other is set with the VCO (already pre-set with SW2).

Note that the specified bit rate is, by TMS standards, rather low. The average oscilloscope display can be a little flickery. Use a short sequence, and the SYNC signal from the SEQUENCE GENERATOR to ext. trig.

- what would happen if the bit rate was speeded up ?
- what would happen if the frequency of the SPACE signal, at the transmitter, was moved towards 2.083 kHz ? Of course, the receiver BPF2 would need to be retuned.

After successfully demodulating the MARK and the SPACE:

- test your preparatory work and show how close the MARK / SPACE frequencies can approach before performance is degraded - explain why this is so.
- predict what will happen if the bit rate is increased. If you have supplied your own FSK signal then you should test your prediction.

T2.3 synchronous receiver

A synchronous receiver of Figure 4 requires two local carriers, locked to the MARK and SPACE frequencies. Such a receiver would require two VCO and associated modules, and is probably too ambitious to attempt as part of this experiment.

T2.4 PLL - phase locked loop

A phase locked loop is shown in block diagram form in Figure 5, and modelled in Figure 9.

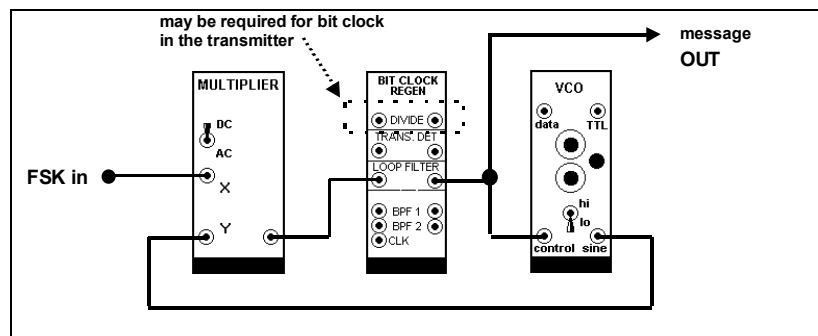


Figure 9: PLL demodulator - the model of Figure 5

The PLL is examined in the experiment entitled *FM demodulation with the PLL* (within *Volume A2 - Further & Advanced Analog Experiments*).

For the present experiment the integrator (of Figure 5) is modelled with the LOOP FILTER in the BIT CLOCK REGEN module. This module contains four independent sub-systems. The DIVIDE-BY-8 sub-system may already be in use at the transmitter.

If you are fussy about the appearance of the demodulated output it can be further filtered; say with the LPF in the HEADPHONE AMPLIFIER.

Could you use either the DECISION MAKER, or the COMPARATOR in the UTILITIES modules, or the HARD LIMITER in the DELTA MODULATION UTILITIES module, to regenerate the message as a clean TTL sequence ?

TUTORIAL QUESTIONS

- Q1** analysis of the spectrum of an FM signal (an example of non-linear modulation) is not trivial. For the case where the FSK signal can be looked upon as the sum of two ASK signals (example of linear modulation), what can you say about its frequency spectrum ?*
- Q2** the VCO is a very convenient method of making FSK - in fact, CFSK. VCOs come as low-cost integrated circuits, and their modulation characteristic allow wideband FM. However, for communications applications, they have one serious shortcoming. For example ?*
- Q3** what advantage is there in making the frequencies of the two tones of an FSK signal, and the bit rate, sub-multiples of some reference frequency ?*
- Q4** given the bandwidths of a pair of BPFs, what would determine the frequency separation of the two tones f_1 and f_2 , and the message bit rate f_s , in a receiver such as illustrated in Figure 3 ?*
- Q5** what are some of the factors which might determine the choice of either a synchronous or asynchronous FSK demodulator ?*
- Q6** where can one find a convenient TTL HI, and a convenient TTL LO, in TMS ?*
- Q7** consider the asynchronous receiver of Figure 3. The message could be reconstructed from the output of either envelope detector. For example, if the MARK signal is available then the SPACE signal is its complement. So why have both envelope detectors ?*

BPSK - BINARY PHASE SHIFT KEYING

PREPARATION	70
generation of BPSK.....	70
bandlimiting	71
BPSK demodulation.....	72
phase ambiguity.....	72
EXPERIMENT	73
the BPSK generator	73
BPSK demodulator.....	74
measurements	75
further study	76
TUTORIAL QUESTIONS	77
APPENDIX.....	78

BPSK - BINARY PHASE SHIFT KEYING

ACHIEVEMENTS: generation of binary phase shift keyed (BPSK) signal; bandlimiting; synchronous demodulation - phase ambiguities.

PREREQUISITES: it would be advantageous to have completed some of the experiments in Volume A1, involving linear modulation and demodulation. Familiarity with the DECISION MAKER, LINE-CODE ENCODER and LINE-CODE DECODER modules is assumed.

EXTRA MODULES: DECISION MAKER, LINE-CODE ENCODER and LINE-CODE DECODER. A total of two PHASE SHIFTER modules is required.

PREPARATION

generation of BPSK

Consider a sinusoidal carrier. If it is modulated by a bi-polar bit stream according to the scheme illustrated in Figure 1 below, its polarity will be reversed every time the bit stream changes polarity. This, for a sinewave, is equivalent to a phase reversal (shift). The multiplier output is a BPSK¹ signal.

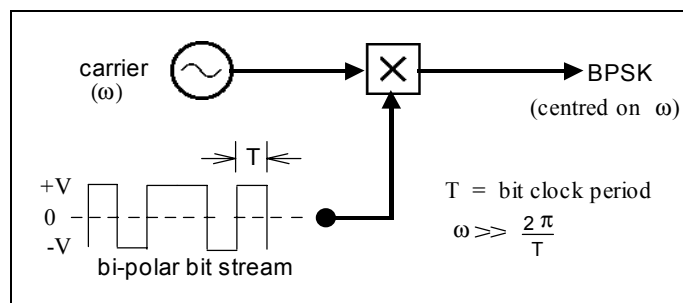


Figure 1: generation of BPSK

¹ also sometimes called PRK - phase reversal keying.

The information about the bit stream is contained in the changes of phase of the transmitted signal.

A synchronous demodulator would be sensitive to these phase reversals.

The appearance of a BPSK signal in the time domain is shown in Figure 2 (lower trace). The upper trace is the binary message sequence.

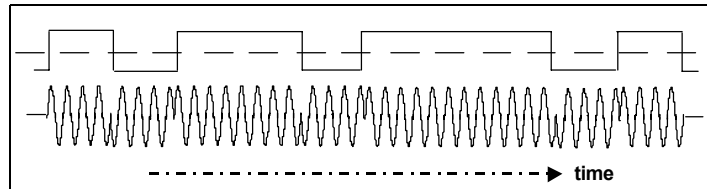


Figure 2: a BPSK signal in the time domain.

There is something special about the waveform of Figure 2. The wave shape is ‘symmetrical’ at each phase transition. This is because the bit rate is a sub-multiple of the carrier frequency $\omega/(2\pi)$. In addition, the message transitions have been timed to occur at a zero-crossing of the carrier.

Whilst this is referred to as ‘special’, it is not uncommon in practice. It offers the advantage of simplifying the bit clock recovery from a received signal. Once the carrier has been acquired then the bit clock can be derived by division.

But what does it do to the bandwidth ?See Tutorial Question Q4.

bandlimiting

The basic BPSK generated by the simplified arrangement illustrated in Figure 1 will have a bandwidth in excess of that considered acceptable for efficient communications.

If you can calculate the spectrum of the binary sequence then you know the bandwidth of the BPSK itself. The BPSK signal is a *linearly modulated* DSB, and so it has a bandwidth twice that of the baseband data signal from which it is derived².

In practice there would need to be some form of bandwidth control.

Bandlimiting can be performed either at baseband or at carrier frequency. It will be performed at baseband in this experiment.

² this assumes $\omega > 2B$

BPSK demodulation

Demodulation of a BPSK signal can be considered a two-stage process.

1. translation back to baseband, with recovery of the bandlimited message waveform
2. regeneration from the bandlimited waveform back to the binary message bit stream.

Translation back to baseband requires a local, synchronized carrier.

stage 1

Translation back to baseband is achieved with a synchronous demodulator, as shown in Figure 3 below.

This requires a local synchronous carrier. In this experiment a stolen carrier will be used.

Carrier acquisition will be investigated in the experiment entitled *DPSK - carrier acquisition and BER* (within *Volume D2 - Further & Advanced Digital Experiments*)

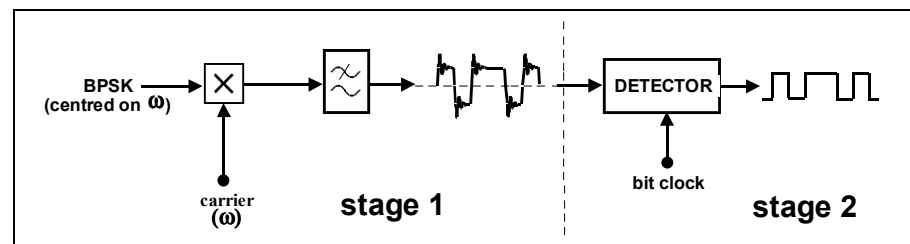


Figure 3: synchronous demodulation of BPSK

stage 2

The translation process does not reproduce the original binary sequence, but a bandlimited version of it.

The original binary sequence can be regenerated with a detector. This requires information regarding the bit clock rate. If the bit rate is a sub-multiple of the carrier frequency then bit clock regeneration is simplified.

In TIMS the DECISION MAKER module can be used for the regenerator, and in this experiment the bit clock *will* be a sub-multiple of the carrier.

phase ambiguity

You will see in the experiment that the sign of the phase of the demodulator carrier is important.

Phase ambiguity is a problem in the demodulation of a BPSK signal.

There are techniques available to overcome this. One such sends a training sequence, of known format, to enable the receiver to select the desired phase,

following which the training sequence is replaced by the normal data (until synchronism is lost !).

An alternative technique is to use differential encoding. This will be demonstrated in this experiment by selecting a different code from the LINE-CODE ENCODER.

EXPERIMENT

the BPSK generator

The BPSK generator of Figure 1 is shown in expanded form in Figure 4, and modelled in Figure 5

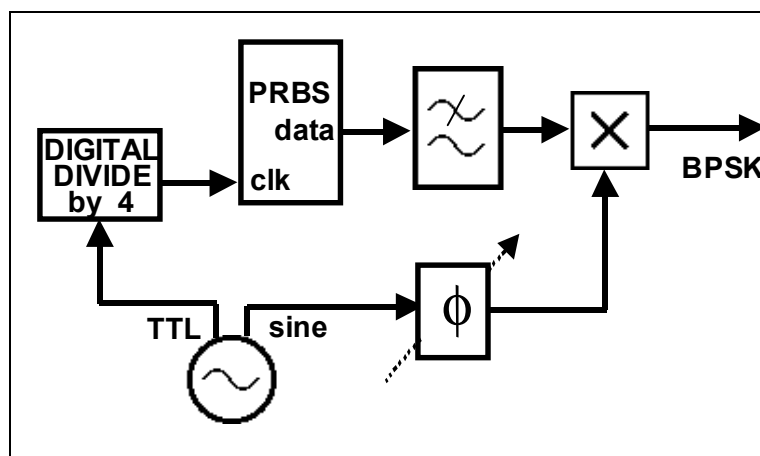


Figure 4: block diagram of BPSK generator to be modelled

Note that the carrier will be four times the bit clock rate.

The lowpass filter is included as a band limiter if required. Alternatively a bandpass filter could have been inserted at the output of the generator. Being a linear system, the effect would be the same.

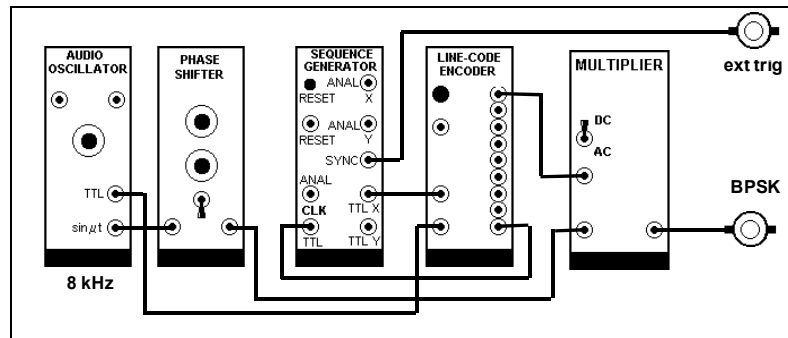


Figure 5: model of the BPSK generator

The AUDIO OSCILLATOR supplies a TTL signal for the bit clock digital DIVIDE-BY-FOUR sub-system in the LINE-CODE ENCODER, and a sinusoidal signal for the carrier.

The PHASE SHIFTER (set to the LO range with the on-board switch SW1) allows relative phase shifts. Watch the phase transitions in the BPSK output signal as this phase is altered. This PHASE SHIFTER can be considered optional.

The digital DIVIDE-BY-FOUR sub-system within the LINE-CODE ENCODER is used for deriving the bit clock as a sub-multiple of the BPSK carrier. Because the DECISION MAKER, used in the receiver, needs to operate in the range about 2 to 4 kHz, the BPSK carrier will be in the range about 8 to 16 kHz.

The NRZ-L code is selected from LINE-CODE ENCODER.

Viewing of the phase reversals of the carrier is simplified because the carrier and binary clock frequencies are harmonically related.

T1 patch up the modulator of Figure 5; acquaint yourself with a BPSK signal. Examine the transitions as the phase between bit clock and carrier is altered. Vary the bandwidth of the PRBS with the TUNEABLE LPF. Notice the envelope.

BPSK demodulator

Figure 3 shows a synchronous demodulator for a BPSK signal in block diagram form. This has been modelled in Figure 6 below. In the first part of the experiment the carrier and bit clocks will be stolen.

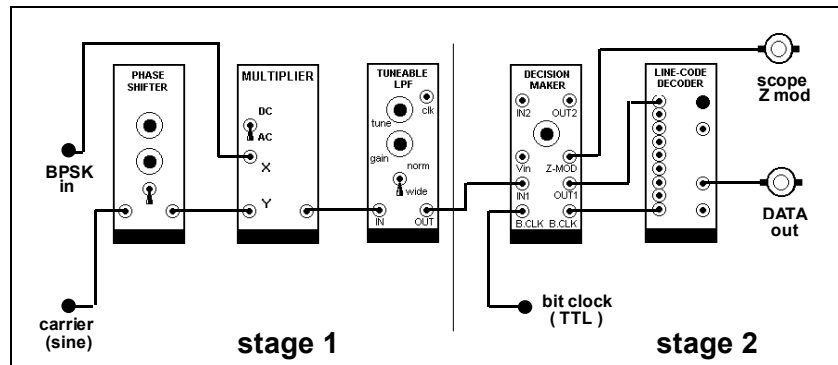


Figure 6: the BPSK demodulator

The phase of the carrier is adjustable with the PHASE SHIFTER for maximum output from the lowpass filter. Phase reversals of 180° can be introduced with the front panel toggle switch.

Select the NRZ-L input to the LINE-CODE DECODER. The LINE-CODE ENCODER and LINE-CODE DECODER modules are not essential in terms of the coding they introduce (since a bi-polar sequence is already available from the SEQUENCE GENERATOR) but they are useful in that they contain the DIVIDE-BY-FOUR sub-systems, which are used to derive the sub-multiple bit clock.

The LPF following the demodulator multiplier is there to remove the components at double the carrier frequency. Its bandwidth can be set to about 12 kHz; although, for maximum signal-to-noise ratio (if measuring bit error rates, for example), something lower would probably be preferred.

measurements

The BPSK will have been bandlimited by the lowpass filter in the transmitter, and so the received waveform is no longer rectangular in shape. But you can observe that the demodulator filter output is related to the transmitted sequence (the NRZ-L code introduces only a level shift and amplitude scale).

The DECISION MAKER³ will regenerate the original TTL sequence waveform.

Notice the effect upon the recovered sequence when the carrier phase is reversed at the demodulator.

The following Tasks are a reminder of what you might investigate.

T2 patch up the demodulator of Figure 6. The received signal will have come from the transmitter of Figure 5. Observe the output from the TUNEABLE LPF, and confirm its appearance with respect to that transmitted. If the sequence is inverted then toggle the front panel 180° switch of the receiver PHASE CHANGER.

³ introduced in the experiment entitled *Detection with the DECISION MAKER* in this Volume

***T3** set the on-board switch SW1 of the DECISION MAKER to accept NRZ-L coding. Use the gain control of the TUNEABLE LPF to set the input at about the TIMS ANALOG REFERENCE LEVEL of ± 2 volt peak. Adjust the decision point. Check the output.*

***T4** observe the TTL output from the LINE-CODE DECODER. Confirm that the phase of the receiver carrier (for the NRZ-L line code) is still important.*

***T5** investigate a change of bandwidth of the transmitted signal. Notice that, as the bandwidth is changed, the amplitude of the demodulated sequence at the DECISION MAKER input will change. This you might expect; but, under certain conditions, it can increase as the bandwidth is decreased ! How could this be ? See Tutorial Question Q6.*

further study

There is an extension to this experiment entitled *DPSK - carrier acquisition and BER* (within *Volume D2 - Further & Advanced Digital Experiments*)

TUTORIAL QUESTIONS

- Q1 do you think BPSK is an analog signal ? Any comments ?*
- Q2 in the model of Figure 5, is it necessary that the MULTIPLIER be switched to DC, as shown?*
- Q3 you observed the shape of the phase transitions as the PHASE SHIFTER of Figure 5 was changed. Would this influence the spectrum of the BPSK signal ?*
- Q4 does making the bit rate a sub-multiple of the carrier frequency have any influence on the spectrum of the BPSK signal ?*
- Q5 what is the purpose of the lowpass filter in the BPSK demodulator model ? What determines its bandwidth ?*
- Q6 the amplitude of the signal at the DECISION MAKER input can decrease as the bandwidth of the transmitter is widened (or vice versa). At first glance this seems unusual ? Explain.*
- Q7 the PHASE SHIFTER in the demodulator of Figure 6 was adjusted for maximum output. What phase was it optimizing, and what was the magnitude of this phase ? Could you measure it ?*

APPENDIX

The digital divider in the BIT CLOCK REGEN module may be set to divide by 1 (inversion) , 2, 4, or 8, according to the settings of the on-board switch SW2.

<i>SW2-A (left)</i>	<i>SW2-B (right)</i>	<i>divide by</i>
DOWN	DOWN	8
DOWN	UP	4
UP	DOWN	2
UP	UP	-1

Table A1: switch selectable division ratios

SIGNAL CONSTELLATIONS

PREPARATION	80
terminology	80
the quadrature modulator	81
encoding	81
demodulation	81
decoding	82
constellations	82
naming conventions	83
more information	83
EXPERIMENT	83
M-LEVEL ENCODER module	83
constellations	84
coding schemes	84
eye patterns	85
M-LEVEL DECODER module	85
eye diagrams	86
error checking	87
TUTORIAL QUESTIONS	88

SIGNAL CONSTELLATIONS

ACHIEVEMENTS: *an introduction to the M-LEVEL ENCODER and M-LEVEL DECODER modules; the signal constellations of m-QAM and m-PSK. Decoding.*

PREREQUISITES: *a theoretical introduction to m-QAM and m-PSK.*

ADVANCED MODULES: *M-LEVEL ENCODER, M-LEVEL DECODER, ERROR COUNTING UTILITIES, a total of two TUNEABLE LPF and two SEQUENCE GENERATORS.*

PREPARATION

This experiment will serve as an introduction to later experiments which use a quadrature amplitude modulator to generate m-QAM and m-PSK signals.

In these applications the modulator requires a pair of multi-level analog signals derived from a single serial binary data stream.

To derive these two signals TIMS uses the M-LEVEL ENCODER module.

At the demodulator a complementary module, the M-LEVEL DECODER, is used.

These two modules will be examined in this experiment, independently of the quadrature amplitude modulator and demodulator with which they will later be associated.

Their purpose will be better understood if you are first reminded of their role in a quadrature modulator and quadrature demodulator.

terminology

The two outputs from the M-LEVEL ENCODER are referred to as the **I** and **Q** signals. Here the '**I**' and the '**Q**' refer to **i**nphase and **q**uadrature, which describe the phase of the carriers of the DSBSC modulators to which they are connected.

The upper case '**M**' in the module names is intended to imply that the **I** and **Q** output signals are '**M**ulti-level'. This is not a common usage of the symbol '**M**'.

It is not the same as the lower case '**m**' used here in the abbreviations m-PSK and m-QAM. The '**m**' in these names refers specifically to the number of points in the constellation diagram (to be defined later), and is derived from the number of bits, **L**, in the frame (defined later), determined by the encoding process.

You will see that:

$$m = 2^L$$

the quadrature modulator

As a reminder, a block diagram of a quadrature modulator is shown in Figure 1. This configuration appeared in the experiment entitled *Phase division multiplex* (within *Volume A2 - Further & Advanced Analog Experiments*), and in Weaver's SSB systems. It is common to many communications systems, and will be seen again in later digital experiments.

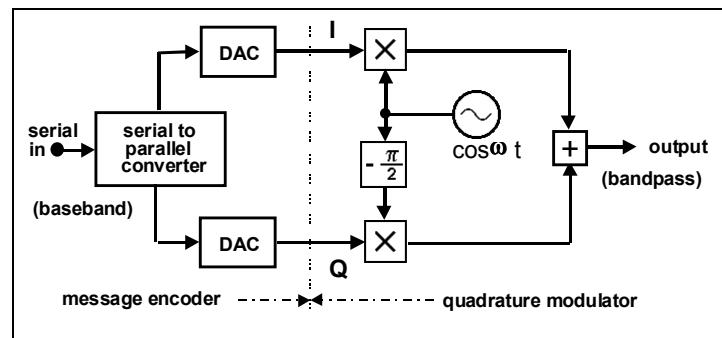


Figure 1: an m-QAM modulator.

encoding

To generate the two multi-level analog signals mentioned above the input serial binary data stream is segmented into frames (or binary words) of L bits each, in a serial-to-parallel converter.

For a particular choice of L there will be $m = 2^L$ unique words.

From each of these words is generated a unique pair of analog voltages, one of which goes to the I -path, and the other to the Q -path, of the quadrature modulator.

A typical arrangement is illustrated in block diagram form in Figure 1 above.

No bandlimiting is shown in Figure 1, but in practice this would be introduced either at the input to each multiplier (possibly in the form of a pulse shaping filter), or at the output of the adder, or both.

demodulation

A quadrature demodulator is illustrated in Figure 2. Remember the input signal is a pair of DSBSC, added in phase quadrature. It is the purpose of the demodulator to recover their individual messages, which are presented to the two inputs of the decoder. If the DSBSC phasing at the transmitter is ideally in quadrature, then the single phase adjustment shown is sufficient to separate the messages of the two signals.

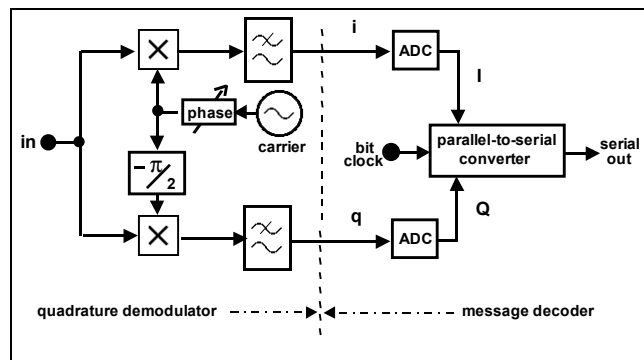


Figure 2: an m-QAM demodulator

decoding

Each arm of the decoder is presented with a bandlimited analog waveform.

The decoder has a bit clock input (stolen in the experiment, else derived from the incoming signal in practice) and knows beforehand the number of bit periods (L) in a frame.

Each waveform is sampled once per frame, and a decision made as to which of the possible levels it represents. This will give a unique pair of levels, which represents a binary word of L bits. This decoded word is output as a serial binary data stream.

constellations

Associated with these signals are phasor diagrams, and signal constellation diagrams.

The phasor diagram is one of the many ways in which some of the properties of these *bandpass* signals can be illustrated.

Each phasor represents the output signal during each of the frames.

The signal constellation diagram shows the location of the *tips* of these phasors on the complex plane.

It is displayed when the two *baseband* multi-level signals **I** and **Q** are connected to the X and Y inputs of an oscilloscope (in X-Y mode).

These signals can come from the encoder output, or from the decoder¹ input. The first of these shows the constellation under ideal conditions. The second shows the constellation after the signal has passed through the channel.

In the second case the display can be used to reveal much about the impairments suffered by the signal.

Like the eye diagram, the constellation diagram displays, in real time, the on-line signal. To obtain these diagrams there is no need to interrupt normal transmission.

¹ the decoding process is described later

Much research has gone into the optimum location of these points in the constellation, in order to obtain the most desirable properties - or combination of properties.

naming conventions

Typically the signal constellation is a symmetrical display. Depending upon the disposition of the points in the display so the resulting modulated signal has different properties, and is given different names.

For example, the points could be in a circle - such as in m-PSK, or in a square grid, as in m-QAM. These constellations are illustrated below in Figure 3, for the case $m = 8$. In these cases the binary serial data stream has been encoded using frames of three bits.

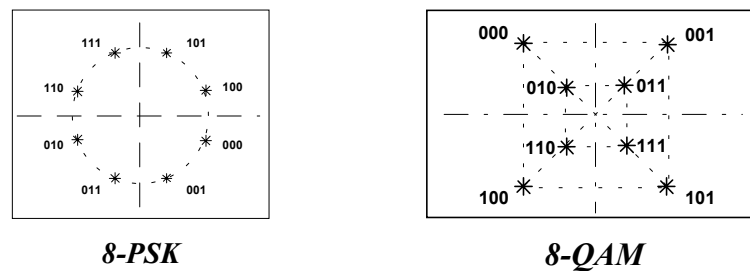


Figure 3: constellation diagrams

The three-bit words located near each point are the bits in the frame with which each point is associated.

more information

For further theoretical detail on these signals and systems see your Text book.

You can find more technical information about the M-LEVEL ENCODER and M-LEVEL DECODER modules in the *Advanced Modules User Manual*.

EXPERIMENT

M-LEVEL ENCODER module

The arrangement to be examined first is that designated as the 'message encoder' of Figure 1, together with a message source. These are modelled in Figure 4 below.

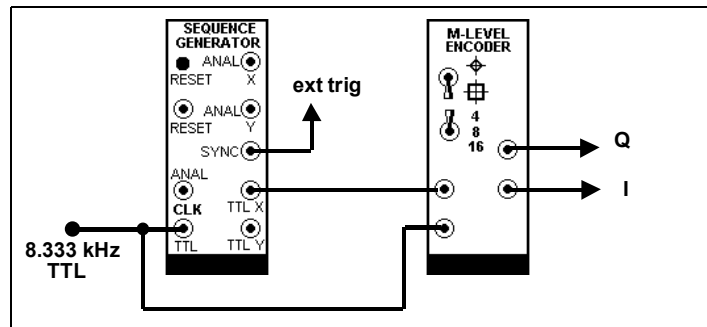


Figure 4: the encoder with 4-QAM selected

As shown, the input is a serial binary data stream from a SEQUENCE GENERATOR. The multilevel **I** and **Q** output signals would go to the quadrature modulator (typically preceded by identical lowpass filters).

***T1** obtain an M-LEVEL ENCODER module. Before plugging it in ensure that the on-board jumper J3 is in the 'NORMAL' position.*

The purpose of each of the sockets and controls on the front panel should be self-explanatory.

***T2** patch up the arrangement of Figure 4. Start with a short sequence from the SEQUENCE GENERATOR (both toggles of the on-board switch SW2 should be UP), and select 4-QAM from the M-LEVEL ENCODER.*

constellations

***T3** predict the appearance of the constellation diagram, and then display it on the oscilloscope (the **I** and **Q** signals connect to the X and Y inputs of the oscilloscope to represent the complex plane with the imaginary axis vertical).*

coding schemes

You will now deduce the coding scheme of the 4-QAM signal. This can be done by examining simultaneously the input data and each one of the **I** and **Q** output signals in turn. The encoder will have arbitrarily selected the frame start point in the incoming serial binary data stream. Each frame will contain two data bits (for the 4-QAM case).

The first requirement, when looking at the input serial binary data stream, is that you must decide where a frame starts. This would be easy if there was not a processing delay (of several clock periods at least) between the end of the frame and the start of the encoded **I** or **Q** output.

Some heuristics will be necessary.

Remember, you *do* know the frame length.

*T4 display the input serial stream and the **I** output signal. Deduce the coding scheme used to map the input data to the output. Repeat for the **Q** output. Record the magnitude of the delay between the frame and the corresponding encoded output (as a function of the input data clock period). There will not necessarily be the same delay for other constellations.*

As time permits the previous two Tasks could be repeated for other constellations. Note that, for larger constellations, it would be necessary to increase the sequence length. Explain.

T5 examine the constellations of each of the other signals available from the M-LEVEL ENCODER. Notice the result of using a short sequence.

eye patterns

T6 display the eye patterns for all of the possible signals from the encoder. Note and record the number and magnitude of the voltage levels involved. Remember, to view all possible levels, long sequences are necessary. Explain.

If you previously displayed the eye patterns before first bandlimiting the signals, so be it. But more representative patterns result if bandlimiting is first introduced.

T7 view the eye patterns of the previous Task with bandlimiting, if not already done so.

Having acquainted yourself with the encoder properties, those of the decoder may now be examined.

M-LEVEL DECODER module

The decoder would normally be provided with the inphase and quadrature outputs from a quadrature amplitude demodulator. These would be noisy, bandlimited baseband signals. Each must be ‘cleaned up’ and their absolute levels adjusted so as to be suitable for analog-to-digital decoding.

The ‘cleaning up’ and decoding is performed by the M-LEVEL DECODER module.

Figure 5 is a model of the m-QAM decoder shown in block diagram form in Figure 2. Its operation will now be examined.

The **I** and **Q** signals from the encoder are shown bandlimited by a pair of lowpass filters, the better to simulate the output of a typical quadrature demodulator.

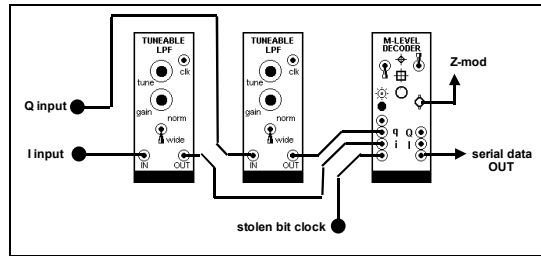


Figure 5: decoder - switched for 4-QAM

Obtain an M-LEVEL DECODER module. Before plugging it in ensure that the on-board RANGE jumper is in the 'HI' position (suits a clock between 4 kHz and 10 kHz). The purpose of each of the sockets and controls on the front panel should be self-explanatory, except perhaps for those associated with the HUNT facility. This will be introduced below.

T8 patch up the decoding model of Figure 5. Set the front panel switches to decode 4-QAM. Initially, at least, set both the TUNEABLE LPF modules to maximum bandwidth.

eye diagrams

The decision point can be moved with the front panel DECISION POINT control. The amount of movement is a little over one bit period. The point can be moved in coarse (one bit period) steps with the HUNT² button. Whilst the HUNT LED is alight (for about 1 second), further presses of the HUNT button are ineffective.

*T9 display an eye diagram of either the **Q** or **I** channel, and choose your decision point. This will provide an opportunity to observe the operation of the HUNT button.*

*T10 confirm the **I** and **Q** signals from the M-LEVEL DECODER are sample-and-held versions of the **i** and **q** inputs (determined at the sampling instant).*

These 'cleaned up' **I** and **Q** waveforms are passed to the analog-to-digital converter of the decoder.

The decoder makes its decisions on absolute voltage levels, so these must be set correctly. This involves varying the amplitude of the signals at the **i** and **q** inputs so that those at the **I** and **Q** outputs³ have a peak-to-peak amplitude of 5 volts. Ideally the minimum of this signal should be zero volts.

In this experiment the filter gain controls can be used for level adjustment.

In later experiments (especially when noise is present) you may choose to fine trim the zero level. In this case the minimum to maximum excursion should be set to

² for more detail on the HUNT LED see the *Advanced Modules User Manual*.

³ the **I** and **Q** signals (the result of a sample-and-hold operation on the **i** and **q** inputs) are the inputs to the analog-to-digital converter of the decoder

exactly 5 volts, and the absolute level of the minimum set to exactly 0 volts using the on-board trimming resistors RV1 and RV2.

*T11 vary the levels at the **i** and **q** inputs of the M-LEVEL DECODER using the gain controls of the TUNEABLE LPF modules. These should be adjusted so that the signals at the **I** and **Q** outputs have minimum to maximum values of 5 volts. The minimum should ideally be zero volts.*

*T12 display and record the absolute voltage levels of the **I** (and **Q**) signals for the various constellations available from the M-LEVEL ENCODER. See Tutorial Question Q3.*

*T13 confirm there is agreement between the **I** and **Q** outputs from the encoder and the **I** and **Q** outputs from the decoder.*

T14 confirm there is agreement between the serial data input to the M-LEVEL ENCODER and the corresponding output from the M-LEVEL DECODER.

With a short sequence it is relatively simple to check for data errors, using the oscilloscope, as in the last Task. With longer sequences it is more difficult, and tedious.

error checking

Instrumented error checking involves a comparison of a reference sequence and the decoded data stream.

Sequence comparison techniques have been examined in earlier experiments⁴. They use a synchronised and aligned reference sequence at the receiver. This sequence is compared, in an X-OR gate, with the decoded sequence.

Any output from the X-OR gate represents errors.

T15 implement an automated method of setting the system to confirm there is error free decoding. A suggested model is shown in Figure 6 below.

⁴ for example, in the experiment entitled *BER instrumentation macro model* in Volume D2 - Further and Advanced Digital Experiments.

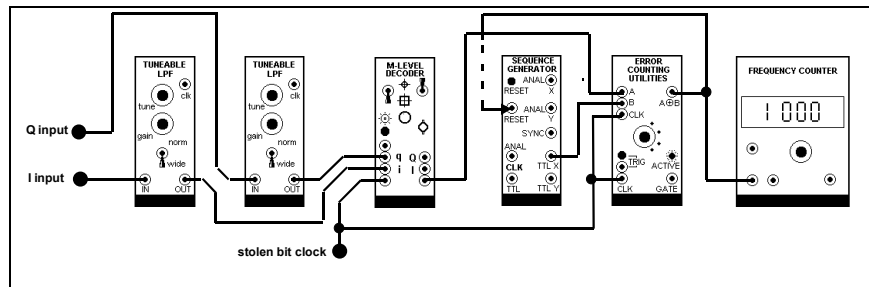


Figure 6: decoder with error counting

Notice that, during setting up, the GATE of the FREQUENCY COUNTER is left permanently open by there being no connection to the TTL ENABLE socket.

T16 repeat any or all of the above, as appropriate, with a longer sequence and different constellations.

TUTORIAL QUESTIONS

- Q1 sketch a section of an input sequence, and the corresponding encoded Q output signal from the M-LEVEL ENCODER switched to 4-QAM. Show clearly the framing, and the delay you measured between each frame and the coded output.*
- Q2 show, in tabular form, the relationships between each frame word, and the corresponding Q and I output levels from the M-LEVEL ENCODER, for 4-PSK.*
- Q3 how many levels are there from each of the outputs of the M-LEVEL ENCODER module for an 8-PSK signal? If these cover the range ± 2.5 volts, specify the levels for each of the points in the constellation of Figure 3. Repeat for other constellations. Compare with measurements.*

SAMPLING WITH SAMPLE AND HOLD

PREPARATION	90
A/D conversion	90
natural sampling	90
flat top sampling	90
message reconstruction by lowpass filtering	91
sample width	91
sample-and-hold sampling	92
EXPERIMENT	92
message reconstruction	93
two-tone test signal	94
aliasing	94
conclusion	95
TUTORIAL QUESTIONS	96

SAMPLING WITH SAMPLE AND HOLD

ACHIEVEMENTS: *investigation of the sample-and-hold operation as a first step towards digitization of an analog waveform. Message reconstruction by lowpass filtering.*

PREREQUISITES: *none*

ADVANCED MODULES: *INTEGRATE & DUMP*

PREPARATION

A/D conversion

Before it is possible to transmit analog information via a digital system the analog signal must first be transformed into a digital format. The *first step* in such a transformation typically involves a sampling process.

natural sampling

Natural sampling of an analog waveform (message) is examined in the experiment entitled *The sampling theorem* (within *Volume A1 - Fundamental Analog Experiments*).

Natural sampling takes a slice of the waveform, and the top of the slice preserves the shape of the waveform.

flat top sampling

A very common, and easily implemented method of sampling of an analog signal uses the sample-and-hold operation. This produces *flat top* samples.

Flat top sampling takes a slice of the waveform, but cuts off the top of the slice horizontally. The top of the slice does *not* preserve the shape of the waveform.

Figure 1 below contrasts the two methods.

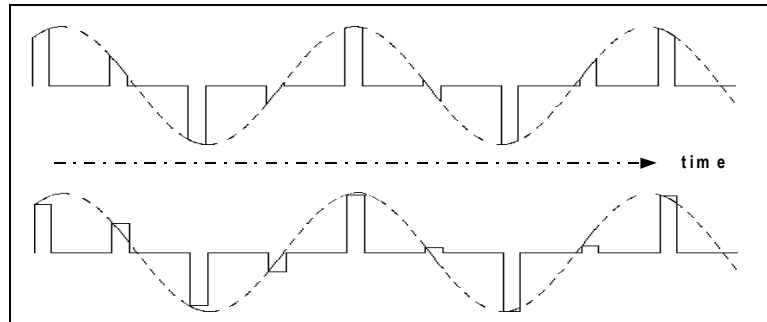


Figure 1: natural sampling (above) and flat top (below)

message reconstruction by lowpass filtering

In the experiment entitled *The sampling theorem* a simple analysis showed that there was *no distortion* of the message when reconstruction was implemented by lowpass filtering.

It will now be declared as an obvious fact:

if message reconstruction by lowpass filtering of natural samples results in no distortion, then there must be distortion when flat top pulses are involved.

Analysis of the distortion for flat top pulses will not be attempted here. Instead some observations will be made, and you can draw your own conclusions.

sample width

An important observation must be made. The pulse width determines the amount of energy in each pulse, and so can determine the amplitude of the reconstructed message. But, in a linear and noise free system, the width of the samples plays no part in determining the amount of distortion of a reconstructed message.

sample-and-hold sampling

The sample-and-hold operation is simple to implement, and is a very commonly used method of sampling in communications systems.

In its simplest form the sample is held until the next sample is taken. So it is of maximum width.

This is illustrated in Figure 2 below.

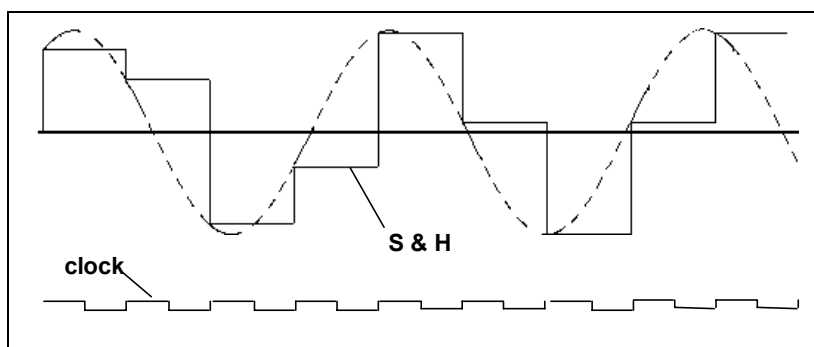


Figure 2: sampling by sample-and-hold (for full sample width)

In the above example the sampling instant is coincident with the rising edge of the clock signal.

In practice there may be a 'processing delay' before the stepped waveform is presented at the output. This is the case in the sub-system being examined in this experiment.

EXPERIMENT

There is a stand alone SAMPLE-AND-HOLD sub-system in the INTEGRATE & DUMP module. This will be used in the present experiment.

***T1** acquire an INTEGRATE & DUMP module. This is a multi-purpose module. Within it is a sub-system which performs sample-and-hold operations. Before plugging it in, set the on-board switch SW1 to the S&H 1 position ('0'). Analog signals connected to the input socket labelled I&D 1 will now undergo a sample-and-hold (S&H 1) operation, the result appearing at the I&D 1 output socket. Ignore the duplicate S&H 2 option available at the I&D 2 sockets.*

***T2** patch up the module according to Figure 3 below.*

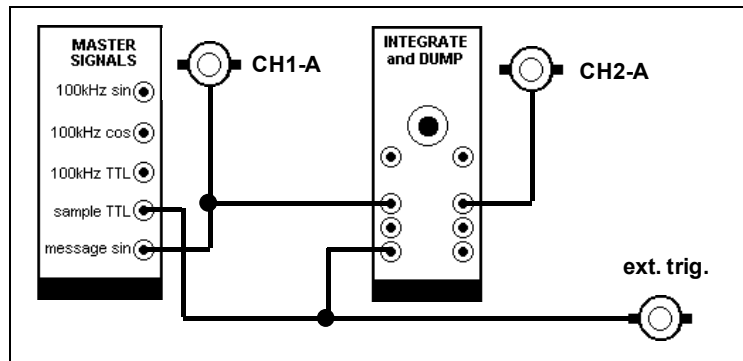


Figure 3: the TIMS model

For a stable view of both input and output it is convenient to use a message which is a submultiple of the sample clock frequency. Thus use the 2.03 kHz message (sinewave) from the MASTER SIGNALS module, together with the 8.333 kHz TTL clock.

***T3** select a sweep speed to show two or three periods of the message - say 0.1 ms/cm. Set equal gains of both channels - say 1 volt/cm. With the patching shown in Figure 3 you might expect to obtain oscilloscope displays similar to that of Figure 2. Try it.*

***T4** note the output from the socket labelled READY. Sketch it with respect to the clock and output signal, showing time relationships.*

There is a processing delay within the sample-and-hold sub-system. As a result, the two displays will be shifted relative in time. The ready signal occurs within the time during which the sample is available, and could be used to signal analog-to-digital (A/D) circuitry to start a conversion.

message reconstruction

Now that you have seen a sample-and-hold operation, you are ready to reconstruct the message from it. This is a lowpass filtering operation.

***T5** use a TUNEABLE LPF module to reconstruct the message. Decide on, then set, a 'suitable' bandwidth. Report your findings. Then read on:*

To what passband width did you set the filter ?

Remember, you are looking for any possible distortion components introduced by the sample-and-hold operation, and then the reconstruction process.

Since the message is at 2.03 kHz a passband of 3 kHz would be wide enough ?

Yes and no !

This would indeed be wide enough to pass the message, but it would not be wide enough to pass any harmonic distortion components.

But the filter passband could not be made wider than half the sampling frequency (else the Nyquist criterion would be violated), and that is not much more than the current message frequency. So something has to be changed.

Is a synchronous message necessary? Not any longer, after having seen the stationary sample-and-hold waveform. So why not use an AUDIO OSCILLATOR, set to its lowest frequency (about 300 Hz), and the 3 kHz LPF within the HEADPHONE AMPLIFIER module. This would give plenty of room for any distortion components to appear at the output. However, unless they are of significant amplitude, they may not be visible on the oscilloscope.

T6 *do as suggested above. Use the oscilloscope to view both the input and output sinewaves simultaneously. Synchronize the oscilloscope (externally) to the source of the message. As an engineering estimate, if the distortion is not obvious, then one could say the signal-to-distortion ratio is better than 30 dB (probably better than 40 dB).*

As well as one can judge the two waveforms are 'identical'? Could you estimate the amount of distortion introduced by the reconstruction process? See Tutorial Question Q1.

If there *was* visible distortion then one should check the 3 kHz LPF reconstruction filter - does it introduce its own distortion? Compare the message shape *before* sampling, *but via this filter*, as well as *after* reconstruction.

Could you attempt to *measure* the mount of distortion? See Tutorial Question Q2. The unwanted components will probably be hidden in the noise level; meaning the signal-to-distortion ratio is much better than 40 dB.

two-tone test signal

Testing for distortion with a single sine wave is perhaps not demanding enough. Should you try a two-tone test signal? The technique was introduced in the experiment entitled *Amplifier overload* (within *Volume A2 - Further & Advanced Analog Experiments*).

aliasing

With the 3 kHz LPF as the reconstruction filter, and an 8.333 kHz sample rate, there should be no sign of aliasing distortion.

To demonstrate aliasing distortion:

T7 *replace the 8.333 kHz sampling signal from the MASTER SIGNALS module with the TTL output from a VCO. Monitor the VCO frequency with the FREQUENCY COUNTER. Starting with the VCO set to its highest frequency on the LO range (about 15 kHz), slowly reduce it, while watching the reconstructed message waveshape. As soon as distortion is evident note the VCO frequency. Knowing the reconstruction filter amplitude characteristic, how does this agree with the Nyquist criterion? See Tutorial Question Q3.*

conclusion

You have seen that the sample-and-hold operation followed by a lowpass filter can reconstruct the signal, whose samples were taken, with ‘good’ accuracy. If you had available a spectrum analyser, or its equivalent, you would have been able to show that unwanted components were at least 40 dB below the wanted components when implemented with TIMS modules operating within their limits. So, for communications purposes, we might say message reconstruction is distortionless.

The sampling process is the first of two major steps in preparing an analog message for digital transmission. The second step is conversion of the sampled waveform to a series of digital numbers. This introduces a second source of distortion, due to the need for *quantization*. But quantization distortion can also be made negligible if sufficient quantization levels are used.

Sample-and-hold followed by amplitude quantization is examined in the experiments entitled *PCM encoding* and *PCM decoding* in this Volume.

TUTORIAL QUESTIONS

- Q1** *assuming a sinewave is accompanied by a small third harmonic component, how large would this have to be before its presence could be detected using only an oscilloscope? This question would not please the purists, because it raises more questions than it asks. But attempt an answer. You could even set up the signal using TIMS and **demonstrate** your reply.*
- Q2** *recall the experiment entitled **Modelling an equation** within Volume A1 - Fundamental Analog Experiments. There was demonstrated the cancellation of a component in a signal. Describe how this technique might be used in the present case to make a measurement of signal-to-distortion ratio.*
- Q3** *define the 'slot bandwidth' of a lowpass filter. Redefine the Nyquist criterion in terms of practical filter characteristics ¹.*
- Q4** *sample-and-hold (flat-top sampling) can be shown to introduce distortion of the message if it is reconstructed by using a lowpass filter alone. From your general reading, or otherwise, is it possible to eliminate this distortion by further message processing? **hint:** key words are aperture effect, $\sin x/x$ correction.*

¹ filter characteristics are defined in Appendix A of Volume A1.

PCM ENCODING

PREPARATION	98
PCM	98
PCM encoding.....	98
the PCM ENCODER module.....	100
front panel features.....	100
the TIMS PCM time frame.....	101
pre-calculations	101
EXPERIMENT	101
patching up	102
quantizing levels for 4-bit linear encoding.....	103
4-bit data format.....	104
7-bit linear encoding	104
companding.....	104
periodic messages.....	105
conclusions	105
TUTORIAL QUESTIONS	106
APPENDIX.....	107

PCM ENCODING

ACHIEVEMENTS: *introduction to pulse code modulation (PCM) and the PCM ENCODER module. Coding of a message into a train of digital words in binary format.*

PREREQUISITES: *an understanding of sampling, from previous experiments, and of PCM from course work or a suitable text. Completion of the experiment entitled **Sampling with SAMPLE & HOLD** (in this Volume) would be a distinct advantage.*

ADVANCED MODULES: *PCM ENCODER*

PREPARATION

PCM

This is an introductory experiment to pulse code modulation - PCM.

The experiment will acquaint you with the PCM ENCODER, which is one of the TIMS Advanced Modules. This module generates a PCM output signal from an analog input message.

In this experiment the module will be used in isolation; that is, it will not be part of a larger system. The formatting of a PCM signal will be examined in the time domain.

A later experiment, entitled *PCM decoding* (in this Volume), will illustrate the recovery of the analog message from the digital signal.

In another experiment, entitled *PCM TDM* (within *Volume D2 - Further & Advanced Digital Experiments*), the module will be part of a system which will generate a two-channel pulse code modulated time division multiplexed system (PCM TDM).

PCM encoding

The input to the PCM ENCODER module is an analog message. This must be constrained to a defined bandwidth and amplitude range.

The maximum allowable message bandwidth will depend upon the sampling rate to be used. The Nyquist criterion must be observed.

The amplitude range must be held within the ± 2.0 volts range of the TIMS ANALOG REFERENCE LEVEL. This is in keeping with the input amplitude limits set for all analog modules.

A step-by-step description of the operation of the module follows:

1. the module is driven by an external TTL clock.
2. the input analog message is *sampled* periodically. The *sample rate* is determined by the external clock.
3. the sampling is a *sample-and-hold* operation. It is internal to the module, and cannot be viewed by the user¹. What is held is the *amplitude* of the analog message *at the sampling instant*.
4. each sample amplitude is compared with a finite set of amplitude levels. These are distributed (uniformly, for *linear* sampling) within the range ± 2.0 volts (the TIMS ANALOG REFERENCE LEVEL). These are the system *quantizing* levels.
5. each quantizing level is assigned a *number*, starting from zero for the lowest (most negative) level, with the highest number being (L-1), where L is the available number of levels.
6. each sample is *assigned* a digital (binary) code word representing the number associated with the quantizing level which is closest to the sample amplitude. The number of bits 'n' in the digital code word will depend upon the number of quantizing levels. In fact, $n = \log_2(L)$.
7. the code word is *assembled into a time frame* together with other bits as may be required (described below). In the TIMS PCM ENCODER (and many commercial systems) a single extra bit is added, in the least significant bit position. This is alternately a *one* or a *zero*. These bits are used by subsequent decoders for frame synchronization.
8. the *frames* are transmitted serially. They are transmitted at the same rate as the samples are taken (but see Tutorial Question 3). The serial bit stream appears at the output of the module.
9. also available from the module is a synchronizing signal FS ('frame synch'). This signals the *end* of each data frame.

¹ the *sample and hold* operation is examined separately in the experiment entitled *Sampling with SAMPLE & HOLD* in this Volume.

the PCM ENCODER module

front panel features

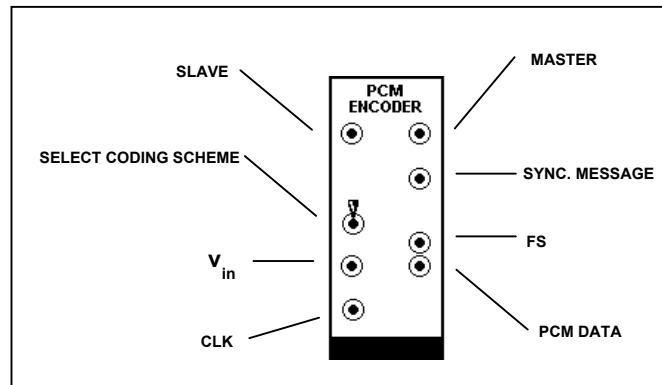


Figure 2: front panel layout of the PCM ENCODER

The front panel layout of the module is shown in Figure 2. Technical details are described in the *TIMS Advanced Modules User Manual*.

Note and understand the purpose of each of the input and output connections, and the three-position toggle switch. Counting from the top, these are:

- **SLAVE**: not used during this experiment. Do *not* connect anything to this input.
- **MASTER**: not used during this experiment. Do *not* connect anything to this output.
- **SYNC. MESSAGE**: periodic, ‘synchronized’, message. Either sinusoidal, or sinusoidal-like (‘sinuous’), its frequency being a sub-multiple of the MASTER CLOCK (being any one of four frequencies selected by an on-board switch SW2). A message synchronized to the system clock is convenient for obtaining stable oscilloscope displays. Having a recognisable shape (but being more complex than a simple sine wave) gives a qualitative idea of distortion during the decoding process (examined in a later experiment). See Table A-1 in the Appendix to this experiment for more details.
- **SELECT CODING SCHEME**: a three-position toggle switch which selects the 4-bit or 7-bit encoding scheme of the analog samples; or (together with an on-board jumper connection) the companding scheme.
- **FS**: frame synchronization, a signal which indicates the end of each data frame.
- **V_{in}**: the analog signal to be encoded.
- **PCM DATA**: the output data stream, the examination of which forms the major part of this experiment.
- **CLK**: this is a TTL (red) input, and serves as the MASTER CLOCK for the module. Clock rate must be 10 kHz or less. For this experiment you will use the 8.333 kHz TTL signal from the MASTER SIGNALS module.

the TIMS PCM time frame

Each binary word is located in a *time frame*. The time frame contains eight *slots* of equal length, and is eight clock periods long. The slots, from first to last, are numbered 7 through 0. These slots contain the bits of a binary word. The least significant bit (LSB) is contained in slot 0.

The LSB consists of alternating *ones* and *zeros*. These are placed ('embedded') in the frame by the encoder itself, and cannot be modified by the user. They are used by subsequent decoders to determine the location of each frame in the data stream, and its length. See the experiment entitled *PCM decoding* (in this Volume).

The remaining seven slots are available for the bits of the binary code word. Thus the system is capable of a resolution of seven-bits maximum. This resolution, for purposes of experiment, can be reduced to four bits (by front panel switch). The 4-bit mode uses only five of the available eight slots - one for the embedded frame synchronization bits, and the remaining four for the binary code word (in slots 4, 3, 2, and 1).

pre-calculations

You will be using an 8.333 kHz master clock. Answer Tutorial Question Q1 now, *before* commencing the experiment.

EXPERIMENT

The only module required for this experiment is a TIMS PCM ENCODER.

It is not necessary, for this experiment, to become involved with *how* the PCM ENCODER module achieves its purpose. What will be discovered is *what* it does under various conditions of operation.

The module is capable of being used in two modes: as a stand-alone PCM encoder, for one channel, or, with modifications to the data stream, as part of a two-channel time division multiplexed (TDM) PCM system.

Operation as a single channel PCM encoder is examined in this experiment.

Before plugging the module in:

T1 select the TIMS companding *A₄-law* with the on-board COMP jumper (in preparation for a later part of the experiment).

T2 locate the on-board switch SW2. Put the LEFT HAND toggle DOWN and the RIGHT HAND toggle UP. This sets the frequency of a message from the module at SYNC. MESSAGE. This message is synchronized to a sub-multiple of the MASTER CLOCK frequency. For more detail see the Appendix to this experiment.

patching up

To determine some of the properties of the analog to digital conversion process it is best to start with a DC message. This ensures completely stable oscilloscope displays, and enables easy identification of the quantizing levels.

Selecting the 4-bit encoding scheme reduces the number of levels (2^4) to be examined.

T3 insert the module into the TIMS frame. Switch the front panel toggle switch to 4-BIT LINEAR (ie., no companding).

T4 patch the 8.333 kHz TTL SAMPLE CLOCK from the MASTER SIGNALS module to the CLK input of the PCM ENCODER module.

T5 connect the V_{in} input socket to ground of the variable DC module.

T6 connect the frame synchronization signal FS to the oscilloscope ext. synch. input.

T7 on CH1-A display the frame synchronization signal FS. Adjust the sweep speed to show three frame markers. These mark the **end** of each frame.

T8 on CH2-A display the CLK signal.

T9 record the number of clock periods per frame.

Currently the analog input signal is zero volts (V_{in} is grounded). Before checking with the oscilloscope, consider what the PCM output signal might look like. Make a sketch of this signal, fully annotated. Then:

T10 on CH2-B display the PCM DATA from the PCM DATA output socket.

Except for the alternating pattern of '1' and '0' in the frame marker slot, you might have expected nothing else in the frame (all zeros), because the input analog signal is at zero volts. But you do not know the coding scheme.

There is an analog *input* signal to the encoder. It is of zero volts. This will have been coded into a 4-bit binary *output* number, which will appear in *each* frame. It need not be '0000'. The *same* number appears in *each* frame because the analog input is *constant*.

Your display should be similar to that of Figure 3 below, except that this shows five frames (too many frames on the oscilloscope display makes bit identification more difficult).

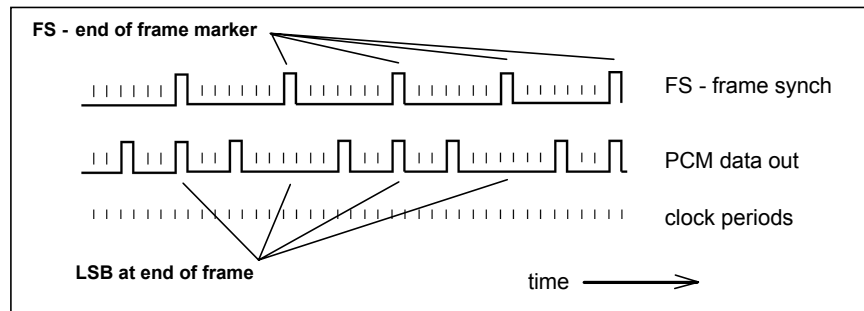


Figure 3: 5 frames of 4-bit PCM output for zero amplitude input

Knowing:

1. the number of slots per frame is 8
2. the location of the least significant bit is coincident with the end of the frame
3. the binary word length is four bits
4. the first three slots are 'empty' (in fact filled with zeros, but these remain unchanged under all conditions of the 4-bit coding scheme)

then:

T11 identify the binary word in slots 4, 3, 2, and 1.

quantizing levels for 4-bit linear encoding

You will now proceed to determine the quantizing/encoding scheme for the 4-bit linear case.

T12 remove the ground connection, and connect the output of the VARIABLE DC module to V_{in} . Sweep the DC voltage slowly backwards and forwards over its complete range, and note how the data pattern changes in discrete jumps.

T13 if you have a WIDEBAND TRUE RMS METER module use this to monitor the DC amplitude at V_{in} - otherwise use the oscilloscope (CH1-B). Adjust V_{in} to its maximum negative value. Record the DC voltage and the pattern of the 4-bit binary number.

T14 slowly increase the amplitude of the DC input signal until there is a sudden change to the PCM output signal format. Record the format of the new digital word, and the input amplitude at which the change occurred.

T15 continue this process over the full range of the DC supply.

T16 draw a diagram showing the quantizing levels and their associated binary numbers.

4-bit data format

From measurements made so far you should be able to answer the questions:

- what is the sampling rate ?
- what is the frame width ?
- what is the width of a data bit ?
- what is the width of a data word ?
- how many quantizing levels are there ?
- are the quantizing levels uniformly (linearly) spaced ?

7-bit linear encoding

T17 change to 7-bit linear encoding by use of the front panel toggle switch.

It would take a long time to repeat all of the above Tasks for the 7-bit encoding scheme. Instead:

*T18 make sufficient measurements so that you can answer all of the above questions in the section titled **4-bit data format** above. Making one or two assumptions (such as ?) you should be able to deduce the coding scheme used.*

companding

This module is to be used in conjunction with the PCM DECODER in a later experiment. As a pair they have a *companding* option. There is compression in the encoder, and expansion in the decoder. In the encoder this means the quantizing levels are closer together for small input amplitudes - that is, in effect, that the input amplitude peaks are compressed during encoding. At the decoder the 'reverse action' is introduced to restore an approximate linear input/output characteristic.

It can be shown that this sort of characteristic offers certain advantages, especially when the message has a high peak-to-average amplitude characteristic, as does speech, and where the signal-to-noise ratio is not high.

This improvement will not be checked in this experiment. But the existence of the non-linear quantization in the encoder will be confirmed.

In a later experiment, entitled *PCM decoding* (in this Volume), it will be possible to check the input/output linearity of the modules as a compatible pair.

T19 change to 4-bit companding by use of the front panel toggle switch.

T20 the T1MS A₄ companding law has already been selected (first Task). Make the necessary measurements to determine the nature of the law.

periodic messages

Although the experiment is substantially complete, you may have wondered why a periodic message was not chosen at any time. Try it.

T21 take a periodic message from the SYNC. MESSAGE socket. This was set as the second Task.

T22 adjust the oscilloscope to display the message. Record its frequency and shape. Check if these are compatible with the Nyquist criterion; adjust the amplitude if necessary with one of the BUFFER AMPLIFIERS.

T23 now look at the PCM DATA output. Synchronize the oscilloscope (as previously) to the frame (FS) signal. Display two or three frames on CH1-A, and the PCM DATA output on CH2-A.

You will see that the data signal reveals very little. It consists of many overlaid digital words, all different.

One would need more sophisticated equipment than is assumed here (a digital analyzer, a storage oscilloscope, ability to capture a single frame, and so on) to deduce the coding and quantizing scheme from such an input signal.

conclusions

What is the advantage of 7-bit over 4-bit encoding? Of what use is companding? From your measurements alone these questions cannot be answered.

These and other questions will be addressed in the experiment entitled *PCM decoding* (in this volume - but see the Tutorial Questions).

The findings of this experiment will be required in later PCM experiments. These will involve decoding of the data stream, an investigation of companding, and time multiplexing of the outputs from two PCM ENCODER modules.

TUTORIAL QUESTIONS

- Q1** from your knowledge of the PCM ENCODER module, obtained during preparation for the experiment, calculate the sampling rate of the analog input signal. Show that it is the same for both the 4-bit and the 7-bit coding schemes. What can you say about the bandwidth of an input analog signal to be encoded ?
- Q2** define what is meant by the data 'frame' in this experiment. Draw a diagram showing the composition of a frame for:
- a) the 4-bit coding scheme
 - b) the 7-bit coding scheme
- Q3** it is possible to transmit each frame at a much slower rate than it was produced (and, of course, recover the original message as well). Explain how this might be done. When might this be an advantage ?
- Q4** explain why a DC message gives a stable oscilloscope display of the PCM DATA output. Why is the display 'unstable' when a sine wave (for example) is the message ?
- Q5** for the 4-bit encoder draw a diagram showing the amplitude quantization levels and the corresponding binary numbers used to encode them. Describe how this information was obtained experimentally.
- Q6** two PCM signals can be combined to produce a time division multiplexed (PCM TDM) signal. With the measurements so far performed this does not seem (and indeed, is not) possible with two PCM ENCODER modules ! Why is this so ? Suggest what changes could be made to the module to implement PCM TDM².
- Q7** if you have studied the principles of companding in your course, describe its advantages. Then, if not already done so, plot the shape of the TIMS compression law introduced by the companding operation you measured. Compare this with published information about the 'A' and 'μ' companding laws used respectively in Europe and the USA.

² in a later experiment it will be seen that suitable modifications to the data stream have been introduced so that a two-channel PCM TDM can be modelled.

APPENDIX

For a MASTER CLOCK of 8.333 kHz, Table A-1 below gives the frequencies of the synchronized message at the SYNC. MESSAGE output for the setting of the on-board switch SW2.

For other clock frequencies the message frequency can be calculated by using the 'divide by' entry in the Table.

These messages are periodic, but not necessarily sinusoidal in shape. The term 'sinuous' means sine-like.

<i>LH toggle</i>	<i>RH toggle</i>	<i>divide clock by</i>	<i>freq with 8.333kHz clock</i>	<i>approx. ampl. and waveform</i>
UP	UP	32	260.4 Hz	0.2 V_{pp} sine
DOWN	UP	64	130.2 Hz	2.0 V_{pp} sine
UP	DOWN	128	65.1 Hz	4.0 V_{pp} sinuous
DOWN	DOWN	256	32.6 Hz	4.0 V_{pp} sinuous

Table A-1

PCM DECODING

PREPARATION	110
signal source	110
clock synchronization.....	110
frame synchronization	110
companding	111
PCM decoding.....	111
the TIMS PCM DECODER module	112
EXPERIMENT	113
the transmitter (encoder)	113
the receiver (decoder)	114
a DC message	114
a periodic message	115
message reconstruction	116
companding	117
frame synchronization	117
TUTORIAL QUESTIONS	118
APPENDIX.....	119
automatic frame synchronization	119

PCM DECODING

ACHIEVEMENTS: *decoding of a PCM signal. Determination of the quantizing scheme used at the encoder. Message reconstruction. Introduction to companding; comparison of 7-bit linear with 4-bit companded PCM.*

PREREQUISITES: *completion of the experiment entitled **PCM encoding** in this Volume. An appreciation of the principles of companding.*

ADVANCED MODULES: *A PCM ENCODER and a PCM DECODER (version 2 preferable).*

PREPARATION

signal source

The signal to be decoded¹ in this experiment will be provided by you, using the PCM ENCODER module as set up in the experiment entitled *PCM encoding*. The format of the PCM signal is described there. You should have already completed that experiment.

clock synchronization

A clock synchronization signal will be stolen from the encoder.

frame synchronization

automatic

In the PCM DECODER module there is circuitry which automatically identifies the location of each frame in the serial data stream. To do this it collects groups of eight data bits and looks for the repeating pattern of alternate ones and zeros placed there (embedded) by the PCM ENCODER in the LSB position.

It can be shown that such a pattern cannot occur elsewhere in the data stream provided that the original bandlimited analog signal is sampled at or below the Nyquist rate.

¹ it is common practice to refer to messages being *demodulated* from analog signals, and *decoded* from digital signals.

When the embedded pattern is found an ‘end of frame’ synchronization signal FS is generated, and made available at the front panel.

The search for the frame is continuously updated. Why ?

Under noisy conditions (not relevant for this particular experiment) the reliability of the process will depend upon the size of the group of frames to be examined. This can be set by the on-board switch SW3 of the PCM DECODER module. See *Table A-1* in the Appendix to this experiment for details.

stolen

Frame synchronization can also be achieved, of course, by ‘stealing’ the synchronization signal, FS, from the PCM ENCODER module. Use of this signal would assume that the clock signal to the PCM DECODER is of the correct phase. This is assured in this experiment, but would need adjustment if the PCM signal is transmitted via a bandlimited channel (see Tutorial Question 0). Hence the embedded frame synchronization information.

companding

You should prepare by reading something about the principles of *companding*. You will already be aware that the PCM ENCODER module can incorporate compression into its encoding scheme. The PCM DECODER module can introduce the complementary expansion. The *existence* of these characteristics will be confirmed, but their *effectiveness* in intelligibility enhancement (when speech is the message) is not examined.

PCM decoding

The PCM DECODER module is driven by an external clock. This clock signal is synchronized to that of the transmitter. For this experiment a ‘stolen’ clock will be used. The source of frame timing information has been discussed above.

Upon reception, the PCM DECODER:

1. extracts a frame synchronization signal FS from the data itself (from the embedded alternate ones and zeros in the LSB position), or uses an FS signal stolen from the transmitter (see above).
2. extracts the binary number, which is the coded (and quantized) amplitude of the sample from which it was derived, from the frame.
3. identifies the quantization level which this number represents.
4. generates a voltage proportional to this amplitude level.
5. presents this voltage to the output V_{out} . The voltage appears at V_{out} for the duration of the frame under examination.
6. message reconstruction can be achieved, albeit with some distortion, by lowpass filtering. A built-in reconstruction filter is provided in the module.

encoding

At the encoder the sample-and-hold operation (before encoding) is executed periodically. It produces a rectangular pulse form². Each pulse in the waveform is of *exactly* the same amplitude as the message *at the sampling instant*.

But *it is not possible* to recover a *distortionless* message from these samples. They are *flat top*, rather than *natural* samples.

Call this the sampling distortion.

At the encoder the amplitude of this waveform was then *quantized*. It is still a rectangular pulsed waveform, but the amplitude of each pulse will, in general, be in error by a small amount. Call this waveform $s(t)$.

This was examined in the experiment entitled *Sampling with SAMPLE & HOLD* (in this Volume), to which you should refer.

decoding

The voltage at V_{out} of the decoder is *identical with* $s(t)$ above. The decoder itself has introduced no distortion of the received signal.

But $s(t)$ is already an inexact version of the sample-and-hold operation at the encoder. This will give rise to *quantization distortion* as well as the *sampling distortion* already mentioned.

You should read about these phenomena in a Text book.

the TIMS PCM DECODER module

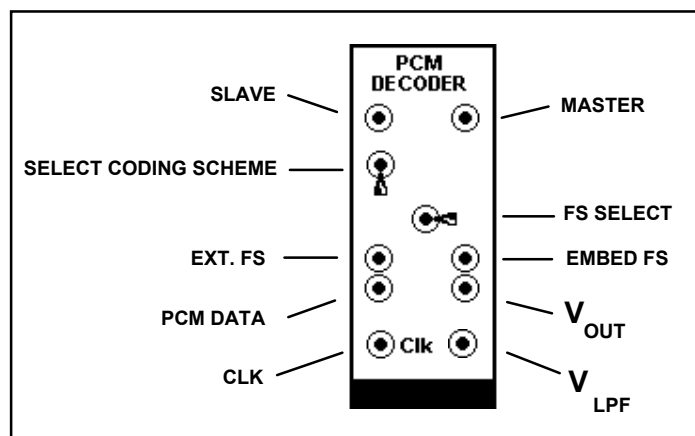


Figure 3: front panel layout of the PCM DECODER

A TIMS PCM DECODER module will be used for decoding.

The front panel of this module is shown in Figure 3. Technical details are described in the *TIMS Advanced Modules User Manual*.

² if the sample is held for as long as the sampling period, it is a stepped waveform. If the sample is held for a shorter time it is a rectangular waveform (or pulseform). It need only be held long enough for the quantizer to make its decision about which of the available (quantized) amplitudes to allocate to the sample.

Note and understand the purpose of the input and output connections, and the toggle switches. Counting from the top, these are:

- **SLAVE:** not used during this experiment. Do *not* connect anything to this input.
- **MASTER:** not used during this experiment. Do *not* connect anything to this output.
- **SELECT CODING SCHEME:** a three position toggle which selects the coding scheme used by the signal to be decoded
- **FS SELECT:** a two-position toggle switch which selects the method of obtaining the frame synchronization signal (FS) either external at (EXT.FS), or derived internally from the embedded information in the received PCM itself (EMBED FS).
- **EXT. FS:** connect an external frame sync. signal here if this method of frame synchronization is to be used.
- **EMBED FS:** if the frame synch. signal is derived internally from the embedded information, it is available for inspection at this output.
- **PCM DATA:** the PCM signal to be decoded is connected here.
- **V_{OUT}:** the decoded PCM signal.
- **CLK:** this is a TTL (red) input, and serves as the MASTER CLOCK for the module. Clock rate must be 10 kHz or less. For this experiment you will use the 8.333 kHz TTL signal from the MASTER SIGNALS module.

EXPERIMENT

the transmitter (encoder)

A suitable source of PCM signal will be generated using a PCM ENCODER module. This module was examined in the experiment entitled *PCM encoding*.

You should set it up before patching up the demodulator.

T1 before plugging in PCM ENCODER module, set the toggles of the on-board SYNC MESSAGE switch SW2. Set the left hand toggle DOWN, and the right hand toggle UP. This selects a 130 Hz sinusoidal message, which will be used later. Now insert the module into the TIMS system.

T2 use the 8.333 kHz TTL signal from the MASTER SIGNALS module for the CLK.

T3 select, with the front panel toggle switch, the 4-bit LINEAR coding scheme.

T4 synchronize the oscilloscope 'externally' to the frame synchronization signal at FS. Set the sweep speed to 0.5 ms/cm (say). This should show a few frames on the screen.

T5 connect CH1-A of the SCOPE SELECTOR to the PCM OUTPUT of the PCM ENCODER.

T6 we would like to recognise the PCM DATA out signal. So choose a 'large' negative DC for the message (from the VARIABLE DC module). From previous work we know the corresponding code word is '0000', so only the embedded alternating '0' and '1' bits (for remote FS) in the LSB position should be seen. Confirm this. They should be 1920 ms apart. Confirm this both by measurement and calculation !

T7 vary the DC output and show the appearance of new patterns on CH1-A. When finished, return the DC to its maximum negative value (control fully anti-clockwise).

The PCM signal is now ready for transmission. In a later experiment the PCM signal will be sent via a noisy, bandlimited channel. For the present it will be connected directly to a TIMS PCM DECODER module.

the receiver (decoder)

T8 use the front panel toggle switch to select the 4-bit LINEAR decoding scheme (to match that of the transmitter)

T9 'steal' an 8.333 kHz TTL clock signal from the transmitter and connect it to the CLK input.

T10 in the first instance 'steal' the frame synchronization signal FS from the transmitter by connecting it to the frame synchronization input FS of the receiver. At the same time ensure that the FS SELECT toggle switch on the receiver is set to EXT. FS.

T11 ensure both channels of the oscilloscope are set to accept DC; set their gains to 1 volt/cm. With their inputs grounded set their traces in the centre of their respective halves of the screen. Remove the grounds.

T12 connect CH2-A to the sample-and-hold output of the PCM DECODER.

!

a DC message

You are now ready to check the overall transmission from transmitter input to decoder output. The message is a DC signal.

T13 connect the PCM DATA output signal from the transmitter to the PCM DATA input of the receiver.

T14 slowly vary the DC output from the VARIABLE DC module back and forth over its complete range. Observe the behaviour of the two traces. The input to the encoder moves continuously. The output from the decoder moves in discrete steps. These are the 16 amplitude quantizing steps of the PCM ENCODER.

You are observing the source of quantizing noise. The output can take up only one of 16 predetermined values.

T15 draw up a table relating input to output voltages.

You can now see the number of quantizing levels at the transmitter, and their values.

T16 compare the quantizing levels just measured with those determined in the experiment entitled **PCM encoding**.

T17 reset the coding scheme on both modules to 7-bit. Sweep the input DC signal over the complete range as before. Notice the 'granularity' in the output is almost un-noticeable compared with the 4-bit case. There are now 2^7 rather than 2^4 steps over the range.

a periodic message

It was not possible, when examining the PCM ENCODER in the experiment entitled *PCM encoding*, to see the sample-and-hold waveform within the *encoder*. But you have just been looking at it (assuming perfect decoding) at the output of the *decoder*.

With a periodic message its appearance may be more familiar to you.

T18 change to a periodic message ³ by connecting the SYNC MESSAGE of the PCM ENCODER, **via** a BUFFER AMPLIFIER, to its input V_{in} . An amplitude of 2 V_{pp} is suitable. Slow down the oscilloscope sweep speed to 1 ms/cm. Observe and record the signal at CH2-A.

When you agree that what you see is what you expected to see, prepare to make a change and predict the outcome.

³ the message was set up in Task 1 to be a 130 Hz sinewave, synchronized to the sampling rate

Currently the encoding scheme is generating a 4-bit digital word for each sample.

What would be the change to the waveform, now displaying on CH2-A, if, at the encoder, the coding scheme was changed from 4-bit to 7-bit ?

Sketch your answer to this question - show the waveform *before* and then *after* the change.

T19 *change the coding scheme from 4-bit to 7-bit. That is, change the front panel toggle switch of **both** the PCM ENCODER **and** the PCM DECODER from 4-bit to 7-bit. Observe, record, and explain the change to the waveform on CH2-A.*

When satisfied, proceed.

message reconstruction

You can see, qualitatively, that the output is related to the input. The message could probably be recovered from this waveform. But it would be difficult to predict with what accuracy.

Lowpass filtering of the waveform at the output of the decoder will reconstruct the message, although theory shows that it will not be perfect. It will improve with the number of quantizing levels.

What amplitude characteristic is required for the reconstruction filter ? See Tutorial Question Q3.

If any distortion components are present they would most likely include harmonics of the message. If these are to be measurable (visible on the oscilloscope, in the present case), then they must not be removed by the filter and so give a false indication of performance. Recall the experiment entitled *Amplifier overload* (within *Volume A2 - Further & Advanced Analog Experiments*).

So we could look for harmonics in the output of the filter. But we do not have conveniently available a spectrum analyzer.

An alternative is to use a two-tone test message. Changes to its shape (especially its envelope) are an indication of distortion, and are more easily observed (with an oscilloscope) than when a pure sinewave is used. It will be difficult to make one of these for this experiment, because our messages have been restricted to rather low frequencies, which are outside the range of most TIMS modules.

But there is provided in the PCM ENCODER a message with a shape slightly more complex than a sinewave. It can be selected with the switch SW2 on the encoder circuit board. Set the left hand toggle UP, and the right hand toggle DOWN. See the Appendix to the experiment entitled *PCM encoding* for more details.

A message reconstruction LPF is installed in the PCM DECODER module (version 2 and above). If you do not have such a module then bypass the next two Tasks.

T20 *change to the complex message from the PCM ENCODER as described above.*

T21 include the built-in LPF in the output of the PCM DECODER, and observe the reconstructed message. Make comparisons between the 4-bit linear and the 7-bit linear coding schemes. Try different message amplitudes into the PCM ENCODER. Can you observe any distortion? Record your observations.

If you think the LPF itself might have introduced some distortion, you could check by connecting the complex message to its input direct, and observing the output.

companding

It is now time to verify the companding algorithm installed in the encoder.

T22 use the front panel toggle switches (on both modules) to select 4-bit companding. Use both 'low' and 'high' level messages into the PCM ENCODER. Check the quantizing characteristic. Record your observations and comment upon them.

Because of the speed limitations of the PCM modules it is not possible to use speech as the message, and so to observe the effects of companding. The effective bandwidth of the system is not wide enough.

See Tutorial Question Q7.

frame synchronization

In all of the above work the frame synchronization signal FS has been stolen from the encoder (as has been the clock signal). This was not necessary.

The PCM ENCODER has circuitry for doing this automatically. It looks for the alternating '0' and '1' pattern embedded as the LSB of each frame. It is enabled by use of the FS SELECT front panel toggle switch. Currently this is set to EXT FS.

T23 change the FS SELECT switch on the front panel of the PCM DECODER module from EXT FS to EMBED. Notice that frame synchronization is re-established after a 'short time'. Could you put an upper limit on this time? See Tutorial Question Q4.

TUTORIAL QUESTIONS

- Q1** in the present experiment a 'stolen' clock signal was used. Why would transmission of the PCM signal via a bandlimited channel necessitate phase adjustment of this stolen clock signal to the PCM DECODER ?
- Q2** sketch the waveforms at the output V_{out} from the decoder, for the 4-bit and the 7-bit linear encoding scheme (and a 'large amplitude' sinusoidal, synchronous message at the encoder). A 'sketch' might show these as being the same, but a more accurate drawing would show more clearly the difference. Explain.
- Q3** how would you arrive at a specification for the reconstruction filter used in this experiment ?
- Q4** from the information in Table A-1 make some quantitative comments on the length of time the built in circuitry of the PCM DECODER would take to recover the frame synchronization signal FS from the incoming data stream. Were you able to verify this by observation ?
- Q5** two sources of distortion of the reconstructed message have been identified; they were called sampling distortion and quantizing distortion.
- a) assuming a sample-and-hold type sampler, what can be done about minimizing sampling distortion ?
 - b) what can be done about minimizing quantizing distortion ?
- Q6** quantizing distortion decreases with the number of quantizing levels available. There is usually a price to be paid for such an option. What would this be ? Was that apparent in the present experiment ? Explain.
- Q7** companding is claimed to offer certain advantages. What are they ? Were you able to demonstrate any of these during the experiment. Explain.

APPENDIX

automatic frame synchronization

The PCM DECODER module has built in circuitry for locating the position of each frame in the serial data stream. The circuitry looks for the embedded and alternating '0' and '1' in the LSB position of each frame.

The search is made by examining a section of data whose length is a multiple of eight bits.

The length of this section can be changed by the on-board switch SW3. Under noisy conditions it is advantageous to use longer lengths.

The switch settings are listed in Table A-1 below.

left toggle	right toggle	groups of eight bits
UP	UP	4
UP	DOWN	8
DOWN	UP	16
DOWN	DOWN	32

Table A-1: synchronization search length options

DELTA MODULATION

PREPARATION	122
principle of operation.....	122
block diagram.....	122
step size calculation.....	124
slope overload and granularity.....	124
slope overload	124
granular noise	125
noise and distortion minimization	126
EXPERIMENT	126
setting up.....	126
slope overload.....	129
the ADAPTIVE CONTROL signal	129
the output	130
complex message	131
TUTORIAL QUESTIONS.....	132
APPENDIX	133
a ‘complex’ message.....	133

DELTA MODULATION

ACHIEVEMENTS: *an introduction to the basic delta modulator; to observe effects of step size and sampling clock rate change; slope overload and granular noise.*

PREREQUISITES: *some exposure to the principles of delta modulation in course work*

ADVANCED MODULES: *DELTA MODULATION UTILITIES, WIDEBAND TRUE RMS METER*

PREPARATION

principle of operation

Delta modulation was introduced in the 1940s as a simplified form of pulse code modulation (PCM), which required a difficult-to-implement analog-to-digital (A/D) converter.

The output of a delta modulator is a bit stream of samples, at a relatively high rate (eg, 100 kbit/s or more for a speech bandwidth of 4 kHz) the value of each bit being determined according as to whether the input message sample amplitude has increased or decreased relative to the previous sample. It is an example of differential pulse code modulation (DPCM).

block diagram

The operation of a delta modulator is to periodically sample the input message, to make a comparison of the current sample with that preceding it, and to output a single bit which indicates the sign of the difference between the two samples. This in principle would require a sample-and-hold type circuit.

De Jager (1952) hit on an idea for dispensing with the need for a sample and hold circuit. He reasoned that if the system *was* producing the desired output then this output could be sent back to the input and the two analog signals compared in a comparator. The output is a delayed version of the input, and so the comparison is in effect that of the current bit with the previous bit, as required by the delta modulation principle.

Figure 1 illustrates the basic system in block diagram form, and this will be the modulator you will be modelling.

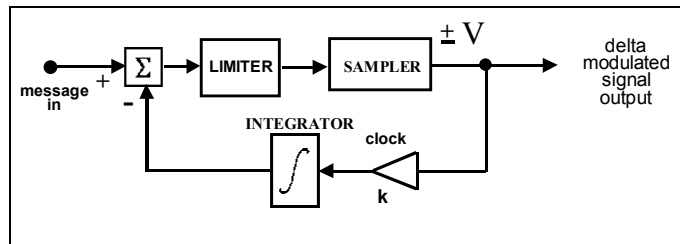


Figure 1: basic delta modulator

The system is in the form of a feedback loop. This means that its operation is not necessarily obvious, and its analysis non-trivial. But you can build it, and confirm that it does behave in the manner a delta modulator should.

The system is a continuous time to discrete time converter. In fact, it is a form of analog to digital converter, and is the starting point from which more sophisticated delta modulators can be developed.

The sampler block is clocked. The output from the sampler is a bipolar signal, in the block diagram being either $\pm V$ volts. This is the delta modulated signal, the waveform of which is shown in Figure 2. It is fed back, in a feedback loop, via an integrator, to a summer.

The integrator output is a sawtooth-like waveform, also illustrated in Figure 2. It is shown overlaid upon the message, of which it is an approximation.

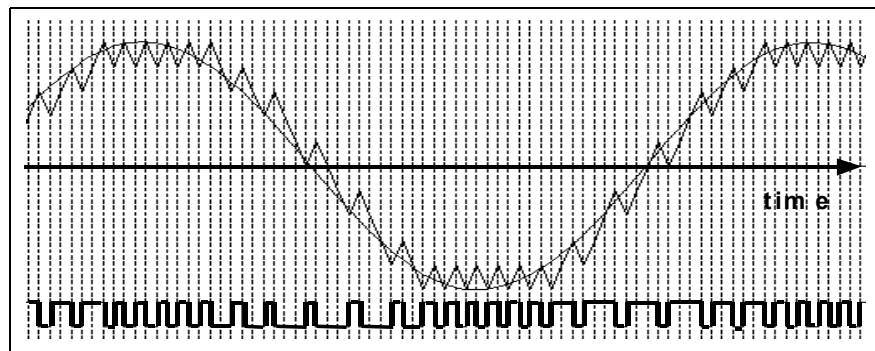


Figure 2: integrator output superimposed on the message with the delta modulated signal below

The sawtooth waveform is subtracted from the message, also connected to the summer, and the difference - an error signal - is the signal appearing at the summer output.

An amplifier is shown in the feedback loop.. This controls the loop gain. In practice it may be a separate amplifier, part of the integrator, or within the summer. It is used to control the size of the 'teeth' of the sawtooth waveform, in conjunction with the integrator time constant.

When analysing the block diagram of Figure 1 it is convenient to think of the summer having unity gain between both inputs and the output. The message comes in at a fixed amplitude. The signal from the integrator, which is a sawtooth approximation to the message, is adjusted with the amplifier to match it as closely

as possible. You will be able to see this when you make a model of the system of Figure 1.

step size calculation

In the delta modulator of Figure 1 the output of the integrator is a sawtooth-like approximation to the input message. The teeth of the saw must be able to rise (or fall) fast enough to follow the message. Thus the integrator time constant is an important parameter.

For a given sampling (clock) rate the step *slope* (volt/s) determines the *size* (volts) of the step within the sampling interval.

Suppose the amplitude of the rectangular wave from the sampler is $\pm V$ volt. For a change of input sample to the integrator from (say) negative to positive, the change of integrator output will be, after a clock period T :

$$\text{output} = \frac{2kVT}{RC} \text{ volt} \quad \dots\dots\dots 1$$

where k is the gain of the amplifier preceding the integrator (as in Figure 1).

Answer Tutorial Questions 1 and 2 before attempting the experiment. You can later check your answer by measurement.

slope overload and granularity

The binary waveform illustrated in Figure 2 is the signal transmitted. This is the delta modulated signal.

The integral of the binary waveform is the sawtooth approximation to the message.

In the experiment entitled *Delta demodulation* (in this Volume) you will see that this sawtooth wave is the primary output from the demodulator at the receiver.

Lowpass filtering of the sawtooth (from the demodulator) gives a better approximation to the message. But there will be accompanying noise and distortion, products of the approximation process at the modulator.

The unwanted products of the modulation process, observed at the receiver, are of two kinds. These are due to 'slope overload', and 'granularity'.

slope overload

This occurs when the sawtooth approximation cannot keep up with the rate-of-change of the input signal in the regions of greatest slope.

The step size is reasonable for those sections of the sampled waveform of small slope, but the approximation is poor elsewhere. This is 'slope overload', due to too small a step.

Slope overload is illustrated in Figure 3.

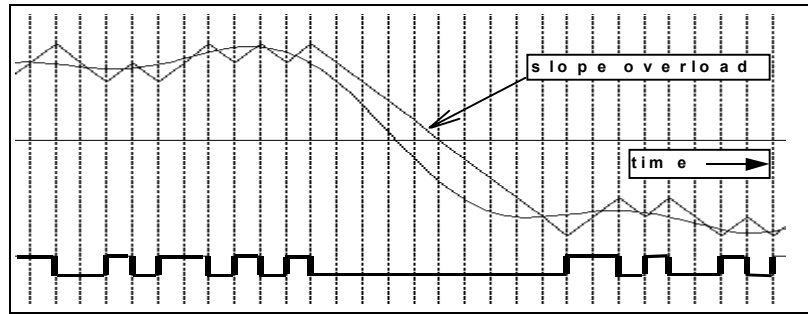


Figure 3: slope overload

To reduce the possibility of slope overload the step size can be increased (for the same sampling rate). This is illustrated in Figure 4. The sawtooth is better able to match the message in the regions of steep slope.

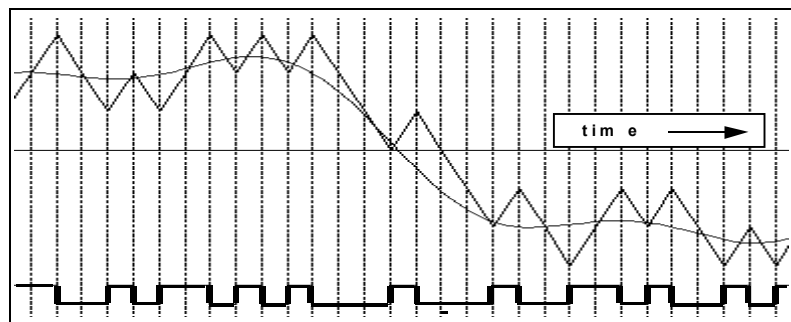


Figure 4: increased step size to reduce slope overload

An alternative method of slope overload reduction is to increase the sampling rate. This is illustrated in Figure 5, where the rate has been increased by a factor of 2.4 times, but the step is the same size as in Figure 3.

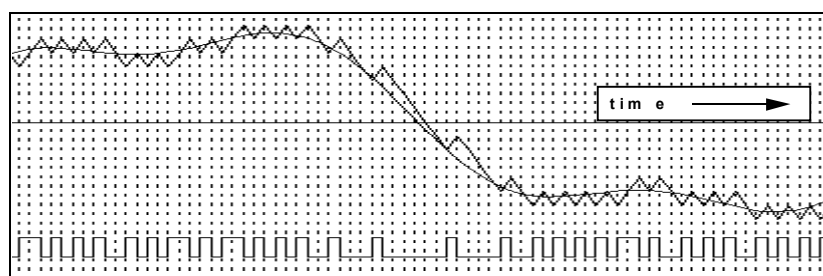


Figure 5: increased sampling rate to reduce slope overload

granular noise

Refer back to Figure 3. The sawtooth follows the message being sampled quite well in the regions of small slope. To reduce the slope overload the step size is increased, and now (Figure 4) the match over the regions of small slope has been degraded.

The degradation shows up, at the demodulator, as increased quantizing noise, or ‘granularity’.

noise and distortion minimization

There is a conflict between the requirements for minimization of slope overload and the granular noise. The one requires an increased step size, the other a reduced step size. You should refer to your text book for more discussion of ways and means of reaching a compromise. You will meet an example in the experiment entitled *Adaptive delta modulation* (in this Volume).

An optimum step can be determined by minimizing the quantizing error at the summer output, or the distortion at the demodulator output.

EXPERIMENT

The block diagram of Figure 1 is modelled with a DELTA MODULATION UTILITIES module, an ADDER, and both of the BUFFER AMPLIFIERS.

You should obtain a DELTA MODULATION UTILITIES module, and read about it in the *TIMS Advanced Modules User Manual*. This module contains three of the elements of the block diagram, namely the LIMITER, SAMPLER, and INTEGRATOR.

The SUMMER block is modelled with an ADDER, both gains being set to unity.

The amplifier preceding the INTEGRATOR in the feedback loop is modelled by a *pair* of BUFFER AMPLIFIERS connected in cascade. These amplifiers both invert, so the combination will be non-inverting - as required.

If the ADDER gains are left fixed at unity, and the message and sampling rates fixed, the only variables to be investigated are the INTEGRATOR time constant, and the gain k of the amplifier (the two BUFFERS in cascade) in the feed back loop.

setting up

*T1 obtain and examine a DELTA MODULATOR UTILITIES module. Read about it in the **TIMS Advanced Modules User Manual**. Before plugging it in set the on-board switches to give an intermediate INTEGRATOR time constant (say SW2A to ON, and SW2B to OFF). Start with no division of the 100 kHz sample clock (front panel toggle switch up to ‘CLK’).*

T2 plug in the ADDER and DELTA MODULATION UTILITIES module.

*T3 use a sinewave to set both of the ADDER gains close to unity. **Do not change these for the duration of the experiment.***

T4 use a sinewave to set both of the BUFFER AMPLIFIER gains to about unity (they are connected in series to make a non-inverting amplifier). Either one or both of these will be varied to make adjustments to the step size during the course of the experiment.

T5 patch up a model of Figure 1. This is shown in Figure 6. Use the 100 kHz TTL signal from the MASTER SIGNALS module as the clock for the SAMPLER, and the 2 kHz MESSAGE for the sinusoidal message to be sampled. The message (2.083 kHz) is a sub-multiple of the 100 kHz sample clock. This helps to obtain text-book like oscilloscope displays.

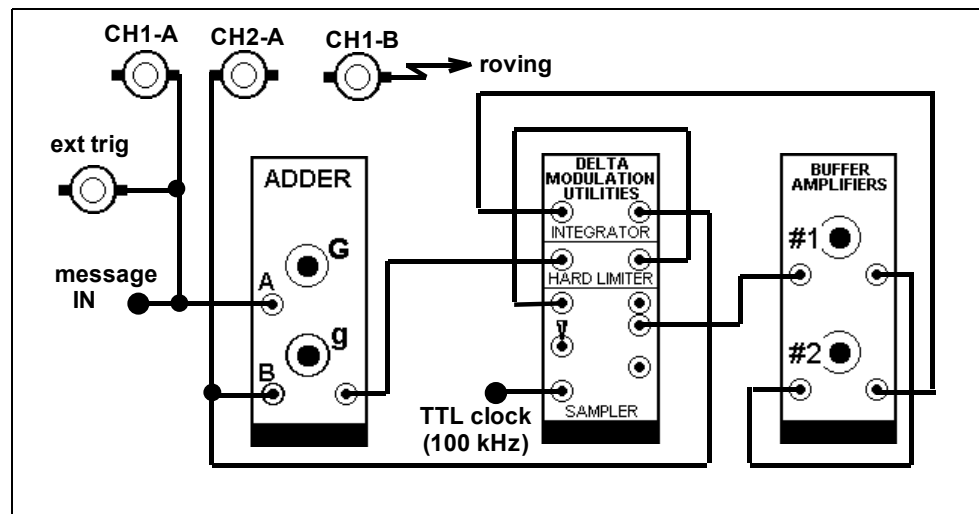


Figure 6: the delta modulator; a model of Figure 1

T6 use the 2 kHz message as the 'ext. trig' signal to the oscilloscope. The signals of immediate interest are the two inputs to the SUMMER, shown connected to CH1-A and CH2-A. Use CH1-B to explore other signals.

You will now set up the modulator for 'acceptable performance'. This means that the INTEGRATOR output should be a reasonable approximation to the message at the input to the SUMMER (of Figure 1).

The only adjustments you should make during the course of the experiment are to:

1. **the step size:** this can be varied in fixed steps with the INTEGRATOR time constant, or fine steps with the gain k of the amplifier (two cascaded BUFFER amplifiers) in the feedback loop (Figure 1).
2. **the sampling clock rate:** with the front panel toggle switch of the DELTA MODULATOR UTILITIES module (100, 50, or 25 kHz).

You should keep a record of the waveforms observed. Sketch them all relative to the sampling clock. Make sure each is consistent with expectations before proceeding to the next Task.

Remember the ADDER is modelling the SUMMER (of Figure 1). The two inputs are the message and its approximation. These two should be of the same general shape and the same amplitude. Since it is their difference which is being sought they will need to be of opposite polarity, as has been arranged (remember, the gains g and G of the ADDER, acting as a SUMMER, have both been set to unity).

Observe the two inputs to the SUMMER. You should use the 'inverse' facility of your oscilloscope (or one channel of another ADDER set to unity gain) and overlay the two displays to simplify their comparison.

warning: remember, when recording other observations, to restore the inverse operation of the oscilloscope to normal.

T7 examine the two inputs to the ADDER on CH1-A and CH2-A. These are the input message, and the INTEGRATOR output respectively. Remember that the INTEGRATOR waveform is required to be an approximation to the message. Adjust the gain k to achieve what you consider the 'best' match. You should have a display similar to that of Figure 2.

You will notice that, despite the fact that the message is a sub-multiple of the clock rate, it is also necessary to fine-tune the oscilloscope sweep speed to obtain a totally stable oscilloscope display. This is through no fault of the oscilloscope - think about it !

T8 find and measure the smallest amplitude step between samples in the INTEGRATOR output waveform over a single clock period. This is the quantizing interval, or step size. Observe that larger steps occur over more than one clock period and that small steps occur when the rate of change of the input is small (near the extrema of the sinewave message). Verify, by calculation, the step size.

Describe in your notes what happens to the approximation when k is decreased, and when k is increased.

***T9** observe the ADDER output and confirm that it is the difference between, rather than the sum of, the two inputs. This is the quantizing noise (quantizing error). Notice that not all peaks are of the same height - there are occasional large peaks. Use the WIDEBAND TRUE RMS METER to measure the quantizing noise (remove any DC with the front panel switch). Adjust the step size with the gain k to minimize the quantizing error. Measure the peak-to-peak amplitude, and rms amplitude. Compare with theoretical expectations. Refer Tutorial Question Q4.*

You will have a chance to measure the distortion of the demodulated signal in the experiment entitled *Delta demodulation* in this Volume. The amount of distortion can be used as another *quantitative* criterion for setting k .

slope overload

The adjustment of the gain k , as a means of controlling slope overload, has so far been made while watching the INTEGRATOR output. This is a *qualitative* judgement of slope overload.

the ADAPTIVE CONTROL signal

In terms of the principle of operation of the delta modulator slope overload gives rise to a succession of samples from the SAMPLER module *of the same sign*. This condition can be detected electronically.

The DELTA MODULATION UTILITIES module has such detection circuitry. When three or more consecutive samples are of the same sign this circuitry signals the fact with a +4 volt output from the ADAPTIVE CONTROL socket of the SAMPLER module. Otherwise the output is at a level of about +2 volt. This signal is used in a later experiment (entitled *Adaptive delta modulation* in this Volume); for now it is instructive to monitor it, for an independent (and more reliable ?) indication of slope overload.

***T10** vary the gain k , and watch the INTEGRATOR output (CH2-A) for signs of slope overload; at the same time monitor the ADAPTIVE CONTROL signal (CH1-B) and compare its pronouncement with your judgement. Since this is a time-sensitive (phase) measurement, make sure your oscilloscope is set up correctly (eg, not on 'alternate-trace' mode). Record how many clock periods elapse, following the onset of slope overload, before this is signalled by the ADAPTIVE CONTROL output signal.*

***T11** re-adjust for 'moderate' slope overload. Increase and decrease the step size by means of the INTEGRATOR time constant (SW2A and SW2B on the DELTA MODULATION UTILITIES module circuit board). Confirm that the degree of slope overload changes as expected.*

T12 the front panel switch of the DELTA MODULATION UTILITIES module inserts dividers between the clock input and the SAMPLER, to vary the clock rate. Select an intermediate clock rate, and re-adjust for 'moderate' slope overload. Show that slope overload increases when the clock speed is halved, or decreases when the clock rate is doubled. Does the step size change when the clock changes ?

the output

So far you have not looked at the output signal from the modulator ! Generally this is the first signal to look at.

The output signal is in TTL format. It is a HI if the INTEGRATOR output is rising, and a LO otherwise. The output signal appears in each of Figures 2,3, 4 and 5.

T13 use CH1-B to look at the modulator output - that is, from the SAMPLER. Compare it with the INTEGRATOR output on CH2-A. Confirm the relationship between the two waveforms.

T14 observe the relationship between the delta modulator output (CH1-B) and the clock signal (use CH2-B).

So far, as promised, there were only two parameters to be varied during the course of the experiment - the loop gain factor k , and the integrator time constant. These were sufficient to allow many observations to be made.

If all of the above has been appreciated it might be a good idea to predict what might happen if the message frequency was changed. Consider the possibilities, then make the change.

T15 set up as for the conditions of Task T7 (whilst observing the two inputs to the SUMMER).

T16 set an AUDIO OSCILLATOR to about 2 kHz, and use it for the message (and ext trig signal), instead of the synchronous 2.083 kHz message. Leaving all other variables fixed, vary the message frequency. Whilst it is not easy to stabilise the display, it is still possible to see some consequences, including the onset of slope-overload. Record and explain your observations.

complex message

A sinewave message is useful for many tests, but a more complex shape can lead to more insights. For meaningful oscilloscope displays it will need to be periodic, and, as before, a sub-multiple of the sampling rate.

Such a message is easy to make with TIMS; a possible method is described in the Appendix to this experiment.

Such a message was used to produce the waveforms of Figures 3, 4, and 5.

T17 make a synchronous, complex message. Vary its shape, and observe results under different conditions.

TUTORIAL QUESTIONS

- Q1** why is it useful to set up the experiment using the 2 kHz signal from the MASTER SIGNALS module, as opposed to a signal from an AUDIO OSCILLATOR, for example ?*
- Q2** what are the system parameters which control the step size (quantization amplitude) for a given sampling rate ?*
- Q3** knowledge of the step size alone is insufficient to make a statement about the possibility of slope overload. What else needs to be known ?*
- Q4** calculate the peak-to-rms ratio of a constant peak-to-peak amplitude sawtooth waveform.*
- Q5** show that delta modulation is a special case of differential pulse code modulation (DPCM). What is the number of bits per word ?*

APPENDIX

a 'complex' message.

We can define a 'complex' message as one which is periodic, and having a shape exhibiting more slope changes than a pure sinewave. As an example, see Figure A.1.

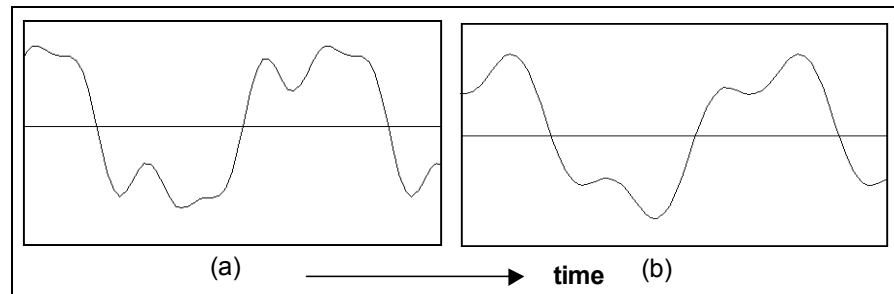


Figure A1: two 'complex' messages

Such a message can be made by filtering a square wave.

The square wave can be obtained by passing a sinewave through a comparator. The TIMS COMPARATOR has an analog output. Its limiting characteristic can be set to 'hard'¹. See the *TIMS User Manual*. The amplitude limited output contains odd harmonics, and the first two or three can be filtered off (together with the fundamental) to make the new shape.

By including a PHASE SHIFTER (this introduces a phase shift which varies with frequency), the shape can be further modified; but this is not essential.

For synchronous displays, in the present experiment, it is useful to use the 2.083 kHz MESSAGE from MASTER SIGNALS.

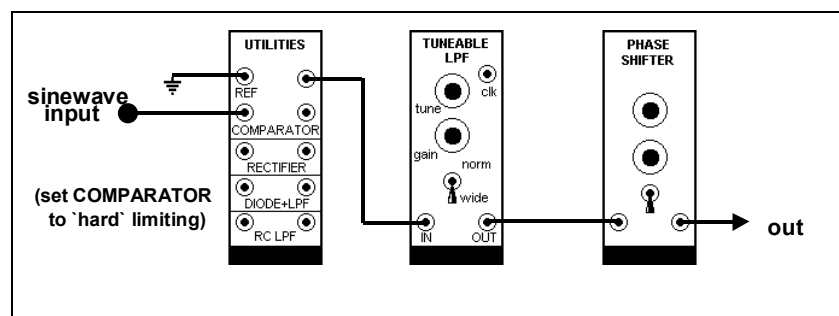


Figure A2: a 'complex' message generator

The waveforms of Figure A1 were made by selecting the first three odd harmonics (a), and the first two odd harmonics (b) respectively. Many shape variations are possible, including these, as the phase is varied.

¹ SW1 toggles DOWN; SW2 toggles UP

An interesting feature is that, by obtaining the complex waveform shape with the TUNEABLE LPF in the WIDE mode, instant reversion to a sine wave is effected by toggling to the NORM mode.

DELTA DEMODULATION

PREPARATION.....	136
delta demodulation methods	136
EXPERIMENT	138
test signal.....	138
the demodulator.....	138
distortion - a qualitative look	138
speech.....	139
distortion - SNDR measurement	139
TUTORIAL QUESTIONS	140

DELTA DEMODULATION

ACHIEVEMENTS: introduction to the demodulation of a delta modulated signal; measurement of quantization distortion at the receiver; listening test on speech.

PREREQUISITES: completion of the experiment entitled *Delta modulation* in this Volume.

ADVANCED MODULES: DELTA MODULATION UTILITIES; DELTA DEMOD UTILITIES; WIDEBAND TRUE RMS METER

PREPARATION

delta demodulation methods

You should refer to your text book and course work for background information regarding delta demodulation methods, and the likely sources of distortion.

For this experiment you will supply your own delta modulated signal, using the modulator examined in the experiment entitled *Delta modulation*.

The TMS DELTA DEMOD UTILITIES module will be used for demodulation (the receiver). It contains a SAMPLER and an INTEGRATOR. The SAMPLER uses a clock stolen from the modulator (the transmitter). The SAMPLER accepts TTL signals as input, but gives an analog output for further analog processing - for example, lowpass filtering.

The principle of the demodulator is shown in block diagram form in Figure 1 below. It performs the reverse of the process implemented at the modulator in the vicinity of the sampler and integrator.

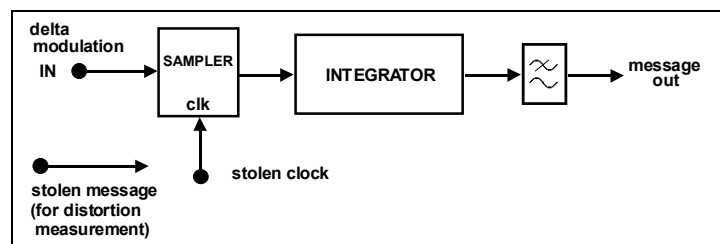


Figure 1: a demodulator for delta modulation

The sampler, which is clocked at the same rate as the one at the modulator, outputs a bi-polar signal ($\pm V$ volts). The integrator generates a sawtooth-like waveform from this. This is an approximation to the original message. Having the same time constant as that at the modulator, and with no noise or other signal impairments, it will be identical with the corresponding signal at the modulator.

However, it is not the message, but an approximation to it.

The sawtooth waveform contains information at the message frequency, plus obvious unwanted frequency components (quantizing noise).

The unwanted components which are beyond the bandwidth of the original baseband message are removed by a lowpass filter. Those unwanted components which remain are perceived as noise and distortion.

Unlike ideal sampling of an analog signal, and ideal reconstruction with a lowpass filter (refer to the experiment entitled *The sampling theorem* within *Volume A1 - Fundamental Analog Experiments*), the reconstruction of the message from a delta modulator is *not* perfect.

You will find that the SNDR¹ is relatively poor, and certainly a lot worse than the signal-to-noise ratio capabilities of the TMS system (typically better than 40 dB). Thus the SNDR that you will be measuring will be entirely due to the imperfections of the delta modulator itself.

However, do not then declare that delta modulation has no practical applications.

You will find, in the experiment entitled *Adaptive delta modulation*, in this Volume, that there are means of implementing improvements.

With further refinement in the circuitry, a higher clock speed, and sophisticated adaptive algorithms², delta modulation can perform remarkably well. It is used extensively in the field of digital audio.

EXPERIMENT

test signal

*T1 set up a delta modulator of the type examined in the experiment entitled **Delta modulation**. Set it up initially for what you consider to be the ‘best’ approximation to the message (compare the two inputs to the SUMMER).*

¹ signal-plus-noise-and-distortion ratio

² see the experiment entitled *Adaptive delta modulation* in this Volume

the demodulator

For this demodulator you will use the DELTA DEMOD UTILITIES module. This contains a LIMITER, a clocked SAMPLER, and an INTEGRATOR of the type in the DELTA MODULATION UTILITIES module.

T2 obtain and examine a DELTA DEMOD UTILITIES module. Read about it in the TIMS Advanced Modules User Manual.

T3 model the demodulator of Figure 1. Set the time constant of the INTEGRATOR to the same value as selected in the modulator. Use the RC LPF in the DELTA DEMOD UTILITIES for the output filter.

Note the SAMPLER accepts a TTL signal from the modulator, as well as a stolen clock. For oscilloscope triggering use the message signal, also stolen from the modulator. Set the front panel clock switch to match that at the modulator.

T4 confirm that the signals at each of the INTEGRATOR outputs are similar.

T5 confirm that the output of the demodulator lowpass filter is a reasonable copy of the original message.

distortion - a qualitative look

At the modulator you can change the sampling rate (100 kHz, 50 kHz, and 25 kHz with the front panel switch), and the step size (RC time constants). You can also control the amount of slope overload. All of these have their influence on the measured SNDR.

T6 introduce various mal-adjustments at the modulator (observed at the output of the modulator INTEGRATOR), and observe their effect at the demodulator output. Use both a sinusoidal message, and a 'complex' message³.

speech

If you have bandlimited speech available at TRUNKS, or from a SPEECH module, you can make many interesting listening tests. How would you describe speech when distorted by slope overload?

T7 make qualitative assessments of the effect of the various mal-adjustments, at the modulator, on the demodulated speech.

³ as defined in the experiment entitled *Delta modulation* in this Volume.

distortion - SNDR measurement

For quantitative signal-to-noise-and-distortion ratio measurements (SNDR) you can model the scheme illustrated in Figure 2.

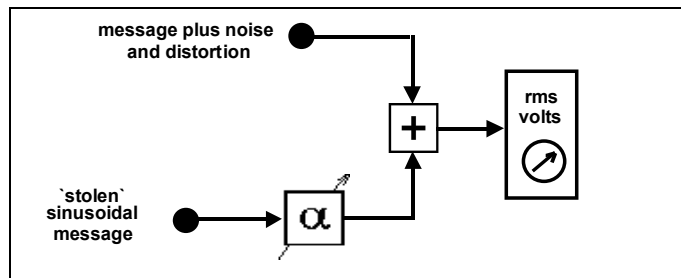


Figure 2: noise and distortion measurement

Recall the experiment entitled *Modelling an equation* (within *Volume A1 - Fundamental Analog Experiments*), where the technique of signal cancellation in an adder was first introduced.

You can use the WIDEBAND TRUE RMS METER to measure the distortion components.

The principle is to cancel the wanted sinusoidal message from the adder output, leaving only the unwanted components (noise-plus-distortion). Having obtained a minimization of the message from the adder output, then removal of the message-plus-noise from the adder leaves the (stolen) message, which will give the reference with which to compare the noise-plus-distortion.

A model of the measurement system is illustrated in Figure 3. Remember to set the on-board switch of the PHASE SHIFTER to LO.

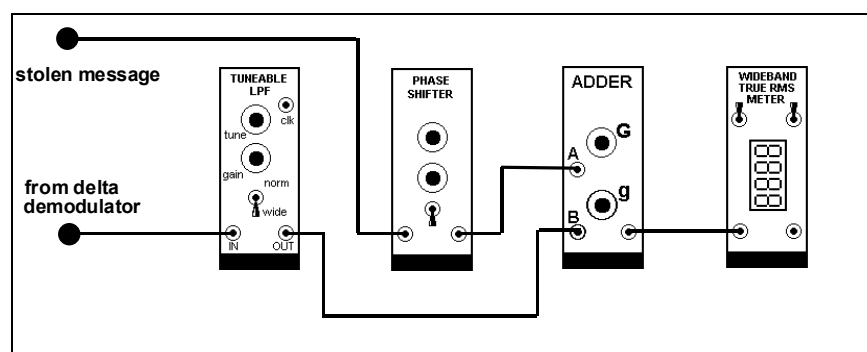


Figure 3: SNDR measurement

T8 as before (when making qualitative observations), introduce various mal-adjustments at the modulator, and observe their effect at the demodulator output. Use a sinusoidal message (refer to Tutorial Question Q4).

TUTORIAL QUESTIONS

- Q1** the term 'granular noise' is often used in the context of delta modulation. Explain where this term comes from. Describe the compromise which has to be made when determining a step size in a delta modulator.
- Q2** describe the procedure used when measuring SNDR with the scheme of Figure 2.
- Q3** what was the effect upon output noise and distortion of an increase of:
- a) step size
 - b) sampling rate
 - c) slope overload ?
- Q4** the noise-and-distortion measurement scheme of Figure 2 was used when the message was a single sine wave. Would it be effective for measurement with a more complex message ? Explain.
- Q5** you were advised to set the time constant of the INTEGRATOR in the demodulator to be the same as that in the modulator. Was this essential ? Describe the consequences of using a different time constant at the demodulator.
- Q6** could the message be recovered from the delta modulated signal using only a lowpass filter ? Explain.

ADAPTIVE DELTA MODULATION

PREPARATION	142
background	142
TIMS adaptive delta modulator	142
the voltage controlled amplifier - VCA	143
EXPERIMENT	144
the adaptive control voltage	144
VCA calibration	144
manual control	145
stability	145
adaptive control	145
demodulation	146
TUTORIAL QUESTIONS	147
APPENDIX	148
loop stability	148

ADAPTIVE DELTA MODULATION

ACHIEVEMENTS: introduction to a variation of the basic delta modulator, which adjusts the step size according to the slope of the signal being sampled

PREREQUISITES: completion of the experiments entitled *Delta modulation* and *Delta demodulation* in this Volume.

ADVANCED MODULES: DELTA MODULATION UTILITIES; DELTA DEMOD UTILITIES; WIDEBAND TRUE RMS METER optional.

PREPARATION

background

It is assumed that you have been introduced to the principles of adaptive delta modulation in your course work.

TIMS adaptive delta modulator

The basic delta modulator was studied in the experiment entitled *Delta modulation*. It is implemented by the arrangement shown in block diagram form in Figure 1.

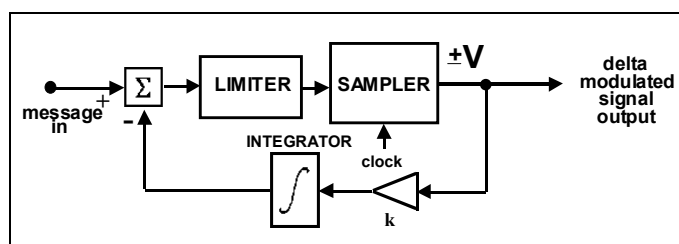


Figure 1: basic delta modulator

You will remember that with this modulator there was a conflict when determining the step size.

A large step size was required when sampling those parts of the input waveform of steep slope. But a large step size worsened the granularity of the sampled signal when the waveform being sampled was changing slowly. A small step size is preferred in regions where the message has a small slope.

This suggests the need for a controllable step size - the control being sensitive to the slope of the sampled signal. This can be implemented by an arrangement such as is illustrated in Figure 2.

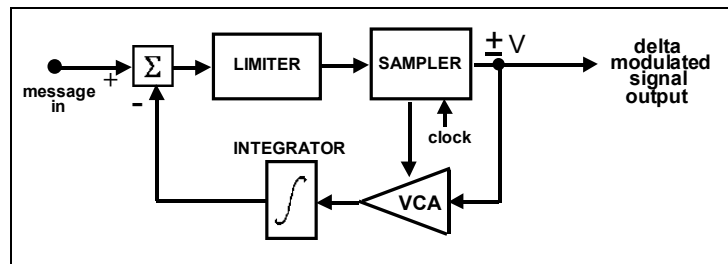


Figure 2: an adaptive delta modulator

The gain of the amplifier is adjusted in response to a control voltage from the SAMPLER, which signals the onset of slope overload.

The step size is proportional to the amplifier gain. This was observed in an earlier experiment.

Slope overload is indicated by a succession of output pulses of the same sign.

The TIMS SAMPLER monitors the delta modulated signal, and signals when there is no change of polarity over 3 or more successive samples.

The actual ADAPTIVE CONTROL signal is +2 volt under 'normal' conditions, and rises to +4 volt when slope overload is detected.

The gain of the amplifier, and hence the step size, is made proportional to this control voltage. Provided the slope overload was only moderate the approximation will 'catch up' with the wave being sampled. The gain will then return to normal until the sampler again falls behind.

Much work has been done by researchers in this area, and sophisticated algorithms have been developed which offer significant improvements over the simple system to be examined in this experiment.

the voltage controlled amplifier - VCA

The VCA can be modelled with a MULTIPLIER. This is shown in Figure 3.

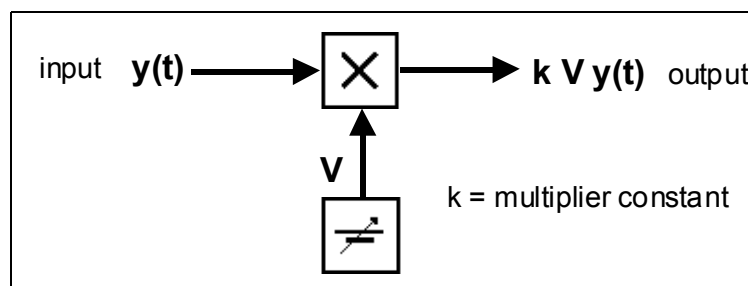


Figure 3: the voltage controlled amplifier

The control in Figure 3 is shown as a DC voltage. This may be set to any value in the range $\pm V_{\max}$. Beyond $V_{\max}$, the MULTIPLIER will overload. However, the control voltage need not be DC, but can be time varying. Under these conditions the arrangement is more likely to be called a modulator.

You have met the MULTIPLIER constant, 'k', in earlier experiments of Part I, where it was defined and measured.

EXPERIMENT

The block diagram of Figure 1 was modelled in the experiment entitled *Delta modulation*. Refer to that experiment for details.

The adaptive delta modulator of Figure 2 differs only by the addition of a voltage controlled amplifier (VCA), modelled, as described above, with a MULTIPLIER.

the adaptive control voltage

The DELTA MODULATION UTILITIES module has a socket labelled ADAPTIVE OUTPUT. The signal from this socket is at a level of either +2 or +4 volts. The lower output is what might be called the 'normal' level. If at any time the delta modulated signal contains three or more consecutive samples of the same size then this signal goes to the higher (+4) volt level ¹. Three or more consecutive samples of the same level indicates slope overload.

When including the VCA in the feedback path you must ensure that at no time will either of the inputs to the MULTIPLIER exceed its safe (ie, linear) operating range (say ± 5 volts absolute maximum).

VCA calibration

Before setting up the delta modulator, it is wise to familiarise yourself with the operation of the VCA.

T1 set up a VCA according to the block diagram of Figure 3. Use the VARIABLE DC module as a control signal, and a sinewave as input. Connect each via a BUFFER amplifier so that the values of $V_{max/x}$ and $V_{max/y}$ can be determined. These are the overload levels for each of the inputs. They are likely to be similar. Select DC coupling with the front panel switch of the MULTIPLIER.

T2 measure the VCA gain for a control voltage of +2 volt. This is the 'normal' output from the ADAPTIVE CONTROL of the DELTA MODULATOR UTILITIES module.

Your measurements should have shown that the MULTIPLIER can accept inputs considerably in excess of the TMS ANALOG REFERENCE LEVEL before overload sets in.

¹ more details in the *TIMS Advanced Modules User Manual*.

Likewise, the INTEGRATOR input can, under some conditions, be subject to quite large input signals; but it is robust and can also handle input amplitudes well in excess of the TIMS ANALOG REFERENCE LEVEL.

You will notice that, except for the presence of the MULTIPLIER in the feedback loop, the modulator is the same as that studied in the experiment entitled *Delta modulation*. You should use the same setting up procedure as in that experiment, with the adaptive control inhibited. This is done by connecting +2 volt in place of the ADAPTIVE CONTROL voltage to the MULTIPLIER.

manual control

*T3 model the block diagram of Figure 1. This is not the adaptive modulator. Refer to the experiment entitled **Delta modulation** for details. The amplifier in the feedback loop is modelled with two BUFFER amplifiers in cascade.*

T4 observe the two inputs to the SUMMER. Adjust the feedback gain so that the sawtooth shows some evidence of (ie, moderate) slope overload.

T5 observe the control voltage from the ADAPTIVE CONTROL output socket. It will be alternating between V_1 (no slope overload) and V_2 volt (following the onset of, and coincident with, the slope overload). Record the value of V_1 (about 2 volt).

T6 insert the VCA between the SAMPLER and the BUFFER AMPLIFIER. Set the control voltage to the VCA to V_1 volts, obtained from the VARIABLE DC supply.

T7 observe the two inputs to the SUMMER. These should be exactly the same as observed during Task T4. The slope overload should, therefore, be apparent as before.

stability

There are now three amplifiers in the feedback loop. At the best of times this could be a cause for concern - the stability of the whole system could be compromised. Refer to the Appendix to this experiment for further comment.

adaptive control

The VCA is now set up in the feedback loop, but is currently in a passive mode.

You are now ready to implement adaptive control of the loop gain by replacing the fixed control voltage V_1 with the adaptive control voltage from the modulator.

What you will want to observe is the reduction of the length of the period of the slope overload.

T8 while watching the length of the slope overload portion of the sawtooth waveform from the INTEGRATOR, replace the DC voltage from the VARIABLE DC supply to the VCA with the ADAPTIVE CONTROL voltage from the modulator.

T9 replace the DC control voltage with the ADAPTIVE CONTROL from the SAMPLER. Notice that the slope overload remains as for the conditions of the previous Task when the control voltage was +4 volt, but that the granularity at the extrema of the message has **not** been worsened.

To change between adaptive and non-adaptive operation move the patch cord from the ADAPTIVE CONTROL output socket of the SAMPLER to the preset (V_1) output of the VARIABLE DC module.

T10 spend some time examining the waveforms at the various interfaces. As necessary, replace the ADAPTIVE CONTROL voltage with the manual (DC voltage) control. Don't forget to monitor the ADAPTIVE CONTROL voltage itself. In other words, make sure you make enough observations to appreciate what is happening.

T11 use a 'complex message', as described in the experiment entitled **Delta modulation**, and compare results (by visual inspection of the INTEGRATOR output waveform) with and without the adaptive feedback operating.

You should now be reasonably confident, from your observations at the modulator (transmitter), that the adaptive feedback control will improve the performance of the system as observed at the demodulator (receiver).

Thus it might be agreed that the object of the experiment has been achieved.

For positive verification, however, it is necessary to build a demodulator and make some further observations.

demodulation

It is essential that you have already completed the experiment entitled *Delta demodulation*. This introduced methods of noise and distortion measurement, which are required now.

You should now model a delta demodulator, as described in the experiment entitled *Delta demodulation..*

Whilst absolute measurement of signal to noise-plus-distortion ratio (SNDR) measurements are of interest, of greater interest in the present situation is to observe the change to the demodulated waveform which happens when the adaptive feedback is introduced. This is a qualitative measurement but nonetheless very instructive.

The setting up procedure at the demodulator will be somewhat similar to that used at the modulator.

Of interest will be a measurement to resolve the question: *is it necessary to make the demodulator adaptive in the same manner as at the modulator ? Is there a penalty for not doing so ?*

T12 set up a demodulator. Use a complex message. Observe recovered waveforms under various conditions.

TUTORIAL QUESTIONS

Q1 make a positive statement about how your observations at the modulator confirmed that the ADAPTIVE CONTROL 'improved' the performance of the modulator.

APPENDIX

loop stability

You are working with a feedback loop. At the best of times these can run into instability if the loop gain is too high. Some of this instability can be caused by unplanned for phase changes round the loop.

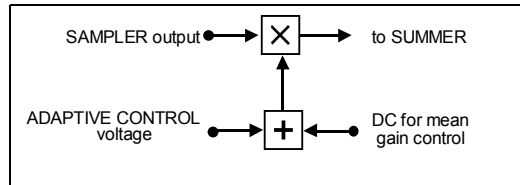


Figure 4: gain modification using VCA

The presence of two BUFFER amplifiers in cascade does not help the situation. These were placed there in the non-adaptive modulator as a convenient method of changing the loop gain.

Now there is an extra source of phase change introduced by the VCA, and also a new source of gain adjustment. If it turns out that the gain provided by the two BUFFER amplifiers is near unity it might be prudent to remove them.

Small gain adjustment could be introduced by the scheme illustrated in Figure 4. This scheme has not been included in any of the Tasks. If you elect to use it, then modify the instructions accordingly.

DELTA-SIGMA MODULATION

PREPARATION.....	150
EXPERIMENT	152
TUTORIAL QUESTIONS	153
APPENDIX A.....	154

DELTA-SIGMA MODULATION

ACHIEVEMENTS: introduction to an important variation of the basic delta modulator (as used in compact disc players).

PREREQUISITES: completion of the experiments entitled *Delta modulation* and *Delta demodulation* in this Volume.

ADVANCED MODULES: DELTA MODULATION UTILITIES, DELTA DEMOD UTILITIES

PREPARATION

It is assumed that you have been introduced to the principles of delta-sigma modulation in your course work, and have completed the experiment entitled *Delta modulation*.

Delta-sigma modulation¹ is an apparently simple variation of the basic delta modulation arrangement. Whilst it is easy to describe the variation (by way of the block diagram, for example), the implications of the change are not necessarily transparently obvious. You should refer to your course work, which presumably will have treated the theory at an appropriate level. Suffice to say that the delta-sigma modulator and demodulator combination finds application in the compact disk digital record player, where its properties are exploited to the full.

The nature of the variation can be seen by first reminding yourself of the configuration of the basic delta modulator, shown in block diagram form in Figure 1.

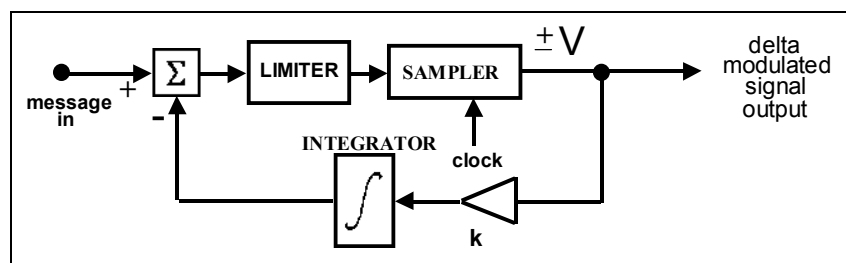


Figure 1: basic delta modulator

¹ also called sigma-delta modulation

The delta-sigma modulator places an integrator between the message source and the summer of the basic delta modulator.

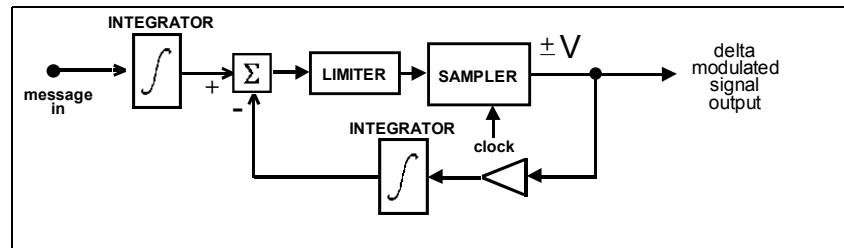


Figure 2: the delta-sigma modulator

The two integrators at each *input* to the linear summer can be replaced by a single integrator at the summer *output*. This simplified arrangement is shown in Figure 3.

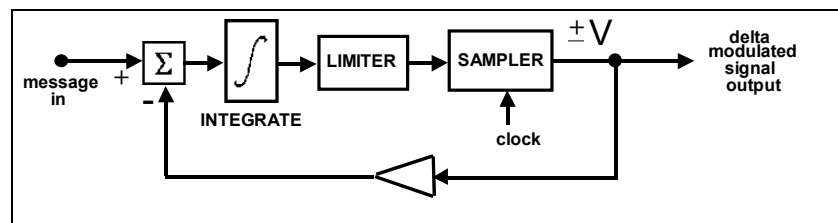


Figure 3: the delta-sigma modulator simplified

The integrator introduced at the input to the summer obviates the need for an integrator in the demodulator. Thus the demodulator can be a simple lowpass filter.

EXPERIMENT

A model of the delta-sigma modulator block diagram of Figure 3 is shown in Figure 4.

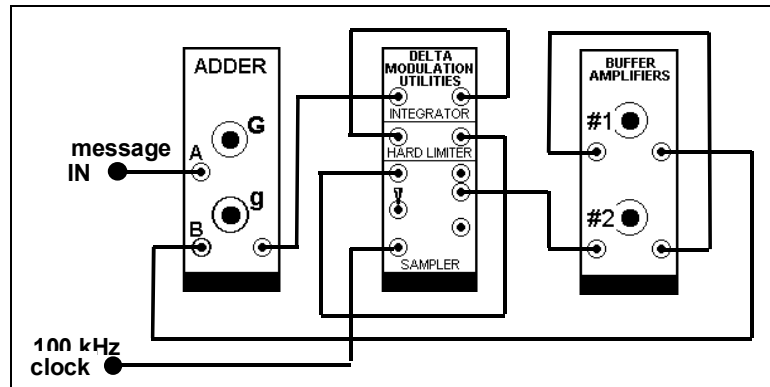


Figure 4: the delta-sigma modulator model

- T1** before plugging in the DELTA MODULATOR UTILITIES module decide upon the integrator time constant, then set it with switches SW2A and SW2B. See Appendix A of this experiment.*
- T2** adjust both ADDER gains to unity, and both BUFFER AMPLIFIER gains to unity. Throughout the experiment the gain g of the ADDER (acting as the SUMMER) will not be changed.*
- T3** patch together the complete delta-sigma modulator according to Figure 4.*

The familiar sawtooth waveform may be observed at the INTEGRATOR output.

You can now examine the behaviour of the modulator under various conditions, and with different messages, as was done for the basic delta modulator in an earlier experiment.

An important message to examine is one with a DC component.

- T4** use a lowpass filter as a demodulator.*

Examine the demodulator performance as was done in the previous delta modulation experiments.

TUTORIAL QUESTIONS

Q1 describe how the delta-sigma modulator-demodulator arrangement is used to advantage in a compact disk (CD) player. This has not been explained in the introduction to the experiment, so you will need to refer to your course work or other sources.

APPENDIX A

The integrator time constant in the DELTA MODULATION UTILITIES module is controlled by the on-board switch SW.

Full details of this integrator may be found in the *Advanced Modules User Guide*. In summary it is composed of an R and C network.

The component subscripts refer to their circuit board designations. Thus the single, fixed capacitor is C2.

The resistor R of the network is made up of R11, R12, and R13.

Resistor R11 is permanently in place, but R12 and R13 can be added in parallel with the switches SW2-A and SW2-B respectively (when ON).

Component values are:

C2	47 nF
R11	5k6 ohms
R12	5k6 ohms
R13	1k5 ohms