

ELEC 2210 EXPERIMENT 12

NMOS Logic

Objectives:

The experiments in this laboratory exercise will provide an introduction to NMOS logic. You will use the Bit Bucket breadboarding system to build and test several DC transistor circuits. The objectives of this experiment include the following:

- Reinforce basic principles of NMOS from ELEC 2210
- Gain an understanding of NMOS logic circuits
- Gain more experience with the oscilloscope
- Continue to develop professional lab skills and written communication skills.

Introduction:

We will examine NMOS logic circuits, which contain only n-channel transistors. The NMOS inverter is the basic gate of the NMOS family. There are four different possible load configurations, namely resistor load, saturated load, linear load, and depletion mode. However, in this experiment we will examine only resistor load and (optionally) saturated load circuits. We will analyze the dc voltage transfer characteristics of several inverter designs. We will also define and develop the noise margin of NMOS digital circuits in terms of the inverter voltage transfer curve. We will then study NMOS NOR logic gates.

Theory:

An inverter circuit outputs a voltage representing the opposite logic-level to its input. Inverters can be constructed using a single NMOS transistor or a single PMOS transistor coupled with a resistor.

Digital inverter quality is often measured using the Voltage Transfer Curve, which is a plot of input vs. output voltage. From such a graph, device parameters including noise tolerance, gain, and operating logic-levels can be obtained. □

Ideally, the voltage transfer curve (VTC) appears as an inverted step-function - this would indicate precise switching between *on* and *off* - but in real devices, a transition region exists. The VTC indicates that for low input voltage, the circuit outputs high voltage; for high input, the output tapers off towards 0 volts.

The slope of this transition region is a measure of quality - steep (close to -Infinity) slopes yield precise switching. The output voltage, V_{OH} , can be a measure of signal driving strength when cascading many devices together.

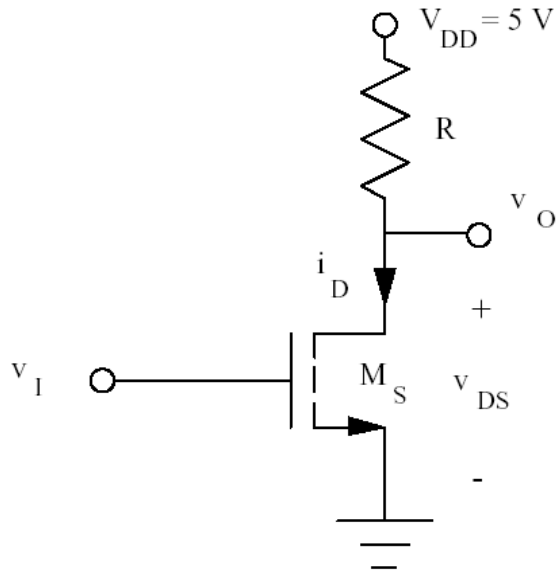


Figure 1. NMOS inverter with resistive load.

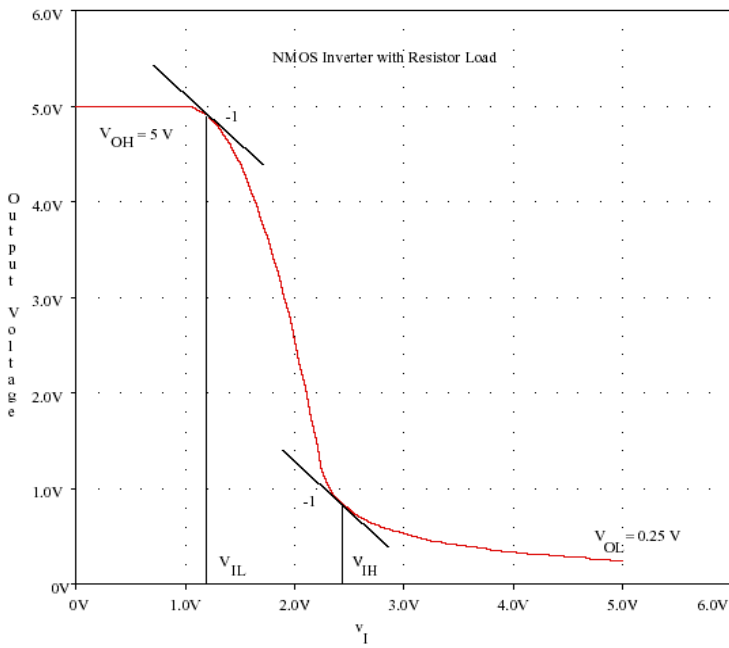


Figure 2. VTC for resistor-loaded NMOS inverter.

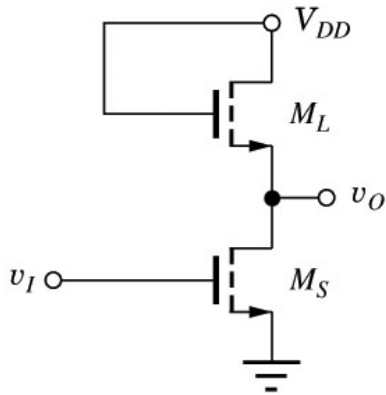


Figure 3. Saturated load inverter.

Graph2:

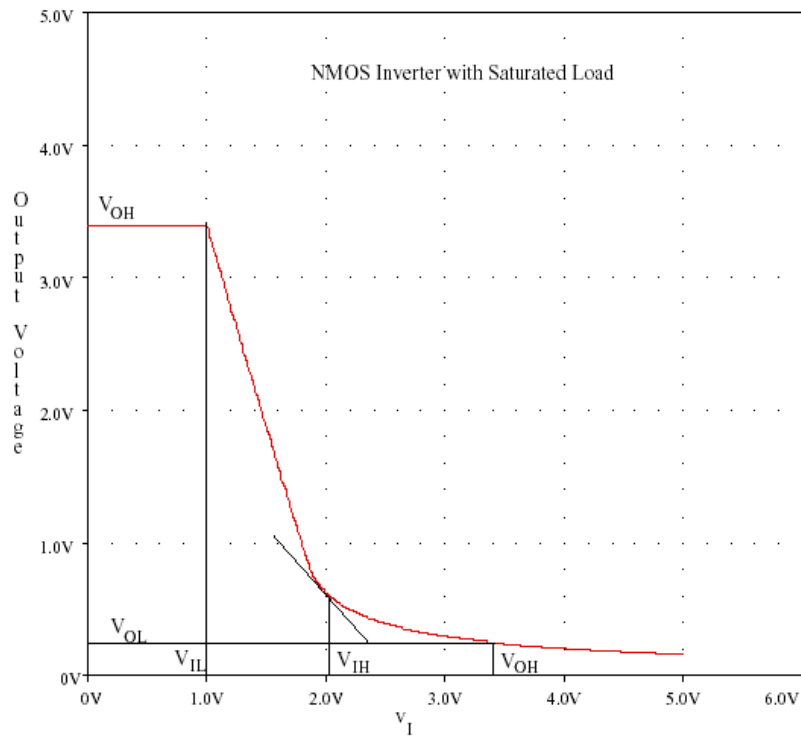


Figure 4. VTC for saturated load inverter.

Pre-Lab

- (1) Obtain the data sheet for the ZVN4306 MOSFET.
- (2) What is the gate-source voltage in Fig. 1 (below)?
- (3) What is the approximate value of the drain current in Fig. 1 (below) with the voltages as shown, assuming V_{DS} is very small?
- (4) What is the average power dissipation in the logic gate shown in Figure 1 if the gate of M1 is connected directly to a 0 to 5V square wave instead of the voltage divider?

Lab Experiment

Components used:	Qty:
ZVN4306 MOSFET	2
1K ohm resistor	4
330 ohm resistor	1

Part 1. VTC of the resistor-loaded NMOS Inverter

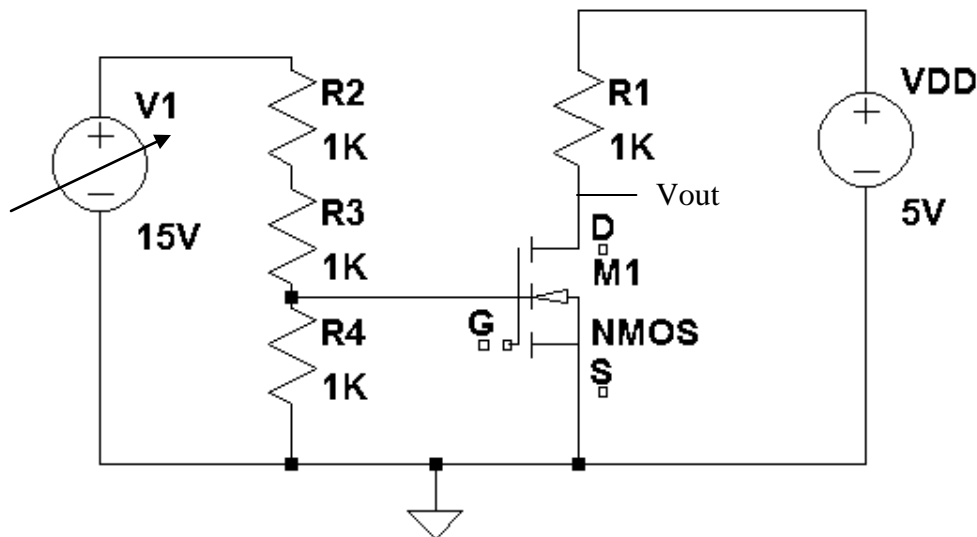


Figure 5: Resistor-loaded NMOS inverter for Step 1.

VTC by Procedure (a):

1. Connect the NMOS inverter as shown in Fig. 1
2. Use a constant 5 V dc power supply for VDD.
3. Use a variable 15 V dc power supply for V1
4. Connect the DMM across D and S of M1 to determine the voltage at the output (Vout).
5. Use the DVM on the bitbucket to measure the voltage at the input (VIN) across G and S.
6. Measure the voltage transfer characteristic (VOUT vs. VIN) of this logic inverter. Vary V1 from 0 V to 15. Record VOUT vs. VIN for a number of data points over the full range of V1.

Start at the minimum value and work your way up, slowly increasing V_1 . Be careful when you record the values between 2V and 3V as there will be a sharp decrease in V_{OUT} . So do a finer tuning in this region and record a number of data points here which will help you when you draw the graph. Plot the voltage transfer characteristic from the data (V_{OUT} vs V_{IN}).

Determine V_H , V_L and the noise margins from your data.

VTC by Procedure (b)

Apply a 0-5V triangle wave to the gate of M1. Using the oscilloscope in the X-Y mode, display the VTC. Read the display to determine V_H , V_L and the noise margins.

Compare your results from procedures (a) and (b).

Part 2. Power dissipation in the NMOS logic inverter.

Disconnect the voltage divider from the MOSFET and use a slide switch to apply 0V or 5V to the gate of M1. Compute the power dissipation in each logic state. What is the average power dissipation in the MOSFET? What is the average power dissipation in the resistor?

Part 3. Truth table of the NMOS NOR.

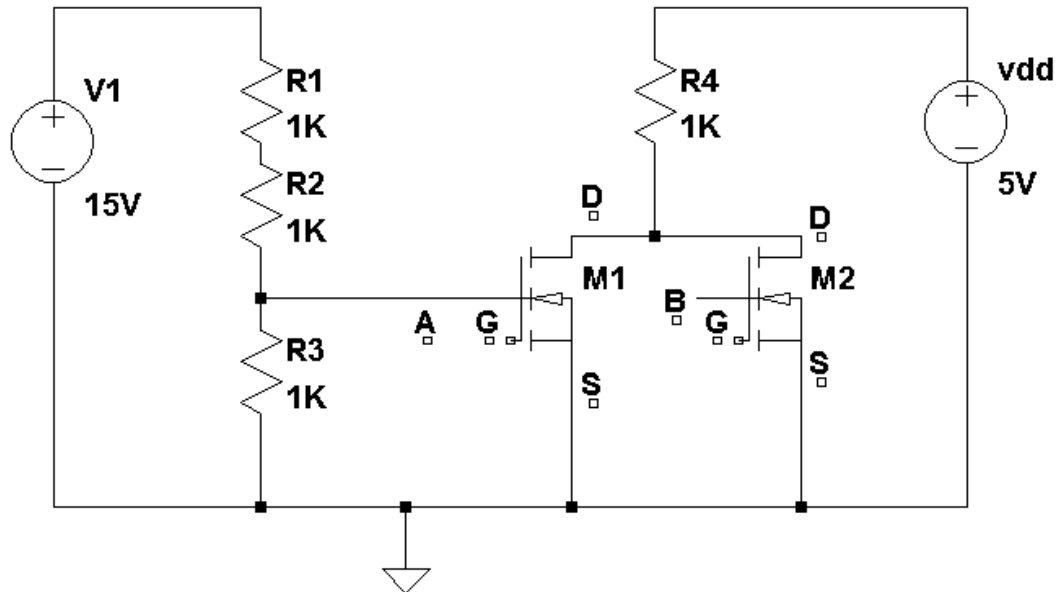


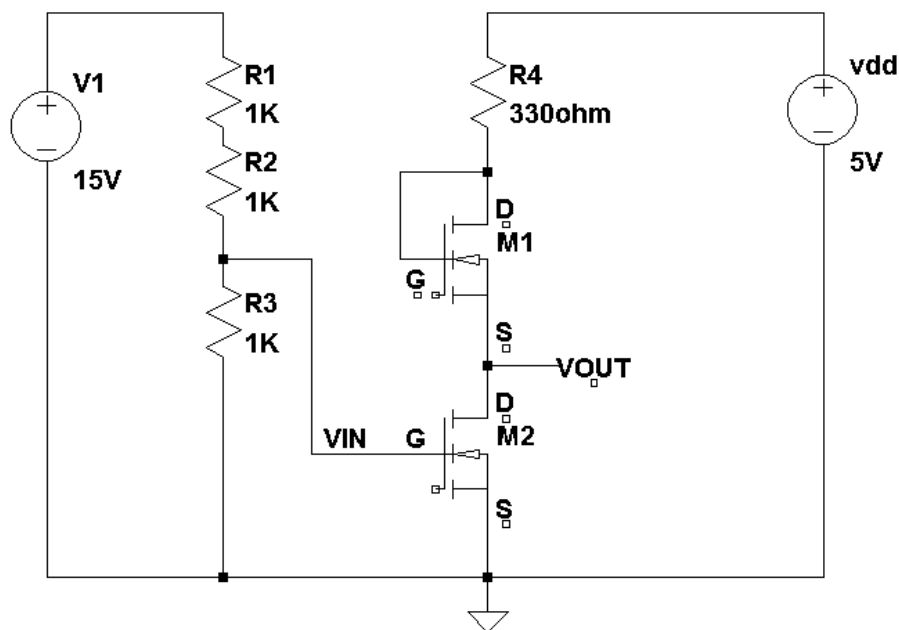
Figure 6: Resistor-loaded NMOS NOR for Step 3.

Procedure:

1. Connect the circuit shown in Fig. 6. The gate terminals of M1 and M2 function as the inputs of this NMOS NOR logic gate. These two inputs are named A and B for convenience. The output is at the common drain connection.

2. Use a constant 5V dc power supply for VDD.
3. Reconnect the voltage divider from Step 1.
4. Connect input B to the bit data switch SW7. Put SW7 to 0 initially.
5. Connect the DVM on the bitbucket to input A of M1.
6. Connect the digital multimeter across the D and S of M2 to measure the output voltage Y.
7. Sweep V1 from 0 V to 15 V and record the VTC of this gate. What are the values of V_L and V_H ?
8. Record the truth table for this gate by recording the output voltage at Y for every logic combination of A and B, and then assigning a logical value (HIGH or LOW) to Y.

Part 4 (Optional). NMOS SATURATED LOAD INVERTER: Voltage Transfer Characteristic and Noise Margins



Procedure:

1. Connect the NMOS inverter as shown above.

Repeat the VTC and Noise Margin measurements you made in Part 1.