LPC2292 Universal Asynchronous Receiver Transmitter (UART)

- Two UARTs on LPC2292
  - UART0: TxD0, RxD0, UART1: TxD1,RxD1

    Pins: P0.0 P0.1 P0.8 P0.9
- Asynchronous serial communications protocol
  - Conforms to “550 industry standard specification”
- Built-in, programmable baud rate generator
- 16-byte transmit/receive FIFO
- 5-to-8 bit data formats
- Programmable parity checking/transmission
- Interrupt-driven operation available

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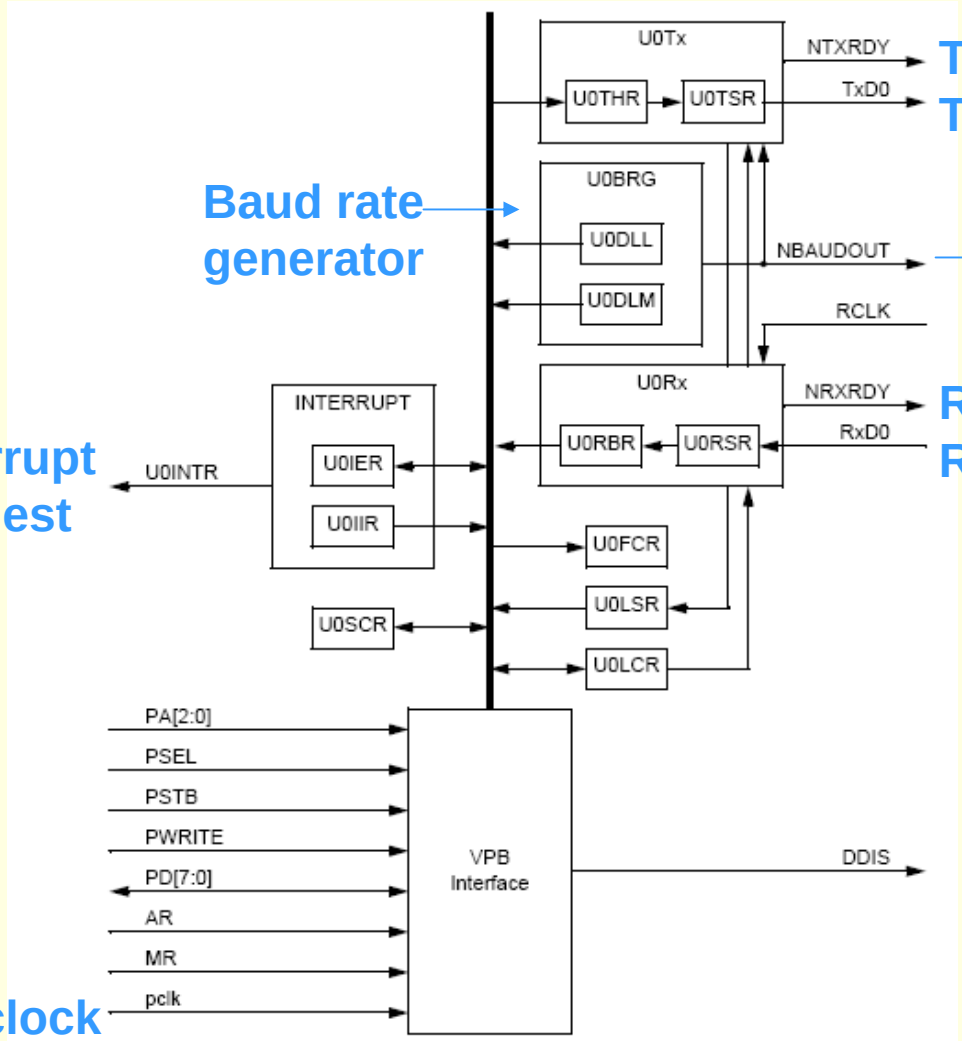
UART0 block diagram



Transmitter ready
Transmitted data

Baud rate generator

16x baud rate = pclk/DLM:DLL

Receiver ready
Received data

Interrupt request

VPB clock

RxD,TxD pins

- Select RxD, TxD pin functions in pin connect block register PINSEL0 (0xE002C000)

  (Configures pins P0.0 – P0.15)

  - PINSEL0(1:0): 00 for GPIO P0.0, 01 for TxD0
  - PINSEL0(3:2): 00 for GPIO P0.1, 01 for RxD0
  - PINSEL0(17:16): 00 for GPIO P0.8, 01 for TxD1
  - PINSEL0(19:18): 00 for GPIO P0.9, 01 for RxD1

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UART0 Register Map

All 8 bits – “unsigned char” in lpc22xx.h

Name	Description	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	Access	Reset Value*	Address
U0RBR	Receiver Buffer Register	MSB			READ DATA				LSB	RO	un-defined	0xE000C000 DLAB = 0
U0THR	Transmit Holding Register	MSB			WRITE DATA				LSB	WO	NA	0xE000C000 DLAB = 0
U0IER	Interrupt Enable Register	0	0	0	0	0	Enable Rx Line Status Interrupt	Enable THRE Interrupt	Enable Rx Data Available Interrupt	R/W	0	0xE000C004 DLAB = 0
U0IIR	Interrupt ID Register	FIFOs Enabled		0	0	IIR3	IIR2	IIR1	IIR0	RO	0x01	0xE000C008
U0FCR	FIFO Control Register	Rx Trigger		Reserved		-	Tx FIFO Reset	Rx FIFO Reset	FIFO Enable	WO	0	0xE000C008
U0LCR	Line Control Register	DLAB	Set Break	Stick Parity	Even Parity Select	Parity Enable	Number of Stop Bits	Word Length Select		R/W	0	0xE000C00C
U0LSR	Line Status Register	Rx FIFO Error	TEMT	THRE	BI	FE	PE	OE	DR	RO	0x60	0xE000C014
U0SCR	Scratch Pad Register	MSB							LSB	R/W	0	0xE000C01C
U0DLL	Divisor Latch LSB	MSB							LSB	R/W	0x01	0xE000C000 DLAB = 1
U0DLM	Divisor Latch MSB	MSB							LSB	R/W	0	0xE000C004 DLAB = 1

UART0 data registers

- Receiver buffer register
  - U0RBR = 0xE000C000 (read only)
  - read returns top byte of FIFO
    - oldest character received
- Transmitter holding register
  - U0THR = 0xE000C000 (write only)
  - write stores byte as “newest” in the FIFO
    - to be transmitted
- RBR/THR accessible only if “divisor latch” access bit disabled (DLAB=0) in U0LCR

UART0 line control register

U0LCR – 0xE000C00C

Initialize data format & enable/disable divisor latch

U0LCR	Function	Description	Reset Value
1:0	Word Length Select	00: 5 bit character length 01: 6 bit character length 10: 7 bit character length 11: 8 bit character length	0
2	Stop Bit Select	0: 1 stop bit 1: 2 stop bits (1.5 if U0LCR[1:0]=00)	0
3	Parity Enable	0: Disable parity generation and checking 1: Enable parity generation and checking	0
5:4	Parity Select	00: Odd parity 01: Even parity 10: Forced "1" stick parity 11: Forced "0" stick parity	0
6	Break Control	0: Disable break transmission 1: Enable break transmission. Output pin UART0 TxD is forced to logic 0 when U0LCR6 is active high.	0
7	Divisor Latch Access Bit	0: Disable access to Divisor Latches 1: Enable access to Divisor Latches	0

Access Read/Transmit buffers only if DLAB = 0

Baud Rate Generator

- UART sampling clock = 16 x baud rate
  - over-sample input for reliable detection of start bit and timing of data samples of received bits
- Sampling freq. = VLSI Peripheral Bus (VPB) clock (pclk) divided by 16-bit “divisor”

  Fsampling = Fpclk / (MSB:LSB)
  - U0DLL (0xE000C000) = Divisor Latch LSB
  - U0DLM (0xE000C004) = Divisor Latch MSB
    - Accessible only when DLAB=1 in LCR

Example: divisor for 9600 baud

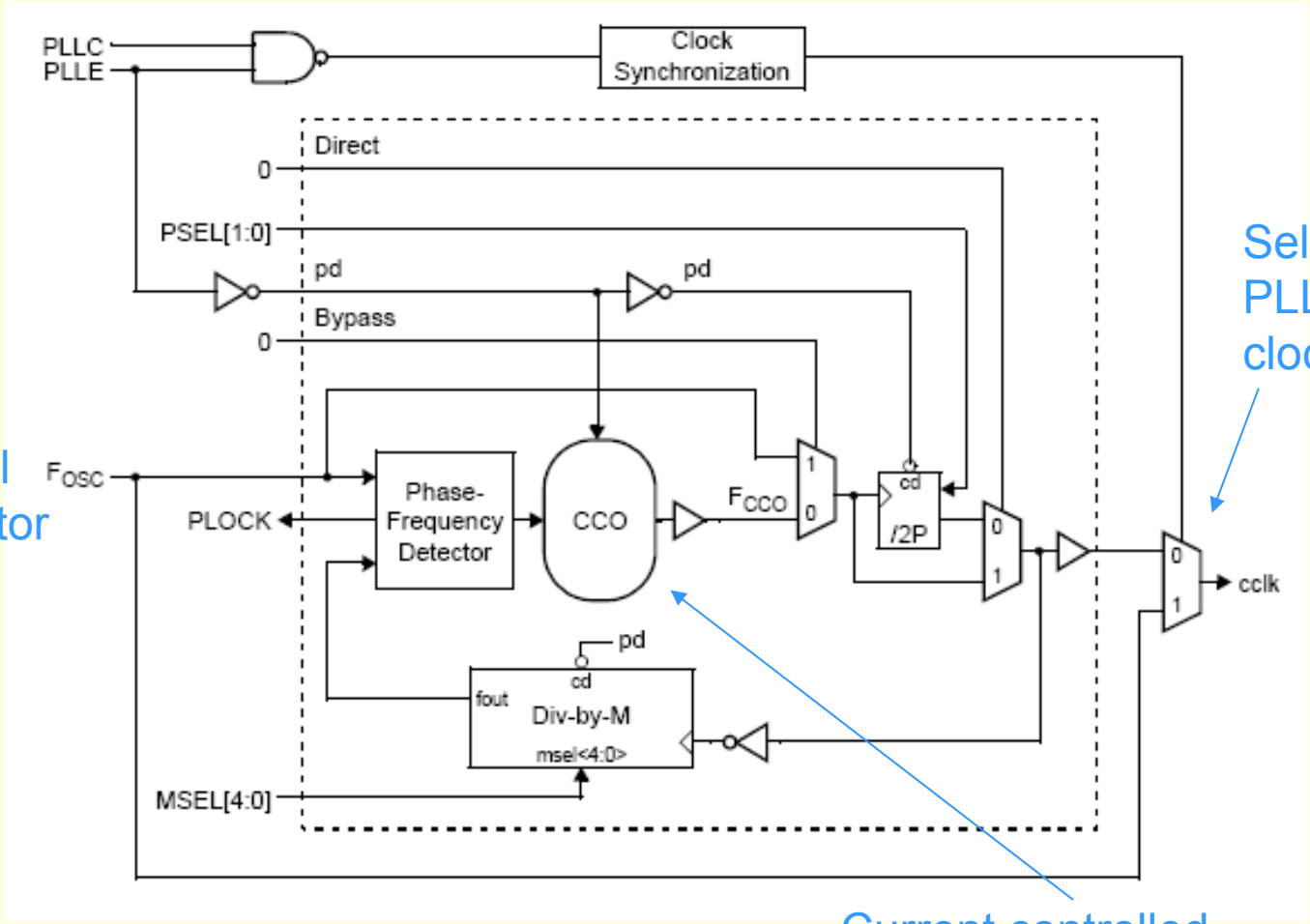
- Assume VPB clock Fpclk= 15MHz
- Fsampling = 16 x 9600 = 153,600 Hz
- Divisor = Fpclk / Fsampling
  = 15MHz/153,600Hz
  = 97.6 ≈ 0x0061
- Program: DLM = 0x00, DLL = 0x61

LPC2292 clocks

Configure in startup code

- uCdragon has 14,7456MHz crystal connected to pins X1/X2 (Xtal frequency for LPC2292 must be 10MHz-25MHz)
  - Oscillator: Fosc = 14.7456MHz
- Phase locked loop (PLL) can generate a higher CPU clock frequency, cclk (next slide)
  - If PLL bypassed: cclk = Fosc
  - Current-controlled oscillator frequency (Fcco) range = 156MHz-320MHz
  - Calculate cclk from programmable factors P & M
    - Fcco = cclk*2*P P = 1,2,4 or 8
    - Fcco = Fosc*M*2*P M = 1-32
- VLSI peripheral bus (VPB) clock (pclk) frequency derived from cclk (programmable)
  - pclk = cclk/N (N=1,2,4*) *default N=4

PLL block diagram



Example: UART initialization

```
ldr     r0,=U0LCR ;point to control reg
mov     r1,#0x83  ;8 data,1 stop,no parity,DLAB=1
str     r1,[r0]   ;write to control reg
ldr     r2,=U0DLL ;point to divisor latch (low)
mov     r1,#0x61  ;low byte of divisor
str     r1,[r2]   ;write to U0DLL
mov     r1,#0x00  ;high byte of divisor
str     r1,[r2,#4] ;write to U0DLM
mov     r1,#0x03  ;DLAB=0
str     r1,[r0]   ;write to control reg
```

C example

```
void init_serial()  {
   pinsel0 = 0x00005000;      //enable TxD,RxD
   U1LCR = 0x83;              //DLAB=1
   U1DLL = 97;                //divisor low
   U1DLM = 0;                 //divisor high
   U1LCR = 0x03;              //DLAB=0
}
```

UART0 FIFO control register

U0FCR – 0xE000C008

Rx “trigger level” = 1, 4, 8, or 14 characters

U0FCR	Function	Description	Reset Value
0	FIFO Enable	Active high enable for both UART0 Rx and Tx FIFOs and U0FCR7:1 access. This bit must be set for proper UART0 opearation. Any transition on this bit will automatically clear the UART0 FIFOs.	0
1	Rx FIFO Reset	Writing a logic 1 to U0FCR1 will clear all bytes in UART0 Rx FIFO and reset the pointer logic. This bit is self-clearing.	0
2	Tx FIFO Reset	Writing a logic 1 to U0FCR2 will clear all bytes in UART0 Tx FIFO and reset the pointer logic. This bit is self-clearing.	0
5:3	Reserved	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
7:6	Rx Trigger Level Select	00: trigger level 0 (default=1 character or 0x01h) 01: trigger level 1 (default=4 characters or 0x04h) 10: trigger level 2 (default=8 characters or 0x08h) 11: trigger level 3 (default=14 characters or 0x0eh) These two bits determine how many receiver UART0 FIFO characters must be written before an interrupt is activated. The four trigger levels are defined by the user at compilation allowing the user to tune the trigger levels to the FIFO depths chosen.	0

Line Status Register

U0LSR = 0xE000C014

Receiver Data Ready
RDR=1 if new char available in RBR

Receive error bits

Transmitter Holding Register Empty
THRE=1 if OK to write new char to THR

U0LSR	Function	Description	Reset Value
0	Receiver Data Ready (RDR)	0: U0RBR is empty 1: U0RBR contains valid data U0LSR0 is set when the U0RBR holds an unread character and is cleared when the UART0 RBR FIFO is empty.	0
1	Overrun Error (OE)	0: Overrun error status is inactive. 1: Overrun error status is active. The overrun error condition is set as soon as it occurs. An U0LSR read clears U0LSR1. U0LSR1 is set when UART0 RSR has a new character assembled and the UART0 RBR FIFO is full. In this case, the UART0 RBR FIFO will not be overwritten and the character in the UART0 RSR will be lost.	0
2	Parity Error (PE)	0: Parity error status is inactive. 1: Parity error status is active. When the parity bit of a received character is in the wrong state, a parity error occurs. An U0LSR read clears U0LSR2. Time of parity error detection is dependent on U0FCR0. A parity error is associated with the character being read from the UART0 RBR FIFO.	0
3	Framing Error (FE)	0: Framing error status is inactive. 1: Framing error status is active. When the stop bit of a received character is a logic 0, a framing error occurs. An U0LSR read clears U0LSR3. The time of the framing error detection is dependent on U0FCR0. A framing error is associated with the character being read from the UART0 RBR FIFO. Upon detection of a framing error, the Rx will attempt to resynchronize to the data and assume that the bad stop bit is actually an early start bit. However, it cannot be assumed that the next received byte will be correct even if there is no Framing Error.	0
4	Break Interrupt (BI)	0: Break interrupt status is inactive. 1: Break interrupt status is active. When RxD0 is held in the spacing state (all 0's) for one full character transmission (start, data, parity, stop), a break interrupt occurs. Once the break condition has been detected, the receiver goes idle until RxD0 goes to marking state (all 1's). An U0LSR read clears this status bit. The time of break detection is dependent on U0FCR0. The break interrupt is associated with the character being read from the UART0 RBR FIFO.	0
5	Transmitter Holding Register Empty (THRE)	0: U0THR contains valid data. 1: U0THR is empty. THRE is set immediately upon detection of an empty UART0 THR and is cleared on a U0THR write.	1
6	Transmitter Empty (TEMT)	0: U0THR and/or the U0TSR contains valid data. 1: U0THR and the U0TSR are empty. TEMT is set when both U0THR and U0TSR are empty; TEMT is cleared when either the U0TSR or the U0THR contain valid data.	1
7	Error in Rx FIFO (RXFE)	0: U0RBR contains no UART0 Rx errors or U0FCR0=0. 1: UART0 RBR contains at least one UART0 Rx error. U0LSR7 is set when a character with a Rx error such as framing error, parity error or break interrupt, is loaded into the U0RBR. This bit is cleared when the U0LSR register is read and there are no subsequent errors in the UART0 FIFO.	0

Example: receiver “busy-wait”

```
        ldr   r0,=U0LSR     ;point to LSR
wait    ldr   r1,[r0]       ;read LSR
        ands  r1,r1,#1      ;test RDR
        beq   wait          ;wait until RDR=1
        ldr   r0,=U0RBR     ;point to RBR
        ldr   r1,[r0]       ;read data
```

Transmitter busy-wait similar

Interrupt enable register

U0IER = 0xE000C004*

4 interrupt sources:

*received data available

*transmitter holding register empty

* character receive time-out

* Rx line error (bits 4-1 of LSR)

U0IER	Function	Description	Reset Value
0	RBR Interrupt Enable	0: Disable the RDA interrupt. 1: Enable the RDA interrupt. U0IER0 enables the Receive Data Available interrupt for UART0. It also controls the Character Receive Time-out interrupt.	0
1	THRE Interrupt Enable	0: Disable the THRE interrupt. 1: Enable the THRE interrupt. U0IER1 enables the THRE interrupt for UART0. The status of this interrupt can be read from U0LSR5.	0
2	Rx Line Status Interrupt Enable	0: Disable the Rx line status interrupts. 1: Enable the Rx line status interrupts. U0IER2 enables the UART0 Rx line status interrupts. The status of this interrupt can be read from U0LSR[4:1].	0
7:3	Reserved	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

*** Accessible when DLAB=0 in lne control register**

Interrupt ID register

U0IIR = 0xE000C008

Allows interrupt handler to determine that there is a pending UART interrupt & cause of the interrupt

U0IIR	Function	Description	Reset Value
0	Interrupt Pending	0: At least one interrupt is pending. 1: No pending interrupts. Note that U0IIR0 is active low. The pending interrupt can be determined by evaluating U0IER3:1.	1
3:1	Interrupt Identification	011: 1. Receive Line Status (RLS) 010: 2a.Receive Data Available (RDA) 110: 2b.Character Time-out Indicator (CTI) 001: 3. THRE Interrupt. U0IER3 identifies an interrupt corresponding to the UART0 Rx FIFO. All other combinations of U0IER3:1 not listed above are reserved (000,100,101,111).	0
5:4	Reserved	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
7:6	FIFO Enable	These bits are equivalent to U0FCR0.	0

Interrupt identification

Interrupt ID # of U0IIR indicates source & priority of interrupt

U0IIR[3:0]	Priority	Interrupt Type	Interrupt Source	Interrupt Reset
0001	-	none	none	-
0110	Highest	Rx Line Status / Error	OE or PE or FE or BI	U0LSR Read
0100	Second	Rx Data Available	Rx data available or trigger level reached in FIFO (U0FCR0=1)	U0RBR Read or UART0 FIFO drops below trigger level
1100	Second	Character Time-out Indication	Minimum of one character in the Rx FIFO and no character input or removed during a time period depending on how many characters are in FIFO and what the trigger level is set at (3.5 to 4.5 character times). The exact time will be: [(word length) X 7 - 2] X 8 + {(trigger level - number of characters) X 8 + 1] RCLKs	U0 RBR Read
0010	Third	THRE	THRE	U0IIR Read (if source of interrupt) or THR write
note: values "0000", "0011", "0101", "0111", "1000", "1001", "1010", "1011","1101","1110","1111" are reserved.				