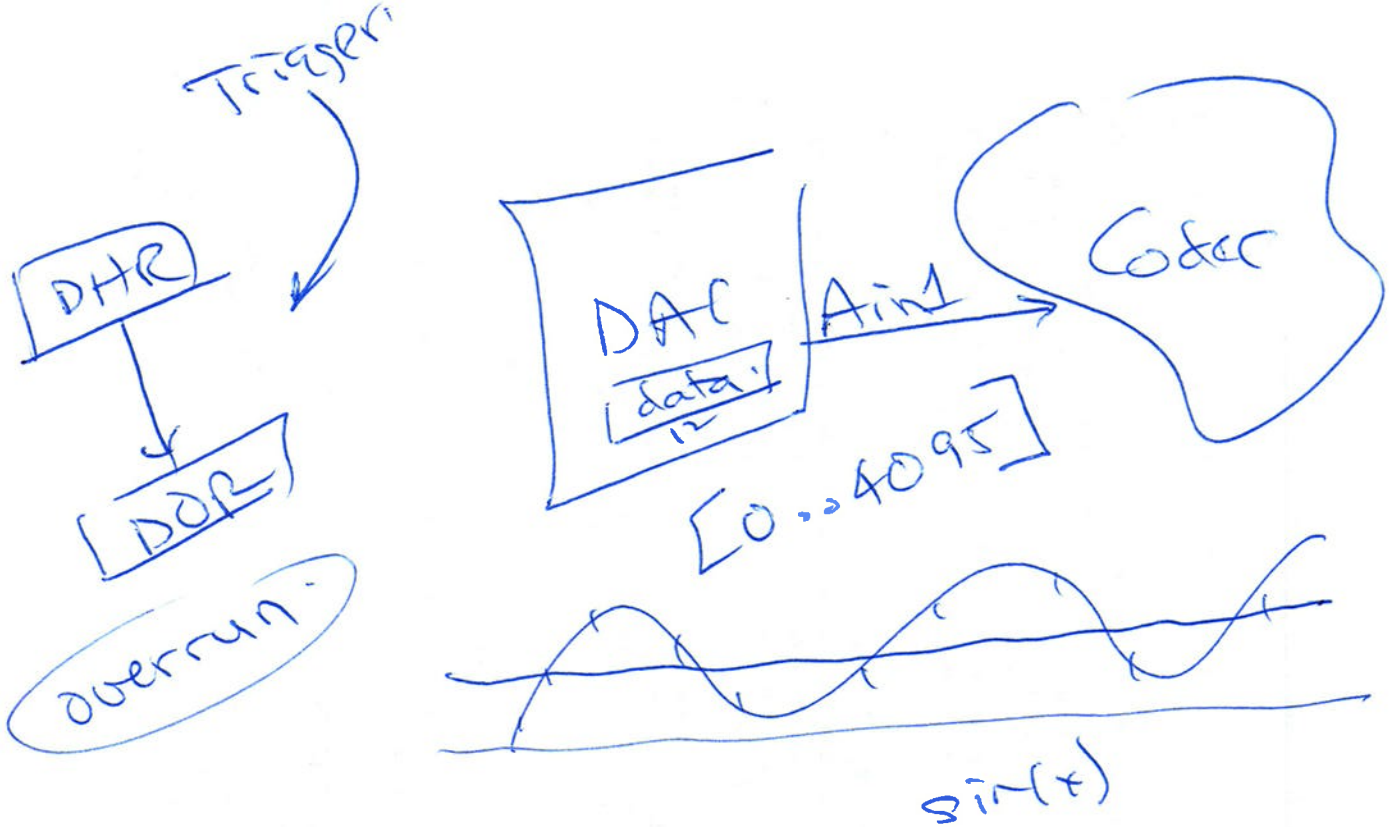

Trigger
DHR
DOR
overrun
DAC
data
12
Ain1
C&C
[0..4095]
sin(x)

Figure 54. DAC channel block diagram

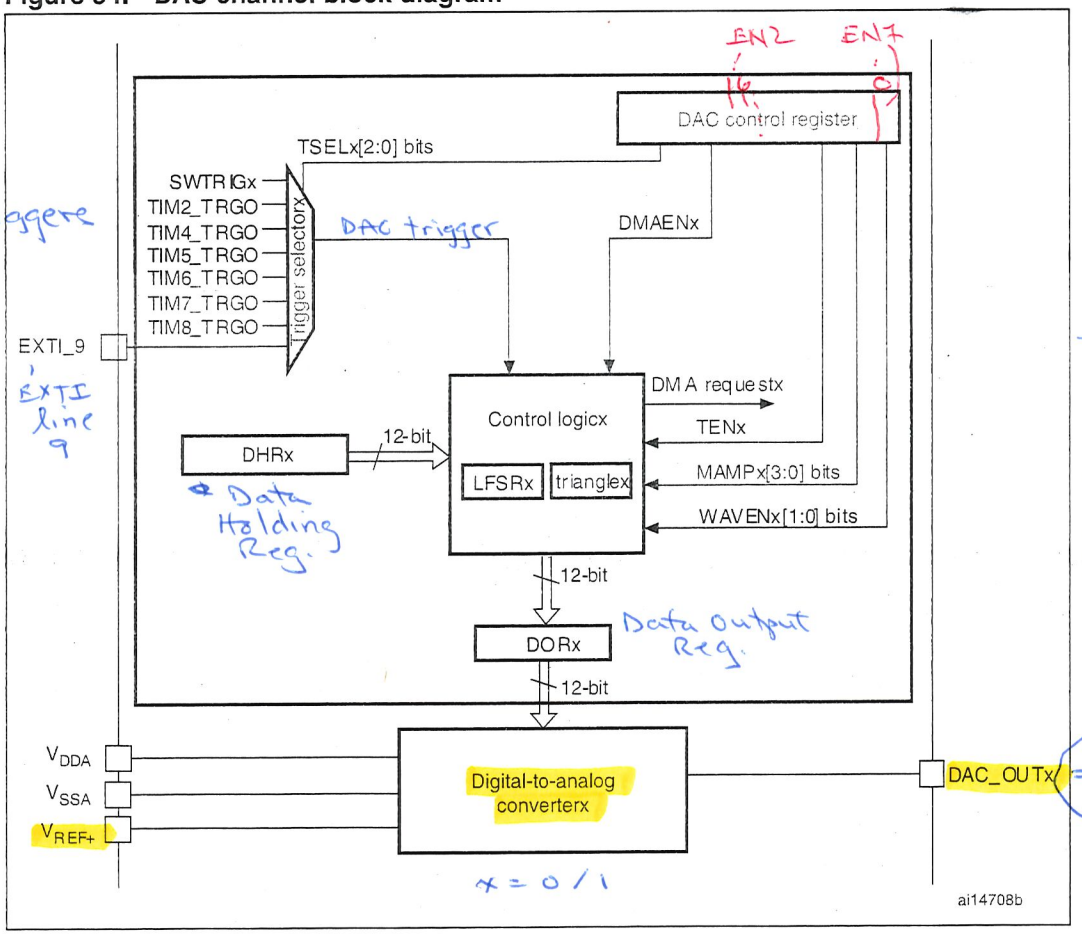
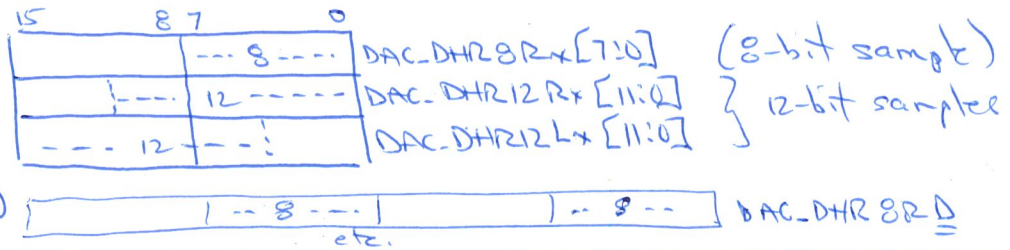
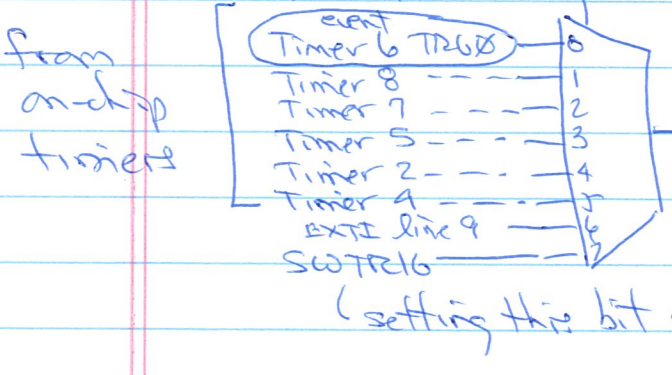


Table 55. DAC pins



DAC_CR [31:16 , 15:0]
DAC2 DAC1

- DMAUDRIE – DMA "under-run" error intr. enable (new request before 1st data used)
- DMAENx – DMA enable
- MAMPx, WAVEx) generate triangle/LFSR noise waveforms
- TSELx[2:0] – trigger select
- TENx – trigger enable (1: trigger DHRx→DORx; 0: write to DHRx data to DORx in one cycle.)



- BOFFx : output buffer disable
- ENx : enable DAC x

DAC_SWTRIGR register:

DAC_DHR12R1 : 12-bit data holding reg/right aligned

DAR_SR : bit 29 = DMAUDR2) under-run flags.
bit 13 = DMAUDR1

Note: Dual-DAC conversion also supported.