

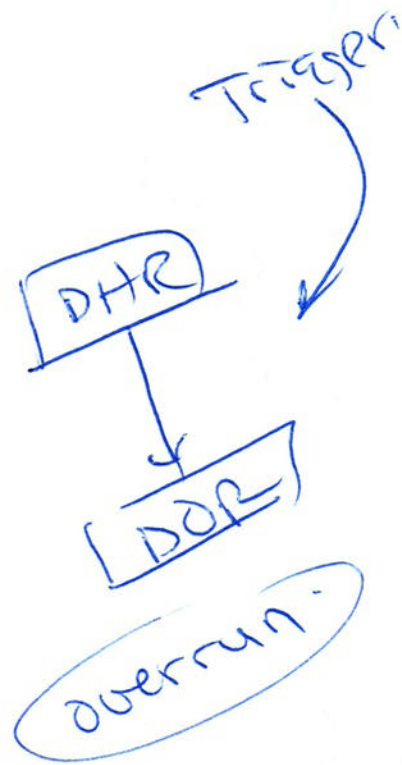


Figure 54. DAC channel block diagram

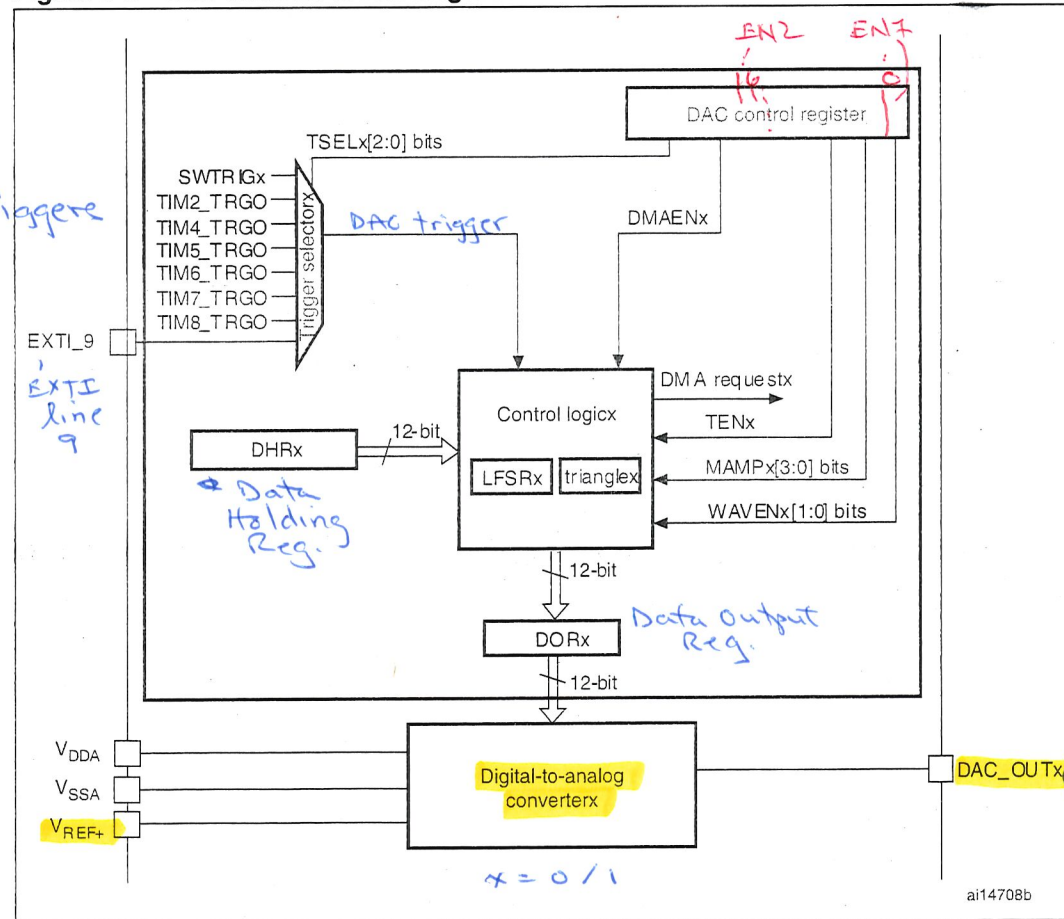


Table 55. DAC pins

Ex:
DAC → DHR12R1 = data;

DAC Init
- clock for GPIO pin
- clock for DAC
- GPIO pin mode analog
- enable DAC

DHR:

15	8	7	0	
		8		①
		12		②
	12		1	③

- ① DAC_DHR8Rx
- ② DAC_DHR12Rx
- ③ DAC_DHR12Lx

Double Convert:

31	23	16	8	0	
		8		8	
		12		12	
	12		12		

DAC_DHR8RD
DAC_DHR12RD
DAC_DHR12LD

$$V_{ref} \times \frac{DOR}{4095} \quad (12\text{-bit})$$

Single Channel Data Reg.

15	8	7	0	
		8		DAC_DHR8Rx[7:0]
		12		DAC_DHR12Rx[11:0]
	12		1	DAC_DHR12Lx[11:0]

(Also "double" value registers)

15	8	7	0	
		8		DAC_DHR8RD
		12		etc.
	12		1	

(8-bit sample)
12-bit samples

DAC_CR [31:16 , 15:0]
DAC2 DAC1

• DMAUDRIE - DMA "under-run" error intr. enable
(new request before 1st data wrd)

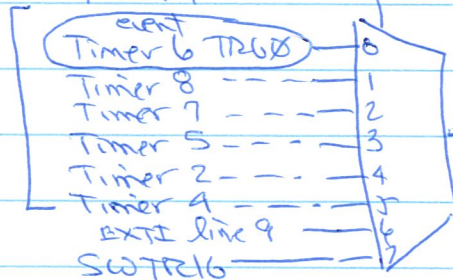
• DMAENx - DMA enable

• MAMPx
• WAVEx } generate triangle/LFSR noise waveforms

• TSELx [2:0] - trigger select

• TENx - trigger enable
1: trigger DHRx → DORx
0: write to DHRx
data to DORx in
one cycle.

from
on-chip
timers



trigger D/A conversion
(DHRx → DORx xfer)

data holding reg data output reg.

(setting this bit start convert.)

• BOFFx : output buffer disable

• ENx : enable DAC x

DAC_SWTRIGR

register: [] SWTRIG2 SWTRIG1

DAC_DHR12R1

: 12-bit data holding reg / right aligned

DAR_SR

bit 29 = DMAUDR2
bit 13 = DMAUDR1 } under-run flags.

Note: Dual-DAC conversions also supported.