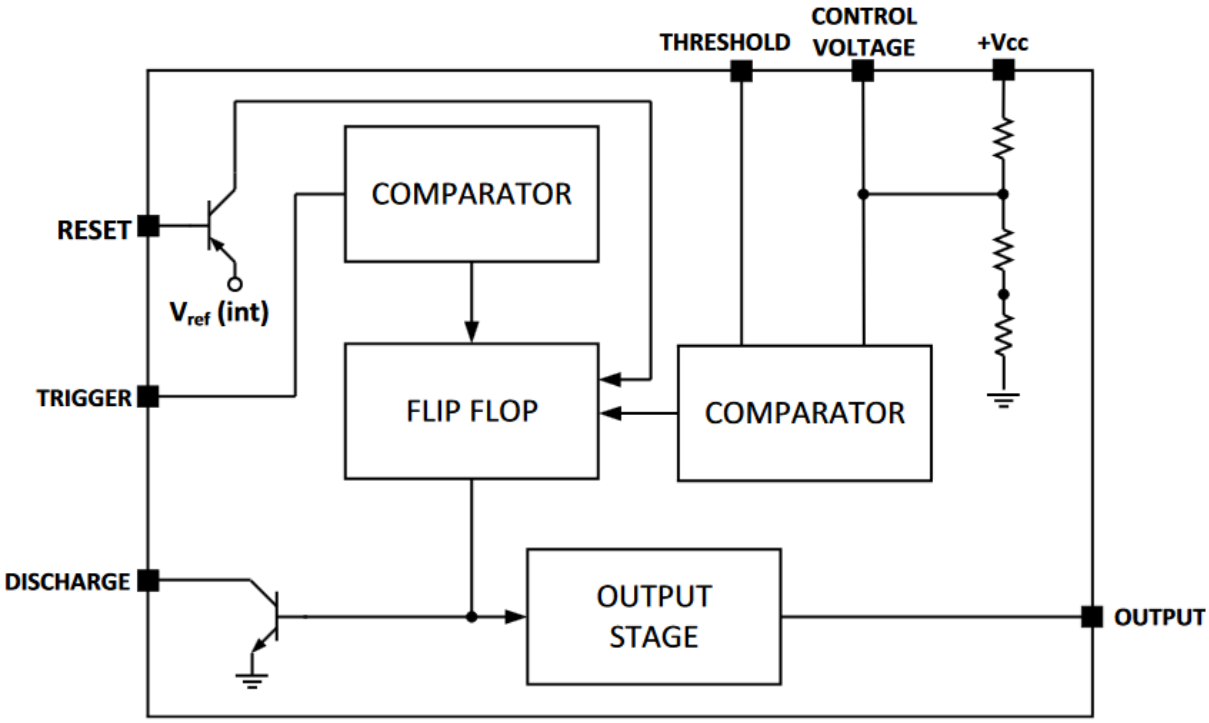
Tuesday 3/2/21

555 Timer Chip

A very popular 8-pin IC for generating time delays and oscillating signals. The original 555 timer chip was released in 1972 by a company called Signetics, in an 8-pin DIP package and an 8-pin SIP package. Signetics (**Sig**nal **Net**work Electron**ics**) was founded in 1961, was sold to Philips in 1975, which is now NXP.

Functional block diagram:

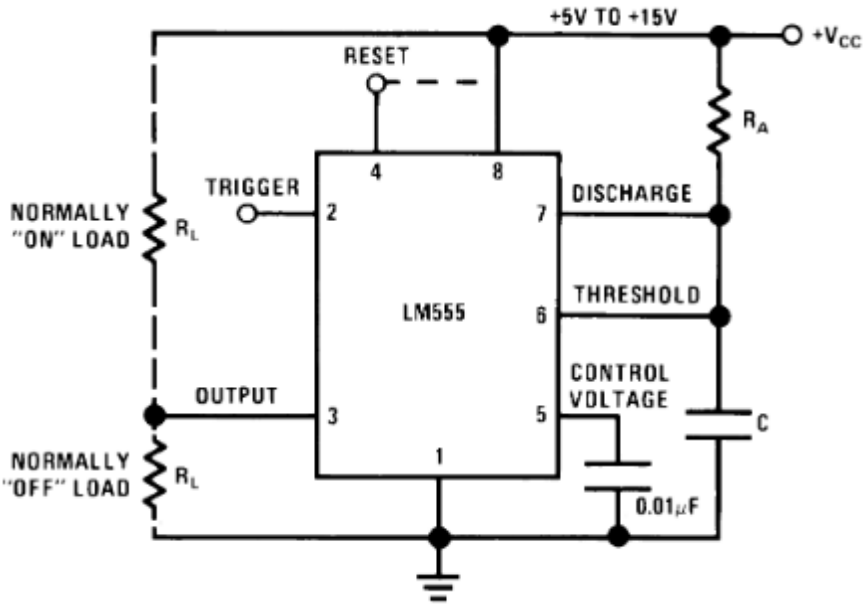


From http://www.ti.com/lit/ds/symlink/lm555.pdf, one of Texas Instruments' versions of the 555

Two modes of operation: monostable (a one-shot), and astable (oscillating).

Monostable Mode

In the monostable mode, the output signal is a single high-level pulse (with R_L tied to ground) that you trigger and the external passive components determine the pulse length. The pulse length can range from μs to hours.

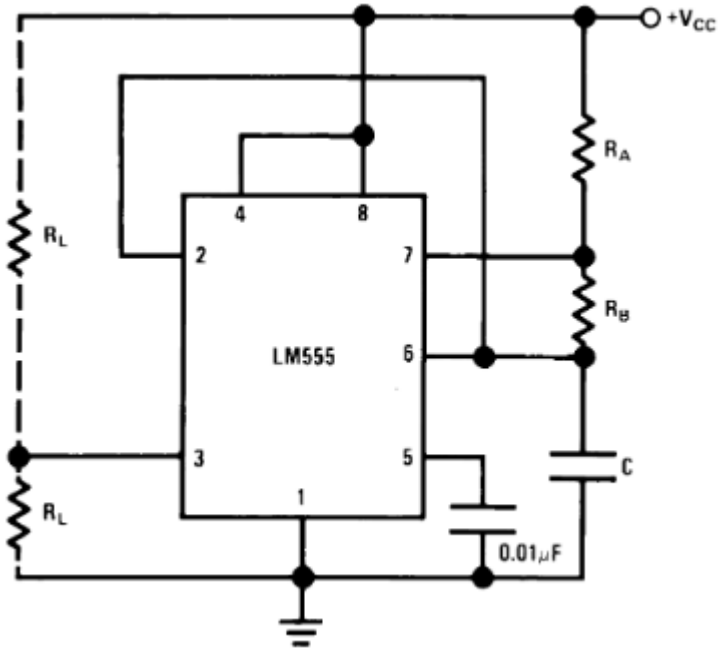


The output is initially low and the trigger input is initially high. Application of a negative going trigger pulse, less than $V_{cc}/3$, starts the process. At this time, the output goes high. When $t = 1.1R_AC$, the output goes back low and stays low until another trigger pulse is applied. The time of the pulse is due to the voltage across C growing exponentially through R_A.

With R_L tied to ground, the pulse "turns on" the load for the duration of the pulse. For R_L tied to V_{cc}, the pulse "turns off" the load for the duration of the pulse.

Astable mode

In the astable mode of operation, the output is a pulse train. It can be a square wave, but it does not have to have a 50% duty cycle.



Capacitor C continually charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. The output is high during the charge time, which is determined by $t_c = 0.693\ (R_A+R_B)C$.

The output is low during the discharge time, which is determined by $t_d = 0.693R_BC$.

Therefore the oscillation period, T, is $T = t_c+t_d$, and

$$f = \frac{1}{T} = \frac{1.44}{C(R_A + 2R_B)}$$

Pin 3 is the output pin. Same R_L convention as in the monostable mode.

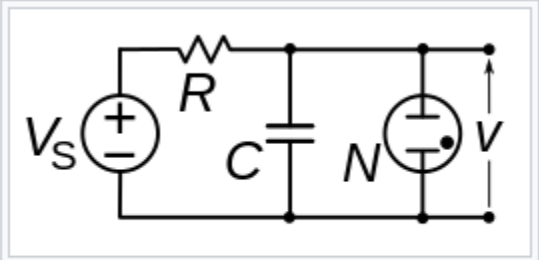
The 556 IC has two 555 timers on it.

The Pearson-Anson Effect

Discovered in 1922 by Stephen Pearson and Horatio Anson.

Some two terminal devices, including a neon lamp, maintain a high resistance between the terminals for any voltage less than a breakdown voltage, V_b. Once V_b has been reached, the resistance between the two terminals drops substantially, and remains low until the voltage across the terminals drops to some extinction voltage, V_e. With the neon lamp, dielectric breakdown occurs when V_b is reached, resulting in a low resistance plasma forming in the gas.

With this effect, a simple relaxation oscillator can be realized:



Pearson-Anson oscillator circuit

Curtesy Wikipedia

C charges through R from the DC voltage source, V_s, until V reaches V_b. Then the neon lamp, N, turns on and C quickly discharges until V reaches V_e. Then the lamp turns off and C begins to charge through R again… The output voltage, V, is a sawtooth waveform.

VCO's, DDS and PLLs

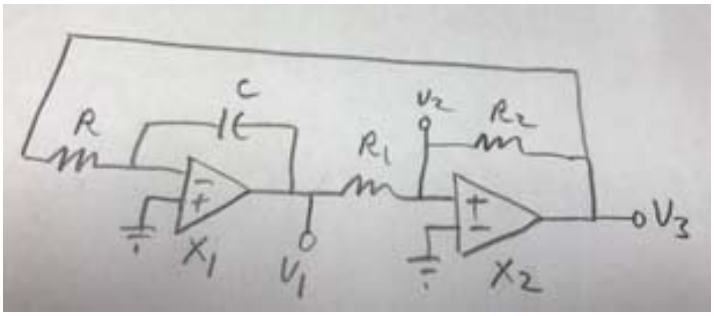
1) VCO

A VCO is a voltage controlled oscillator. How is that realized?

Most oscillators have an oscillation frequency or fundamental frequency inversely proportional to RC or the square root of LC.

One option is to use a FET as a voltage controlled resistance to affect the R in a RC time constant controlled oscillator. However, this can be problematic in an oscillator where the output signal goes positive and negative (body diode in a MOSFET, nonsymmetrical response about 0V V_{gs} in a jFET).

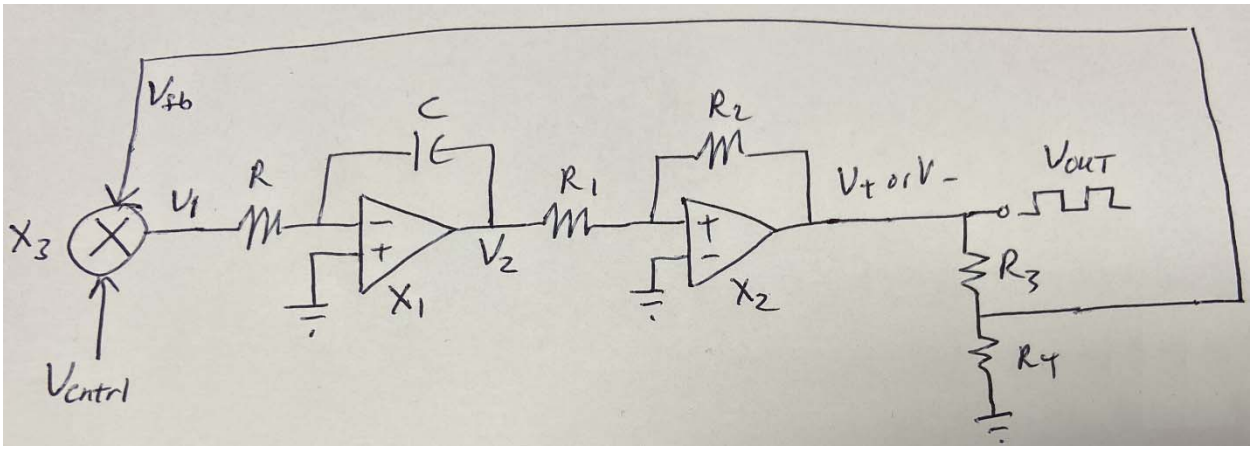
Consider again the op amp based relaxation oscillator:



V_3 is a square wave output signal. The oscillation frequency is:

$$f = \frac{1}{T} = \frac{R_2}{4R_1RC}$$

Where RC is from the integrator stage. Consider the effect of adding a four quadrant multiplier into the circuit:



V_{cntrl} is a small DC control voltage and $V_{cntrl} > 0$ V.

V_{OUT} is a square wave with voltages alternating between V+ and V-.

V_{fb} is the feedback voltage and is attenuated from V_{OUT} by the R_3:R_4 voltage divider according to:

$$V_{fb} = V_{OUT}\frac{R_4}{R_3+R_4}.$$

V_1 is the input voltage to the integrator subcircuit. X_3 is a four quadrant multiplier and its's output voltage, V_1, is the product of V_{fb} and V_{cntrl}. Assuming that V_{cntrl} changes much more slowly than the integrator's RC time constant, then

$$v_2 \approx V_{o1} - \frac{V_1}{RC}t \qquad \text{for t} \geq 0\text{s},$$

where V_{01} is the initial voltage across the capacitor at t = 0 s. From the previous analysis of the op amp relaxation oscillator:

$$0 = \left(-V_{-}\frac{R_1}{R_2} - \frac{V_1 t}{RC}\right)R_2 + V_{+}R_1,$$

which can be rewritten as:

$$t = \frac{RC}{V_1}(V_{+} - V_{-})\frac{R_1}{R_2},$$

which leads to:

$$f = \frac{1}{T} = \frac{1}{2t} = \left(\frac{V_1}{V_{+}-V_{-}}\right)\frac{R_2}{2R_1RC}.$$

Let's assume that $V_{+} = -V_{-}$, leading to:

$$f = \frac{1}{T} = \frac{1}{2t} = \left(\frac{V_1}{V_{+}}\right)\frac{R_2}{4R_1RC}.$$

With the op amp relaxation oscillator, $V_1 = V_{+}$, leading to:

$$f = \frac{R_2}{4R_1RC}.$$

But here,

$$V_1 = V_{cntrl}V_{fb} = V_{cntrl}V_{+}\left(\frac{R_4}{R_3+R_4}\right).$$

Therefore, for this square wave VCO:

$f = V_{cntrl}\left(\frac{R_4}{R_3+R_4}\right)\frac{R_2}{4R_1RC}$,

for V_{cntrl} a DC voltage and $V_{cntrl} > 0$ V

where f is the fundamental frequency of the V_{out} output square wave.

If V_{cntrl} is not a DC voltage, such as:

$V_{cntrl} = V_a + V_b \sin(\omega t)$,

where V_a is DC and $V_a > |V_b| > 0$ V,

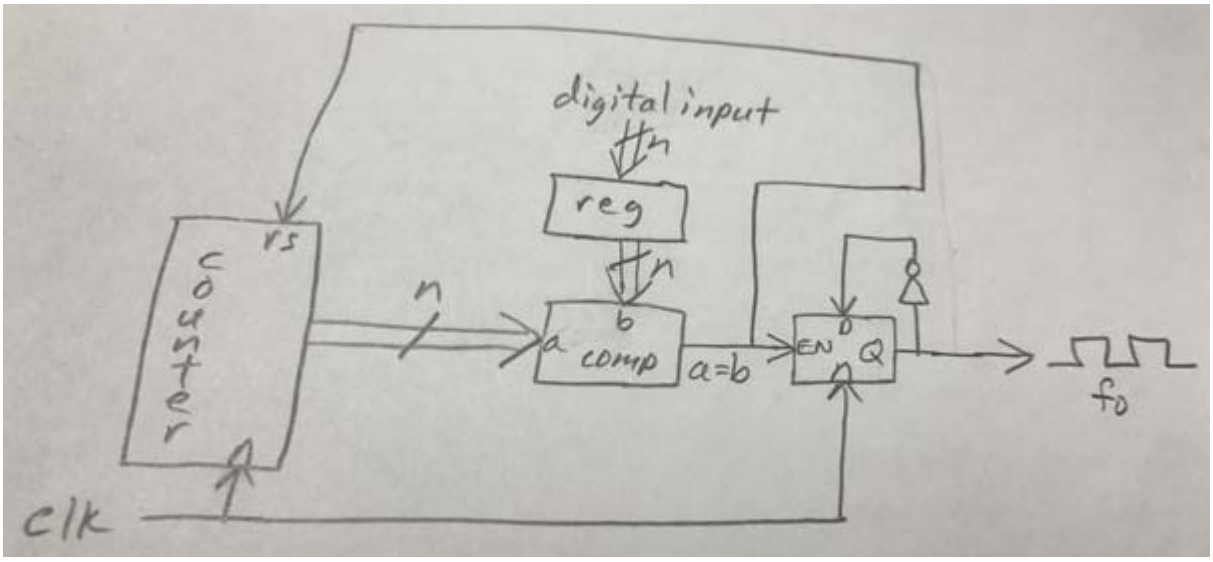
the integral of V_1 has to be recalculated and the math gets more complicated.

However, the fundamental frequency of the output square wave will change with the time varying input sinusoid and the range of f will increase in proportion to the amplitude of the input sinusoid, similar to FM.

Note, if $V_{cntrl} = 0$ V, V_{out} will be stuck at V+ or V-.

2) Digitally Controlled Oscillator

A variable frequency square wave can also be created by dividing down the frequency of a high frequency clock:



Digital input range: 1 to 2^n

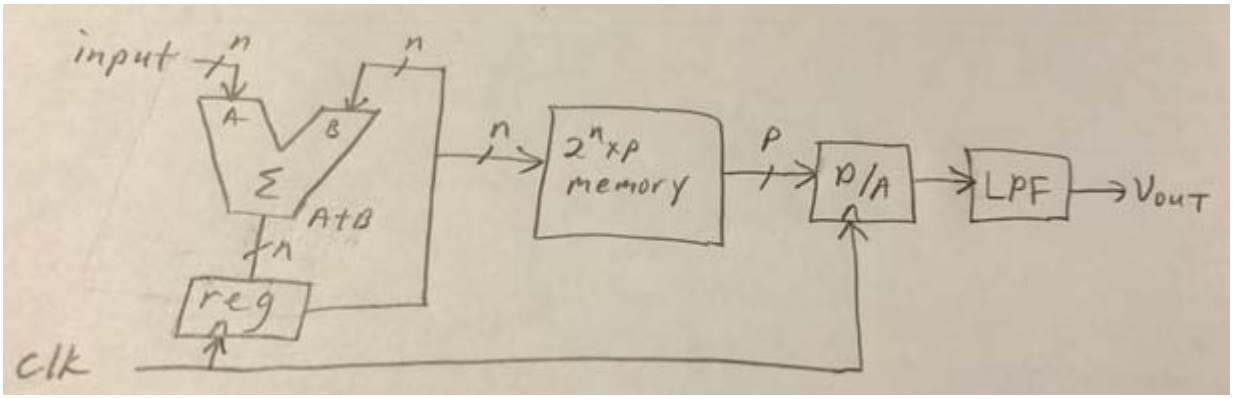
$$f_o = \frac{f_{clk}}{2(digital\ input)}$$

This digital circuit can easily be implemented in an FPGA or similar device.

An analog input signal could be run through an A/D to generate the digital input signal, thus realizing a VCO.

3) Direct Digital Synthesis (DDS)

Using a 2^nxp memory, store one cycle of a sine wave: 2^n samples [sin(2π/n)] with p-bit amplitude resolution.

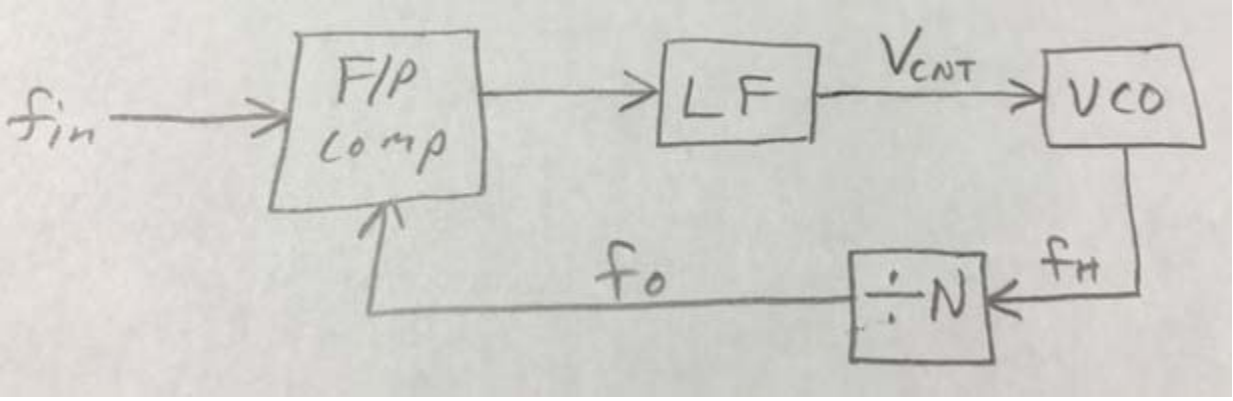


If input is 1, it takes 2^n clk cycles to go through (read out) the entire memory. The frequency of the output sinewave will then be $f_{CLK}/2^n$. As the input number increases, it takes fewer clk cycles to go through the address space of the memory, proportionally increasing the frequency of the output sinewave. The LPF is needed to reduce high frequency noise and to smooth the output sinewave. The output sinewave is directly digitally synthesized, hence the name "DDS."

Any waveform could be stored in the memory and run through the D/A and LPF to create arbitrary analog waveforms. Traditionally, high frequency versions were called a DRFM, for Digital RF Memory, and were used in radar systems

4) Phase Locked Loops (PLL)

A PLL frequency and phase locks a voltage controlled oscillator (VCO) to an input periodic signal (sinewave or square wave).



F/P comp: frequency / phase comparator – produces a signal indicating the frequency and/or phase difference between the two input periodic signals. Implementations include four quadrant multipliers, mixers, and logic circuits

LF: loop filter, often a lowpass filter. The output (V_{CNT}) drives the VCO. A LF may contain an integrator so that the error between f_{in} and f_o is driven to zero.

VCO: voltage controlled oscillator. The output, f_H, may be a sinewave or a square wave.

/N: "divide by N" : a digital clock divider (often a synchronous counter) is used to reduce f_H to f_o (with square wave signals). This can allow multiple frequency and phase locked clocks at different frequencies (and even phases) to be generated. This stage is not required in a PLL though.

Applications of PLLs:

(1) As a frequency synthesizer (uses the /N stage).
(2) FM demodulation. V_{CNT} is the demodulated output signal.
(3) Clock signal generation and synchronization.
(4) Recovering a carrier or clock signal from noise, or if occasional pulses are missing.
(5) As sensor instrumentation when a measurand variable frequency oscillator is used as/with the sensor. V_{CNT} can then be proportional to the measurand.

Implementation can be all analog, analog and digital, all logic circuit based, or s/w defined with A/Ds and D/A's. They can be built at the component level or purchased as a complete system.

A PLL once frequency lock is achieved can be modelled as a linear feedback control system to lock the phase. Frequency locking a PLL is a highly nonlinear process.

FLLs (frequency locked loops) are similar and possibly a little simpler to implement, since the frequency is known and only the phase has to be locked.

ANALOG DEVICES

155.52 MHz Frequency Synthesizer

AD809

FEATURES

Frequency Synthesis to 155.52 MHz
19.44 MHz or 9.72 MHz Input
Reference Signal Select Mux
Single Supply Operation: +5 V or –5.2 V
Output Jitter: 2.0 Degrees RMS
Low Power: 90 mW
10 KH ECL/PECL Compatible Output
10 KH ECL/PECL/TTL/CMOS Compatible Input
Package: 16-Pin Narrow 150 Mil SOIC

PRODUCT DESCRIPTION

The AD809 provides a 155.52 MHz ECL/PECL output clock from either a 19.44 MHz or a 9.72 MHz TTL/CMOS/ECL/PECL reference frequency. The AD809 functionality supports a distributed timing architecture, allowing a backplane or PCB 19.44 MHz or 9.72 MHz timing reference signal to be distributed to multiple 155.52 Mbps ports. The AD809 can be applied to create the transmit bit clock for one or more ports.

An input signal multiplexer supports loop-timed applications where a 155.52 MHz transmit bit clock is recovered from the 155.52 Mbps received data.

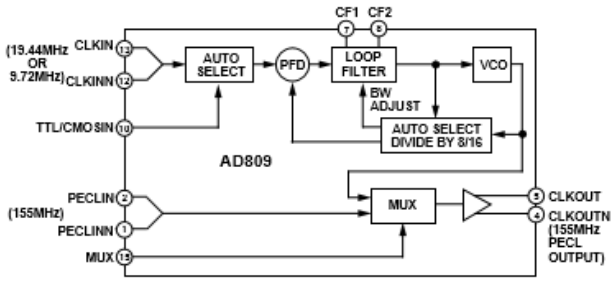
The low jitter VCO, low power and wide operating temperature range make the device suitable for generating a 155.52 MHz bit clock for SONET/SDH/Fiber in the Loop systems.

The device has a low cost, on-chip VCO that locks to either 8× or 16× the frequency at the 19.44 MHz or 9.72 MHz input. No external components are needed for frequency synthesis; however, the user can adjust loop dynamics through selection of a damping factor capacitor whose value determines loop damping.

The AD809 design guarantees that the clock output frequency will drift low (by roughly 20%) in the absence of a signal at the input.

The AD809 consumes 90 mW and operates from a single power supply at either +5 V or –5.2 V.

FUNCTIONAL BLOCK DIAGRAM



REV. A

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