Probabilistic Soft Error Rate Estimation from Statistical SEU Parameters*

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Abstract

Nanometer CMOS VLSI circuits are highly sensitive to soft errors, also known as single-event upsets (SEU) that induce current pulses at random times and at random locations in a digital circuit. Environmental causes of SEU include cosmic radiation and high-energy particles. Our neutron induced soft error rate (SER) estimation method propagates single event transient (SET) pulses through the affected logic circuit. A pulse is modeled by two parameters, a probability of occurrence and a probability density function of the pulse width. We consider the entire neutron linear energy transfer (LET) spectra of the terrestrial background in our analysis. Failures in time (FIT) rates are calculated for ISCAS85 benchmark circuits. In comparison to the reported SER analysis work, our method considered many more factors like the sensitive region of a device, electrical masking and circuit technology that influence the SER. A comparison with measured SER for SRAMs shows better relevancy of our work over other published work. Our CPU times are reasonable; benchmark circuit C1908 with 880 gates requires only 1.14 seconds. We conclude that soft error estimation is highly sensitive to factors like sensitive regions, process variation and circuit characterization. Field test or accelerated test data on logic devices would be needed to further validate the accuracy of the analysis.

1 Introduction

Soft errors, or Single Event Upset (*SEU*), used to be one of the major concerns for avionics and space mission applications during past decades, now become a major bottleneck for ground-based electronic reliability. Soft errors are defined as radiation errors in microelectronic circuits caused when charged particles striking at the sensitive regions in the silicon of a circuit. Soft errors on SRAM or DRAM memories were extensively studied at the end of the twentieth century [6]. Because memories have high density of components and integrate large amount of storage elements, they are more sensitive to soft errors than logic circuits.

Continuous downscaling of CMOS technologies results in clock frequencies reaching the multiple gigahertz range, supply voltage decreasing below one volt level and load capacitances of circuit nodes dropping to femtofarads. Therefore, soft error rate in logic and processors are increasing with these technology trends. In addition, if other circuit noises such as cross coupling, ground bounce are considered as soft errors, the logic FIT (*failure in time*, 1 FIT = 1 fail in 10^9 hours) rate is expected to increase faster and finally the FIT rate in logic is likely to be comparable to the FIT rate in memory [10]. The SER due to high-energy neutrons in SRAM cells, latches, and logic circuits for feature size from 600nm to 50nm were studied and have been reported [26]. According to that study, the SER per chip of logic circuits is expected to increase nine orders of magnitude from 1992 to 2011, becoming comparable to the failure rate of unprotected on-chip memories.

Well-known noise sources include noisy power supply, lightning and electrostatic discharge (ESD), ground bounce, and interconnect coupling capacitances. With advances in the design and manufacturing technology, the non-environmental conditions may not be the dominant affect for the submicron semiconductor reliability. However, the errors caused by cosmic rays and alpha particles will

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remain the prevalent reliability factor in electronic systems. The detail discussion on the source of alpha particles and neutrons and their effects on electronics can be found in a recent tutorial paper [30].

In Section 2, we will review our novel environment dependent soft error model. This soft error model is based on both error occurrence rate represented as a probability, and the single event transient (SET) pulse density represented as a probability density function. The detailed SER calculation algorithms are described in our recent work [29, 31]. In Section 3, we compare our analysis results with relevant published work. In Section 4, we discuss various key factors that may influence logic SER. Some of those factors are barely considered in existing logic SER estimation work.

2 Previous Work

The soft error rate estimation means predicting the soft-error rate due to cosmic and high-energy particle radiation in integrated circuit chips by building reasonably accurate SER analysis models. A prediction of SER needs not only the SER simulation using actual circuit characteristics like device technology and manufacturing process, but also accurate data on radiation environment.

Traditional soft-error testing seeks to reproduce and then accelerate the die's real-life environment [13]. Typically a neutron beam accelerator is used to conduct the test. SER testing is frequently used to evaluate chip SER by using a tester containing hundreds of chips and evaluating their fail rate at nominal conditions. Field testing is very expensive and always takes up to a year to obtain the reliable results but it is important to validate modeling and accelerated testing. The long delay to get the SER results is usually unacceptable for contemporary chip market. The alternative is either costly test more chips with bigger tester or deviate from the nominal conditions and lead the test in a more sensitive state [35]. For example, the test facilities in the Jungfraujoch lab in Switzerland locate at 11,000 feet, which can accelerate ground-level test times by a factor of 11. In this lab, *iRoC Technologies* obtained a statistically significant number of soft errors on different devices over a period of 4 to 6 months [17].

The standard procedures and requirements for terrestrial SER testing of ICs should follow the semiconductor industry–specified accelerated testing methods. The JEDEC (*Joint Electron Device Engineering Council*) standard includes JESD89, JESD89-A [11] and JESD89-2. In JESD89 [11], the standard specifications cover soft errors due to alpha particles and atmospheric neutrons. Also, the standard requirements and procedures for terrestrial SER testing of integrated circuits, and the standardized methodology for reporting the results of the tests are defined. For example, these standards specify that, the SER data obtained from alpha accelerated SER tests should be extrapolated to an alpha flux of 0.001 particles/hr-cm^2; and the neutron accelerated SER (*ASER*) test results to the typical neutron flux observed at New York City, which the reported data shows when the energy is range of 10–10000 MeV, the neutron flux is 3.9×10^{-3} N/cm^2-s and when the energy range is from 1 to 10 MeV, the neutron flux is 4.0×10^{-3} N/cm^2-s [9, 11]. Primarily, the procedures apply to memory devices like DRAMs and SRAMs, but with some adjustments they can be used for logic devices [11].

The existing computer programs to calculate soft error rate or to model the single event effects (*SEE*) on electronics include SEMM, developed by IBM [27]; CRIME, mainly supported by U.S. Air Force and Office of Naval Research grant [4] and CREME96 developed by Naval Research Laboratory [28].

Due to the specific characterizations of logic circuits, SER analysis for logic circuits poses a big challenging for electronic reliability analysis. Unlike memories, the soft errors occurs in the logic circuit may be filtered out by the circuit itself thus may not effect the circuit performance. These masking effects are commonly known as logic masking, electrical masking and temporal masking [19]. Analytical methods are widely used to model soft errors probabilistically for logics. Asadi *et al.* [2] presented a soft error rate estimation technique based on error probability propagation. Rejimon and Bhanja [25] gave a single event fault model based on probabilistic Bayesian networks, which capture spatial dependencies. However, these approaches do not take the circuit electrical masking factor and the characteristic of transient pulses like pulse widths into account. An improvement was provided by Zhao *et al.* [33]. They proposed a constraint-aware robustness insertion methodology that protects the sequential elements in digital circuits against various noise effects. However, in that work the authors did not include the environmental factors like the error frequency. Besides, their propagation method required tabulating all the pulse width and height data for each

logic gate. It would thus take enormous memory for large logic circuits. Some other good logic circuit SER estimation works include SEAT-LA [22], SERA [32] and [24].

In [18], a cost effective approach to selectively protect high susceptibility of nodes in logic circuits by duplication was presented. A recent paper [16] proposed an approach using symbolic based on Binary Decision Diagrams, Algebraic Decision Diagrams and probabilistic model for sequential SER analysis. Rewriting, with optimization for area and power consumption, can also be used for reducing the soft error rate [1].

3 An Environment-Based Probabilistic Soft Error Model

Different from memories, in a logic circuit, single event effect exists as a single event transient (SET) pulse. An SET has its unique characteristics like polarity, waveform, amplitude and duration, and these characteristics depend on particle impact location, particle energy, device technology, device supply voltage and output load. A single event upset does not occur unless the SET can survive the circuit masking effects and being captured by a clock edge of the sequential element [17].

Environmental neutrons come from cascaded interactions when galactic cosmic rays traverse earth's atmosphere. These neutrons reach the ground with finite probabilities [20]. The intensity of cosmic-ray induced neutrons flux in the atmosphere varies with altitude, location in the geomagnetic field, and solar magnetic activity. The flux rate data is available from the reported measurement records over decades [15]. Each neutron has a unique energy when it arrives to the ground. Not every particle hit on the sensitive silicon area can induce an error. An SEU occurs with certain probability for each high-energy particle hit. Such probability can be obtained from existing computer programs, for example, IBM's SEMM (Soft Error Monte-Carlo Modeling) program [27]. Although we did not use the SEMM program in our experiment on logic circuits, we mention it to illustrate how the error probability can be derived.

In our analysis, we consider all energy components in our proposed soft error model, we average the error probability over different energies and assign each circuit node with a unique error occurrence probability value.

The particle energy distribution under specific locations for specific technology nodes can also be obtained from experimental measured results. For example, the cosmic particle strikes were simulated using a heavy ion beam at the Twin Tandem Van de Graaff accelerator at Brookhaven National Laboratory and the results suggest that in the natural environment of space the probability distribution of high-energy particles falls rapidly with increasing LET. For both 0.5μ and 0.35μ CMOS technology processes at the ground level, the largest population has an linear energy transfer (LET) of $20MeV\text{-}cm^2/mg$ or less and the particles with LET greater than $30MeV\text{-}cm^2/mg$ are exceedingly rare [8]. These data will be used in our experiments in Section 4.

The transient current pulse created by a particle strike for each given LET can be calculated from double exponential equation [14]:

$$\begin{cases} I(t) = \frac{Q_{coll}}{\tau_\alpha - \tau_\beta}(e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}}) & \text{(a)} \\ Q_{coll} = 10.8 \times L \times LET & \text{(b)} \end{cases} \quad (1)$$

where Q_{coll} is the collected charge in the sensitive region, τ_α is the collection time constant, which is a process-dependent property of the junction, and τ_β is the ion-track establishment time constant, which is relatively independent of the technology. In bulk silicon, a typical charge collection depth (L) is 2μ for every 1 $MeV\text{-}cm^2/mg$, and an ionizing particle deposits about $10.8fC$ charge along each micron on its track. Typical values are approximately $1.64 \times 10^{-10} sec$ for τ_α and $5 \times 10^{-11} sec$ for τ_β from measurements [3, 33].

By charging and discharging the circuit node capacitance, the single event transient current pulse is converted into a transient voltage pulse in Figure 1. Figure 2 gives a neutron-induced soft error model for logic circuits. Because the probability per hit is related to the neutron flux which is location dependent, we can easily get the circuit SER in units of *FIT* for different locations if the corresponding neutron flux data is available.

In summary, this probabilistic soft error model is based on two considerations: (1) the SEU occurrence rate, presented as probability and (2) once an SEU occurs, it exists in the logic circuit as SETs with different pulse widths represented as a probability density function.

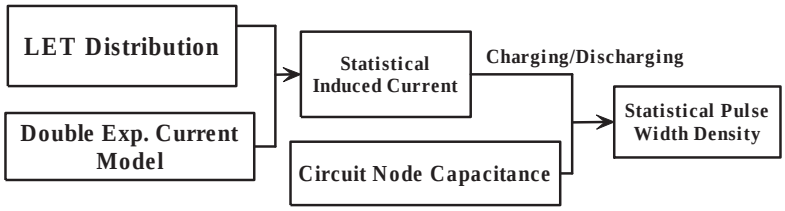

Figure 1. Transforming statistical neutron energy spectrum to SET width statistics.

Table 1. Comparison of Experimental Results on ISCAS85 Benchmark Circuits.

Circuit	# PI	# PO	# Gate	our approach T(s)	our approach (FITs)	Rao et al. [24] T(s)	Rao et al. [24] (FITs)	Rajaraman et al. [22] T(min)	Rajaraman et al. [22] Error Prob.
c432	36	7	160	0.04	1.18×10^3	<0.01	1.75×10^{-5}	108	0.0725
c499	41	32	202	0.14	1.41×10^3	0.01	6.26×10^{-5}	216	0.0041
c880	60	26	383	0.08	3.86×10^3	0.01	6.07×10^{-5}	102	0.0188
c1908	33	25	880	1.14	1.63×10^4	0.01	7.50×10^{-5}	1073	0.0011

Computing Platform	Sun Fire 280 R	Pentium 2.4 GHz	Sun Fire v210
Circuit Technology	TSMC035	Std. 0.13μm	70nm BPTM*
Altitude	Ground	Ground	N/A

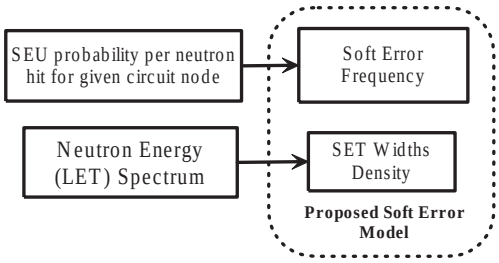

Figure 2. Proposed probabilistic neutron induced soft error model for logic.

4 Experimental Results

In this section, we compare our experimental results with the relevant published works and discuss various key factors that may influence logic SER. Some of those factors have not been considered in the existing logic SER estimation work. For a detailed algorithm to propagate soft errors through elementary logic gates and the algorithm to calculate circuit SER, please refer to the previous published paper [31]. We simulated ISCAS85 benchmark circuits by a simulator developed in C programming language. For simplicity, we assume that all circuits are working at the ground level and the probability of SEU per particle hit is 10^{-4}. We have neglected the polarity of SETs and the temporal masking factor. At ground level we use the neutron energy statistics assuming the SET width density per circuit node follows a *normal* distribution with mean $\mu = 150$ and standard deviation $\sigma = 50$. These assumptions are justified for relatively small values of particle flux and small chip area. From [34], the total neutron flux at sea level is $56.5m^{-2}s^{-1}$. For a CMOS circuit in TSMC035 technology, we assume the sensitive region to be $10\mu m^2$ for each circuit node. For a circuit with n primary outputs and m nodes, the circuit SER is $\Sigma_{i=0}^{n}(\Sigma_{j=0}^{m} SER_{i\_caused\_by\_j})$ which is different from [31], in which we calculated the SER per gate per output $(\frac{1}{n}\Sigma_{i=0}^{n}(\frac{1}{m}\Sigma_{j=0}^{m} SER_{i\_caused\_by\_j}))$. The unit for SER is in FIT. In Table 1, we compare our SER results for selected benchmark circuits with available results; not all benchmark circuit SER results have been published. We see our results pose several orders of magnitude difference compared with the results from Rao et al [24]. The term BPTM marked with asterisk (*) stands for Berkeley Predictive Technology Model. The running time of our approach for big circuit is also acceptable. For example, for C1908 with 880 gates, the simulation running time is only 1.14 second. Field test data for logic circuits is largely unavailable but the actual neutron experiments on a test chip in the future will help validate our analysis. However, the measured data for SRAM memories is available. In Table 3, we compare our work and the estimated logic SER from Rao et al. with the reported SRAM SER from measurement.

We can see, our results show better relevancy with the measured SRAM SER. The CPU times for these results are for a Sun Fire 280R workstation. In Table 2, we compare our proposed approach with previous relevant works on logic soft error rate estimation [2, 22, 24, 25, 32]. From this table we can see

Table 2. Comparison of our work with other SER estimation methods.

Authors and Reference	Factors considered							
	LET Spectrum	Re-conv. Fanout	Sensitive Regions	SEU prob.	Vectors Applied	Location Altitude	Circuit Tech.	SET Degradation
Our work	yes	no	yes	yes	no	yes	yes	yes
Rao et al. [24]	yes	no	no	no	yes	yes	yes	yes
Rajaraman et al. [22]	no	no	no	no	yes	no	no	yes
Asadi-Tahoori [2]	no	no	no	yes	no	no	no	no
Zhang-Shanbhag [32]	yes	no	yes	yes	yes	yes	yes	no
Rejimon-Bhanja [25]	no	no	no	yes	yes	no	no	no

Table 3. Relevancy Comparison.

Measured Data (Altitude Unknown)		Estimated Logic Circuit SER (Ground Level)	
Devices	SER (FIT/Mbit)	Our Work (FIT)	Rao et al. [24] (FIT)
0.13μm SRAMs [7]	10,000 to 100,000		
SRAMs, 0.25μm and below [12]	10,000 to 100,000	1,000 to 20,000	1×10^{-5} to 8×10^{-5}
1 GBit memory in 0.25μm [21]	4,200		

that none of the existing logic SER estimation work has considered the re-convergent fanout, which may have a significant influence on the analysis. We will further discuss these factors in the next section.

5 Discussion of Results

From Table 2, the specification or experimental setup is compared. We can see, to accurate calculate logic SER, factors that influence logic SER estimation should be comprehensive considered. However, none of the existing analysis has considered all of them.

1. The physics of the SEU phenomena seems involved. For example, the analysis of the funneling and the angle of incidence are not considered. We take the energy of neutrons to be the main source that induces the SEU. However, in real cases, it is the physics of interaction between neutrons and silicon that produces the SEU. Simpler modeling and assumptions may influence the SER estimation accuracy.

2. The sensitive region of a transistor is defined as the channel region of an off nMOS transistor or the drain region of an off pMOS transistor. For a CMOS circuit, the "on" or "off" status of transistors is determined from inputs. In our approach, we statically assume that each circuit node's sensitive region is $10\mu m^2$. This may bias the SER results. Also, although we have considered the sensitive area of the circuit node, the strikes on pMOS or nMOS influence the polarity of SETs. So, the dynamic state of the circuit may further affect the SER.

3. Compared to the earth surface, the size of the sensitive region of a single transistor or a circuit board is trivially small and is getting smaller with the technology trend. At the surface of the earth we take the probability of a particle strike at a sensitive node simply by taking the ratio of the number of particles strikes/μm^2-s to strikes/m^2-s. Theoretically, it seems correct because note that 1 m^2 equals 10^{12} μm^2. To imagine this event in real cases, most probably there will be no strike on the sensitive regions but such low probability events can not be neglected. Once the SEU occurs, the circuit SER may easily be several orders of magnitude higher compared to the case of no strike at all. For example, a circuit may experience 1 SEU in 6 months (4320 hours), equals 231,480 FIT. It is also likely that the circuit has 0 SEU in these 6 months, so the measured SER is 0 FIT.

4. For logic circuits, fan-out details should be considered. In our experiment we only considered the worst case error rate for re-convergent fanouts. For example, if a re-convergent fanout has two paths, and one passes through more

gates compared to the other, our program only takes the path that has fewer gates because it is likely to give the worst SER. Timing and logic simulation may be needed for better accuracy [5]. In a real circuit, two situations can arise:

- When an SET goes through a large fan-out node the large load capacitance can eliminate the SET through node inertia.
- Or if the SET is not canceled by the fan-out node, it goes through multiple fan-out paths. If all paths have equal length, the SET might cancel itself at the merging point depending on path inversions. However, if paths have different lengths, one SET on the affected node can cause several propagating SETs to further increase the SER of the circuit.

The path delays may also influence logic SER.

5. It is highly recommended to have more field tests for logic circuits. Also, we suggest that the SER results from field tests for the same circuit, even in the same working environment, may be widely different at different times. Still, with field test data, the logic circuit SER results can be validated. A comparison with measurement may be the only way to determine which factors can be really neglected and which assumptions and approximations are justified.

6. None of these SER estimation approaches considered process variation effects on SER, which may also be a factor in the vulnerability to transient errors. It is reported that, intra-die process variation of threshold voltage may result in SER variation of 41% in a small circuit [23].

6 Conclusion

In this paper we have presented an environment-dependent soft error model for logic circuits based on error occurrence rate and the SET pulse width density. Our analysis requires logic signal probabilities. For any given set of input vectors or signal statistics, these may be obtained either from logic simulation or from static analysis of the circuit topology. For simplicity, we ignore correlations among reconverging signals. If those correlations were considered, some paths may not be activated. Temporal masking by clock sampling would further increase the masking. From our discussion, the logic SER may be highly sensitive to factors like sensitive region calibration, process variation and circuit characterization, making soft error estimation for logic circuits a complex problem. Comprehensive studies on them should provide better insights in the future.

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