J Electron Test (2015) 31:479–489
DOI 10.1007/s10836-015-5545-1

Defect Level Constrained Optimization of Analog and Radio Frequency Specification Tests

Suraj Sindia[1] · Vishwani D. Agrawal[2]

Received: 1 June 2015 / Accepted: 22 October 2015 / Published online: 7 November 2015
© Springer Science+Business Media New York 2015

Abstract The objective of this work is to minimize testing cost of analog and RF circuits for which complete specification tests are available. We use an integer linear program (ILP) to eliminate as many tests as possible without exceeding the required defect level. The method leverages correlation among specifications, thereby avoiding the tests for specifications that are sufficiently covered by tests for other specifications. First, Monte Carlo simulation determines probabilities for each test covering all other specifications it was not originally intended for. These probabilities and the given defect level then define an ILP model for eliminating unnecessary tests. An hypothetical example illustration of ten specifications demonstrates that depending on the defect level requirement up to half of the tests may be eliminated. Monte Carlo simulation using spice for probabilistic characterization of tests versus specifications followed by ILP optimization for two commercially available integrated circuits, an operational amplifier and a radio frequency power controller (RFPC), are presented as evidence of effectiveness of the technique.

Keywords Analog and mixed-signal testing · Defect-level · RF testing · Specification-based testing · Test optimization

Responsible Editor: L. M. Bolzani Pöhls

Work described here was performed while S. Sindia was with the Department of Electrical and Computer Engineering, Auburn University, Auburn, AL 36849, USA. Ideas in this research were first presented at the 15th IEEE Latin-American Test Workshop, Fortaleza, Brazil, March 12-15, 2014 [22].

✉ Vishwani D. Agrawal
vagrawal@eng.auburn.edu

Suraj Sindia
suraj.sindia@intel.com

[1] Intel Corporation, Hillsboro, OR 97124, USA

[2] ECE Department, Auburn University, Auburn, AL 36849, USA

1 Introduction

1.1 Test Cost and Defect Level

Testing an integrated circuit chip more than what is necessary adds to the cost of testing and, consequently, increases the total cost of shipping the chip. The amount of testing to be done on a chip should be based on the acceptable *defect level*. Defect level is the fraction of bad devices passing the test [6].

1.2 Rising Specification Test Cost of Analog Circuits

Classifying an analog, mixed-signal, or radio-frequency circuit as "good" or "bad" requires it to be tested against a set of specifications it was designed for. These specifications usually have a nominal value and an acceptable bound of a continuous range between minimum and maximum values. Tests, henceforth referred to as specification tests, often require expensive test instruments and complex test setups [5, 21] depending on specifications and the circuit being tested. At modern technology nodes, testing analog and RF circuits against all their specifications is becoming expensive and costs as much as manufacturing the integrated circuit as shown in the International Technology Roadmap for Semiconductors (ITRS) prediction of Fig. 1 [9].

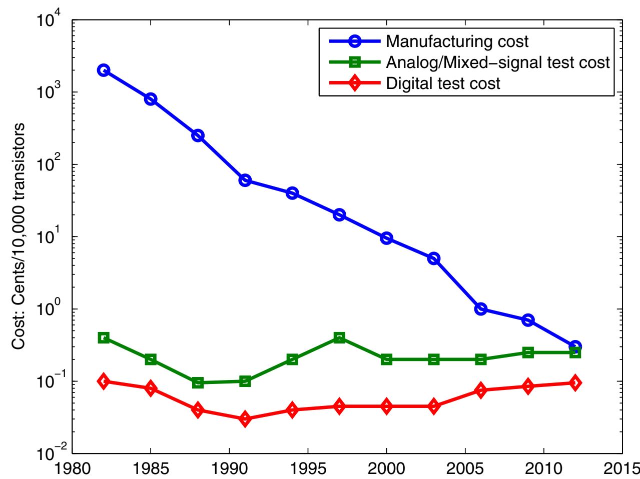

Fig. 1 Manufacturing cost per transistor has steadily declined over the years, whereas test cost per transistor has remained fairly steady over the years and is expected to remain so, catching up with manufacturing cost by 2015 or so per the ITRS prediction [9]

1.3 Prior Work

Specification test minimization for analog circuits is a well researched topic. We will briefly compare several existing methods with the ideas proposed in this paper. In one of the earliest studies of specification test minimization, Brockman and Director [4] use Monte Carlo method to arrive at a joint probability distribution between specifications and circuit process parameters. They then eliminate a subset of specifications that have correlation with the remaining specifications. Their process of eliminating redundant specifications must rely on combined knowledge of the designer and test engineer and hence significantly differs from the systematic integer linear programming (ILP) approach of the present work.

Selecting a subset of tests that sensitize parametric faults based on a structural fault model to reduce test time has been proposed [8, 17]. In contrast, we target specification tests directly and make no assumptions about faults or fault models considering that analog and radio-frequency circuits, in general, are designed to meet specifications and tested against those specifications. Moreover, fault models do not satisfactorily capture different specification violations leading to false-positives and false-negatives [10]. Past [18] and recent [24] studies have proposed signatures of circuit specifications that are easier and hence cheaper to measure than the specifications themselves. The proposed approach in this paper can be used to minimize the circuit specifications or their low-cost signatures as the ILP model remains agnostic to the specifications (or their signatures) used, giving further savings in addition to what is possible from low-cost signatures alone. Biswas et al. [2, 3] use boolean minimization to identify redundant tests from production test pass-fail data and achieve impressive test cost reduction. But that may not be useful in the test generation phase where we do not yet have the pass-fail data. More recent work [7, 13, 33] uses the inter-die (i.e., die on the same wafer) spatial correlation of analog specifications to minimize the number of measurements to be made on individual dice by predicting specifications based on measurements made on die in the neighborhood. The idea is based on correlations that exist among specification for any given die. As a result the proposed method can give cost savings in addition to what is possible using inter-die correlation.

1.4 Contributions of This Paper

This paper provides a framework to reduce the testing cost by compacting specification test set. In order to do this, we leverage the inherent correlation that exists among any pair of specifications of a circuit. These correlations allow us to define an integer linear program that minimizes the final test set while ensuring that the defect level does not exceed a desired threshold. The correlations among specifications of the circuit are estimated through Monte Carlo simulation, which is done off line and only once before the start of the actual manufacturing test.

The paper is organized as follows. Section 2 formally states the problem being solved. Section 3 elucidates the problem through a graphical representation. Section 4 formulates an integer linear program whose result will yield an optimized test set given a defect level threshold and cross-correlations among specification tests. The numerical example of Section 5 illustrates the methodology demonstrating the potential savings that can be achieved. Section 6 describes an operational amplifier circuit example for which cross correlation among specification tests is estimated through Monte Carlo simulation and an optimized test set is arrived at using the framework proposed in this paper. Section 7 is a case study of a radio frequency power controller (RFPC) specification test minimization using the proposed ILP. We conclude in Section 8.

2 Problem Statement

Consider a circuit under test (CUT) that has specifications $S_1, S_2, \cdots S_k$. A test T_i is used to check the correctness of specification S_i. We assume that these k tests are "perfect"; ith test will detect any out of range deviation of the ith specification. Such tests are often derived and used in practice because they guarantee a "zero" (assumed perfect) defect-level. Defect-level refers to test escapes or faulty devices passing test [6] and it is often measured in parts per million (PPM).

The specification-based test is very thorough (almost zero defect-level) but it can be very long. Typically, it requires long test time on the automatic test equipment (ATE), making the test expensive. A significant problem in the industry is to reduce the cost of testing without raising the defect level. In this work we propose an optimization solution.

In general, for k specifications the number of tests may or may not be exactly k. But, that does not affect the way the following analysis is done.

3 A Graph Representation

Figure 2 shows a bipartite graph [1] with two sets of vertices representing tests and specifications, respectively. In the graph an edge label p_{ij} represents the probability of test T_i testing for specification S_j. In general, the test T_i is designed to test for specification S_i. Therefore, we assume $p_{ii} = 1.0$ for all i. For edges for which $i \neq j$ we find the probabilities p_{ij} by Monte Carlo simulation as described in Section 6. Note that, in general, $p_{ij} \neq p_{ji}$. Also, a specification may be testable only by a subset of tests. That accounts for the missing edges in the graph for which the label $p_{ij} = 0$.

4 An Integer Linear Program (ILP)

We define a [0,1] integer variable x_i for each test T_i. We will formulate an integer linear program (ILP) to determine the values $\{x_i\}$ such that if $x_i = 1$, test T_i will be retained and if $x_i = 0$, T_i will be discarded. Thus, the objective function for the ILP is,

$$\text{minimize} \sum_{i=1}^{k} x_i \tag{1}$$

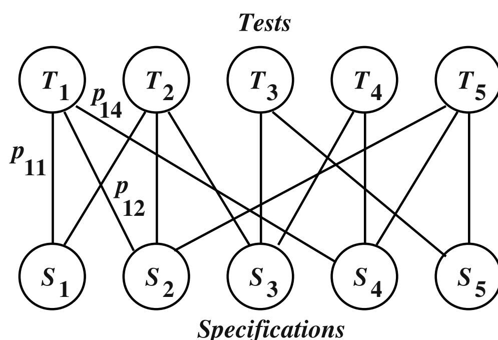

Fig. 2 Bipartite graph [1] of tests $\{T_i\}$ and specifications $\{S_i\}$ of a circuit under test (CUT). The edge label p_{ij} is the probability of testing specification S_j by test T_i

Next, we derive a set of linear constraints. Suppose, we wish the defect-level not to exceed a given value dl. Let, $P(S_j)$ be the probability of fully testing (covering) the specification S_j. Then,

$$1 - \prod_{j=1}^{k} P(S_j) \leq dl \tag{2}$$

If we assign equal significance to all specifications, then each specification should identically contribute to the defect-level. Thus,

$$(1 - dl)^{1/k} \leq P(S_j), \forall j \tag{3}$$

This can also be expressed as,

$$1 - P(S_j) \leq 1 - (1 - dl)^{1/k}, \forall j \tag{4}$$

Since any specification j may be covered by multiple tests, we determine its coverage probability as,

$$P(S_j) = 1 - \prod_{i=1}^{k} (1 - p_{ij})^{x_i} \tag{5}$$

When $x_i = 1$, i.e., test T_i is retained, it contributes a factor $(1 - p_{ij})$ to the product in Eq. 5, and when $x_i = 0$, i.e., T_i is discarded, it contributes 1 to the product. We can also write,

$$\ln[1 - P(S_j)] = \sum_{i=1}^{k} x_i \ln(1 - p_{ij}) \tag{6}$$

From Eqs. 4 and 6, we get the linear constraints for the ILP:

$$\sum_{i=1}^{k} x_i \ln(1 - p_{ij}) \leq \ln[1 - (1 - dl)^{1/k}], \; j = 1, \; 2, \cdots k \tag{7}$$

5 A Hypothetical Example

Consider ten specifications, $S_1, \cdots S_{10}$, and their respective tests, $T_1, \cdots T_{10}$. Probabilities of each test covering various specifications are summarized in Table 1. We have skewed the test coverage probabilities to demonstrate the compaction of tests as the defect level is varied, but such high cross correlation in analog circuit specification tests is not uncommon and has been reported in the literature [12]. For an illustration, we assume a defect level 1,000 parts per million (PPM), i.e., $dl = 10^{-3}$.

For minimizing the tests we use the ILP formulation of Section 4. The objective function (1) is:

$$\text{minimize} \sum_{i=1}^{10} x_i, \tag{8}$$

where, $\{x_i\} = integer[0, 1]$, $1 \leq i \leq 10$, subject to a set of constraints given by Eq. 7. Right hand side of inequality (7)

Table 1 Test coverage probabilities (p_{ij}) in a hypothetical example with 10 specifications and 10 tests

Specification	p_{ij} values for tests									
	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9	T_{10}
S_1	1.00	0.97	0.94	0.91	0.88	0.85	0.82	0.79	0.76	0.73
S_2	0.73	1.00	0.97	0.94	0.91	0.88	0.85	0.82	0.79	0.76
S_3	0.76	0.73	1.00	0.97	0.94	0.91	0.88	0.85	0.82	0.79
S_4	0.79	0.76	0.73	1.00	0.97	0.94	0.91	0.88	0.85	0.82
S_5	0.82	0.79	0.76	0.73	1.00	0.97	0.94	0.91	0.88	0.85
S_6	0.85	0.82	0.79	0.76	0.73	1.00	0.27	0.26	0.17	0.03
S_7	0.88	0.85	0.82	0.79	0.76	0.15	1.00	0.36	0.30	0.04
S_8	0.91	0.88	0.85	0.82	0.79	0.02	0.41	1.00	0.37	0.04
S_9	0.94	0.91	0.88	0.85	0.82	0.25	0.17	0.39	1.00	0.40
S_{10}	0.97	0.94	0.91	0.88	0.85	0.38	0.15	0.14	0.06	1.00

is evaluated as, $\ln[1 - (1 - 10^{-3})^{1/10}] = -9.21$. To avoid $\ln 0 = -\infty$ coefficients on the left hand side, we approximate probabilities like $p_{ii} = 1.0 \approx 1 - 10^{-15}$. Therefore, the corresponding coefficients evaluate to $\ln(10^{-15}) = -34.54$. The ten constraints are:

$-34.54x_1 - 3.51x_2 - 2.81x_3 - 2.41x_4 - 2.12x_5 - 1.90x_6 - 1.71x_7 - 1.56x_8 - 1.43x_9 - 1.31x_{10} \leq -9.21$,
$-1.31x_1 - 34.54x_2 - 3.51x_3 - 2.81x_4 - 2.41x_5 - 2.12x_6 - 1.90x_7 - 1.71x_8 - 1.56x_9 - 1.43x_{10} \leq -9.21$,
$-1.43x_1 - 1.31x_2 - 34.54x_3 - 3.51x_4 - 2.81x_5 - 2.41x_6 - 2.12x_7 - 1.90x_8 - 1.71x_9 - 1.56x_{10} \leq -9.21$,
$-1.56x_1 - 1.43x_2 - 1.31x_3 - 34.54x_4 - 3.51x_5 - 2.81x_6 - 2.41x_7 - 2.12x_8 - 1.90x_9 - 1.71x_{10} \leq -9.21$,
$-1.71x_1 - 1.56x_2 - 1.43x_3 - 1.31x_4 - 34.54x_5 - 3.51x_6 - 2.81x_7 - 2.41x_8 - 2.12x_9 - 1.90x_{10} \leq -9.21$,
$-1.90x_1 - 1.71x_2 - 1.56x_3 - 1.43x_4 - 1.31x_5 - 34.54x_6 - 0.31x_7 - 0.30x_8 - 0.19x_9 - 0.03x_{10} \leq -9.21$,
$-2.12x_1 - 1.90x_2 - 1.71x_3 - 1.56x_4 - 1.43x_5 - 0.16x_6 - 34.54x_7 - 0.45x_8 - 0.36x_9 - 0.04x_{10} \leq -9.21$,
$-2.41x_1 - 2.12x_2 - 1.90x_3 - 1.71x_4 - 1.56x_5 - 0.02x_6 - 0.53x_7 - 34.54x_8 - 0.46x_9 - 0.04x_{10} \leq -9.21$,
$-2.81x_1 - 2.41x_2 - 2.12x_3 - 1.90x_4 - 1.71x_5 - 0.29x_6 - 0.19x_7 - 0.49x_8 - 34.54x_9 - 0.51x_{10} \leq -9.21$,
$-3.51x_1 - 2.81x_2 - 2.41x_3 - 2.12x_4 - 1.90x_5 - 0.48x_6 - 0.16x_7 - 0.15x_8 - 0.06x_9 - 34.54x_{10} \leq -9.21$.

Solving this by an open source ILP solver [14] results in a minimized test set of only *six* tests by eliminating T_1, T_2, T_3 and T_5 from the original test set of ten tests, T_1 through T_{10}.

Table 2 summarizes the optimized tests for various defect levels in the range 1 PPM through 10,000 PPM using the ILP formulation of Section 4 for the test coverage probabilities given in Table 1. As can be seen in the table, test size reduction of 40 % is achieved at a defect level of 1,000 PPM, which is a typical test escape accepted in custom analog circuits in deep sub-micron technology nodes such as 180nm or lower [3]. As one would expect, the test set size reduction varies directly as the defect level is allowed to increase. For example 20 % reduction at $dl = 10$ PPM, whereas it is 50 % at $dl = 10,000$ PPM. The potential test reduction could be higher if there is stronger cross-correlation between circuit specifications, or if a higher defect level can be tolerated, or both.

In Table 2 we notice that even for 1 PPM, which represents a very high quality level, two tests have been eliminated. This is quite a normal occurrence considering the fact that each test may have originally targeted a

Table 2 ILP optimization in 10-test hypothetical example

Defect level	ILP result: $x_i = 1$, T_i selected, else discarded										Number of	Test size
dl in PPM	x_1	x_2	x_3	x_4	x_5	x_6	x_7	x_8	x_9	x_{10}	selected tests	reduction (%)
1	1	0	1	1	0	1	1	1	1	1	8	20
10	0	1	0	1	0	1	1	1	1	1	7	30
100	1	1	0	0	0	1	1	1	1	1	7	30
1,000	1	0	0	0	0	1	1	1	1	1	6	40
10,000	1	1	1	1	1	0	0	0	0	0	5	50

separate specification. Case studies discussed next support this observation.

6 Case Study I: Operational Amplifier

In order to obtain realistic values of test coverage probabilities for specifications of a given analog circuit, we use Monte Carlo simulation by *spice* program with integrated circuit emphasis [26]. We intend to demonstrate the test minimization procedure illustrated in Section 5 on a commercially available operational amplifier tested across seven specifications, namely:

- S_1: DC gain
- S_2: Slew rate
- S_3: 3-dB bandwidth
- S_4: Input referred offset voltage
- S_5: Power supply rejection ratio
- S_6: Common mode rejection ratio
- S_7: Input bias current

6.1 Circuit Details

The Texas Instruments (TI) LM741 operational amplifier circuit is shown in Fig. 3 with nominal values of components. This is a simplified schematic as provided in the data-sheet [27]. The circuit has 22 active devices (bipolar junction transistors or BJT), 12 resistors, and one capacitor. Five thousand instances of the circuit are created by sampling passive component (resistor and capacitor) values from normal distributions, with the mean for each component set to its nominal value (shown alongside the component in Fig. 3) and standard deviation set to 5 % of the mean. For active components (NPN and PNP BJT), β or dc current gain is sampled from a normal distribution with mean set to the nominal value of 625 and standard deviation set to 62.5, i.e., 10 % of the mean. All other parameters of the BJT are left unchanged at their nominal values specified in the model file [28].

6.2 Calculating p_{ij}

Table 3 lists the minimum, nominal, and maximum values of specifications S_1 through S_7 as given in the TI LM 741 datasheet [27]. A circuit instance is considered to "fail" a given specification if the simulated value for that circuit instance lies outside the minimum-maximum range. Note that some specifications are "single-ended," that is, they may not have either a minimum or a maximum bound. In such a cases, a circuit instance would be labeled as "fail" if it lies outside the "single-ended" range.

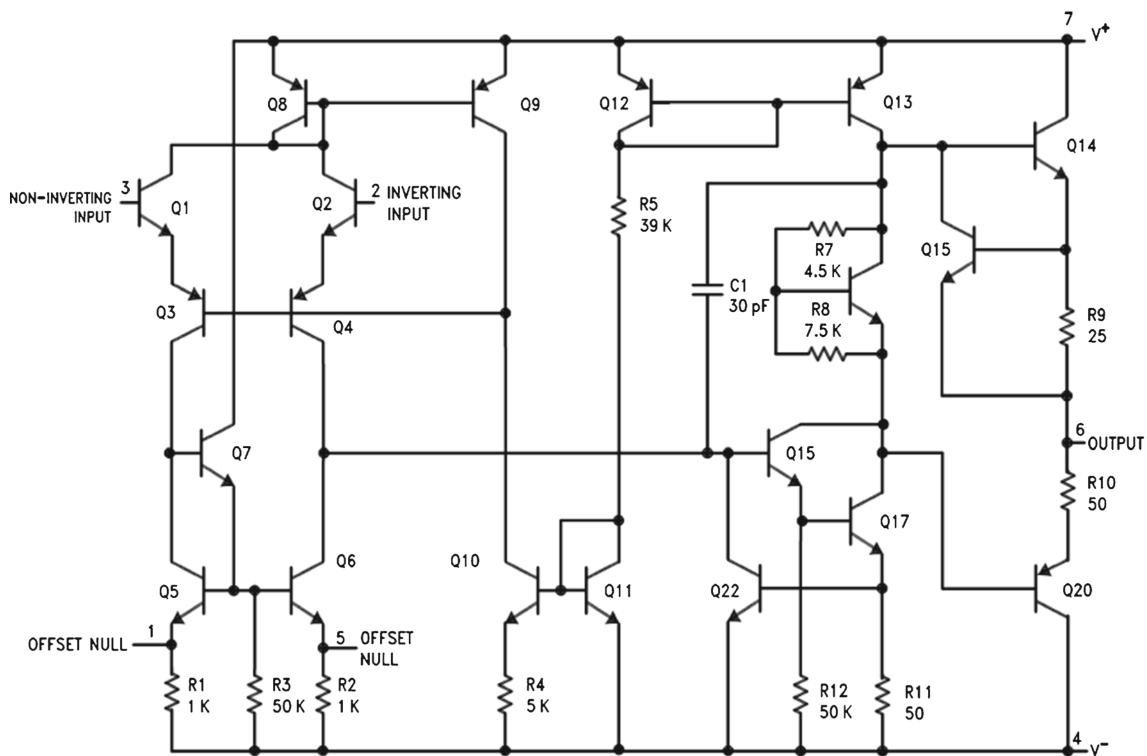

Fig. 3 Circuit schematic of operational amplifier LM741 [27] with nominal values of the components. This is the circuit example used for estimating correlation among specifications through Monte Carlo simulation

Table 3 Operational amplifier specifications from LM 741 data-sheet [27] used in case study I

Specification		Values			Unit
Label	Description	Minimum	Nominal	Maximum	
S_1	Dc gain	50	200		V/mV
S_2	Slew rate	0.3	0.5		V/μs
S_3	3-dB bandwidth	0.4	1.5		MHz
S_4	Input referred offset voltage		± 10	± 15	mV
S_5	Power supply rejection ratio	86	96		dB
S_6	Common mode rejection ratio	80	95		dB
S_7	Input bias current		30	80	nA

We calculate the conditional test coverage of specification S_j by S_i or, in other words, the likelihood of test T_i for S_i covering S_j, as follows:

$$p_{ij} = \frac{\text{Number of instances failing both } S_i \text{ and } S_j}{\text{Number of instances failing } S_j} \tag{9}$$

For LM 741 operational amplifier circuit of Fig. 3 all seven specifications S_1 through S_7 for the 5,000 circuit instances, generated as described in Section 6.1, are first measured from simulation. Next, the conditional test coverage between all pairs of specifications is obtained using Eq. 9. For example, out of the 5,000 circuit instances S_1 is violated in 45 circuit instances while S_2 is violated in 81 instances as shown in the graph of Fig. 4. Seventeen circuit instances fail both S_1 and S_2 (labeled on the edge between nodes S_1 and S_2 in the graph.) This gives probability p_{12}, which is the probability of test for specification S_1 (i.e., T_1) covering specification S_2 as $p_{12} = \frac{17}{81} = 0.21$. Similarly, p_{21}, which is the probability of test for specification S_2 (i.e., T_2) covering specification S_1 is $p_{21} = \frac{17}{45} = 0.38$. Values of p_{ij} for the LM 741 circuit across all seven specifications are listed in Table 4, where for the sake of clarity T_i is used as column header to signify the test for specification S_i.

6.3 ILP Solution

Choosing a desired defect level dl anywhere in the range 1 to 100 PPM, the ILP reduces the number of specifications to be tested by one, from 7 to 6, by eliminating test T_4 for specification S_4. It is also intuitively clear why this may

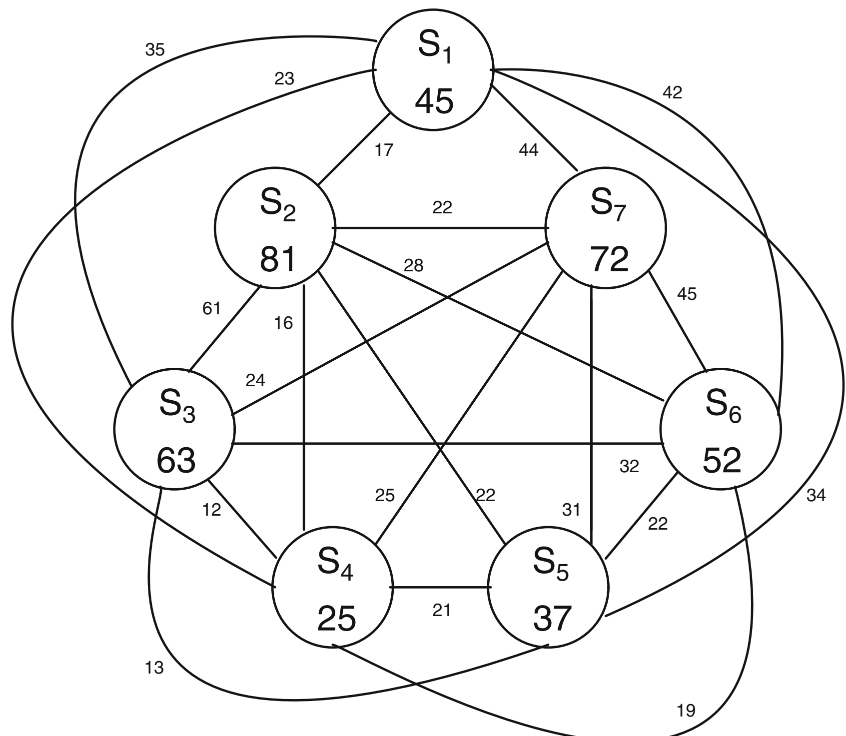

Fig. 4 A graph depicting the number of circuit instances failing each specification (noted inside the node) and the number of circuit instances failing both specifications (noted on the edges)

Table 4 Probabilities p_{ij} for Opamp LM 741 example

Specification	p_{ij} values for tests						
	T_1	T_2	T_3	T_4	T_5	T_6	T_7
S_1	1.00	0.38	0.78	0.51	0.76	0.93	0.98
S_2	0.21	1.00	0.75	0.20	0.27	0.35	0.27
S_3	0.56	0.97	1.00	0.19	0.21	0.51	0.38
S_4	0.92	0.64	0.48	1.00	0.84	0.76	1.00
S_5	0.92	0.59	0.35	0.57	1.00	0.59	0.84
S_6	0.81	0.54	0.62	0.37	0.42	1.00	0.87
S_7	0.61	0.31	0.33	0.35	0.43	0.62	1.00

be so from Table 4 as test T_7 covers S_4 with probability 1. Upon relaxing defect level, dl, further to 1,000 PPM, the number of specifications to be tested is reduced by one more specification as test T_1 for specification S_1 is eliminated, thereby giving a compacted set of 5 tests. Defect level 10,000 PPM allows elimination of T_3 leaving only four tests. Further test compaction could be possible by varying the minimum/maximum thresholds used for the specifications. This line of research is currently being pursued.

7 Case Study II: RF Power Controller

We now apply the ILP based test minimization procedure to a commercially available RF power controller (RFPC) circuit, LTC 4400 from Linear Technology [15].

7.1 Circuit Description and Specifications of RFPC

This circuit controls the gain of RF power amplifier and is a critical component in the up-link signal chain of an RF transceiver. Functional diagram of LTC 4400 used in a typical up-link signal chain is shown in Fig. 5. The RFPC supplies a control voltage to the RF power amplifier based on frequency of transmission and the desired gain at that frequency. RFPC has two inputs as shown in Fig. 5: 1) input RF monitors the output of the antenna through a feedback network, and 2) input PCTL provides a control signal that traces the desired power amplifier gain. The only output of RFPC, V_{PCA}, drives the control signal of the power amplifier. The small signal equivalent circuit of the LTC 4400 is shown in Fig. 6. It should be pointed out that there are three more physical pins in a common variant of the LTC 4400 chip. These include V_{CC} for power, GND and a control pin (SHDN, not shown in the functional diagram of Fig. 5) for putting the device in a sleep mode.

Important specifications of an RFPC include slew rate, bandwidth, and drive current of the output, V_{PCA}, and the RF input resistance. Specifications of LTC 4400, the RFPC considered in this case study, are shown in Table 5. The minimum, nominal and maximum values of each specification (if available) are taken from the LTC 4400 data-sheet [15].

7.2 Calculating p_{ij} Matrix for RFPC

We resort to Monte Carlo simulations for computing the probabilities, p_{ij}, as described in [22] and similar to [25]. However, in this work we have not used any speed-up over conventional Monte Carlo approach as proposed in [25]. Ten thousand instances of the small signal equivalent circuit

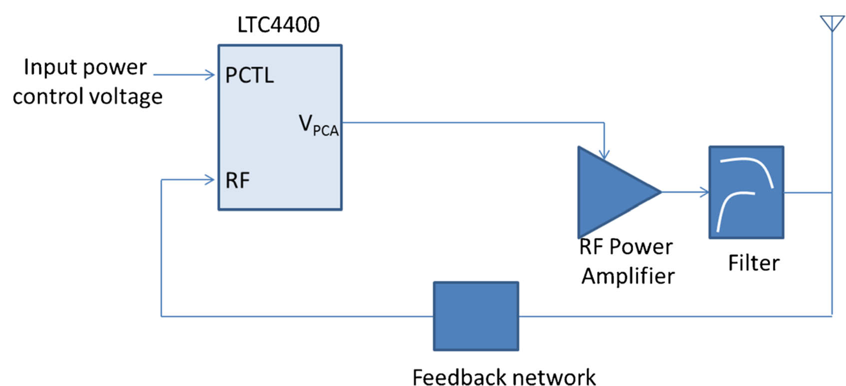

Fig. 5 Functional diagram of RF power controller as used in the up-link of a typical RF transceiver. Notice that the RFPC provides the power amplifier with the necessary control voltage to control its gain

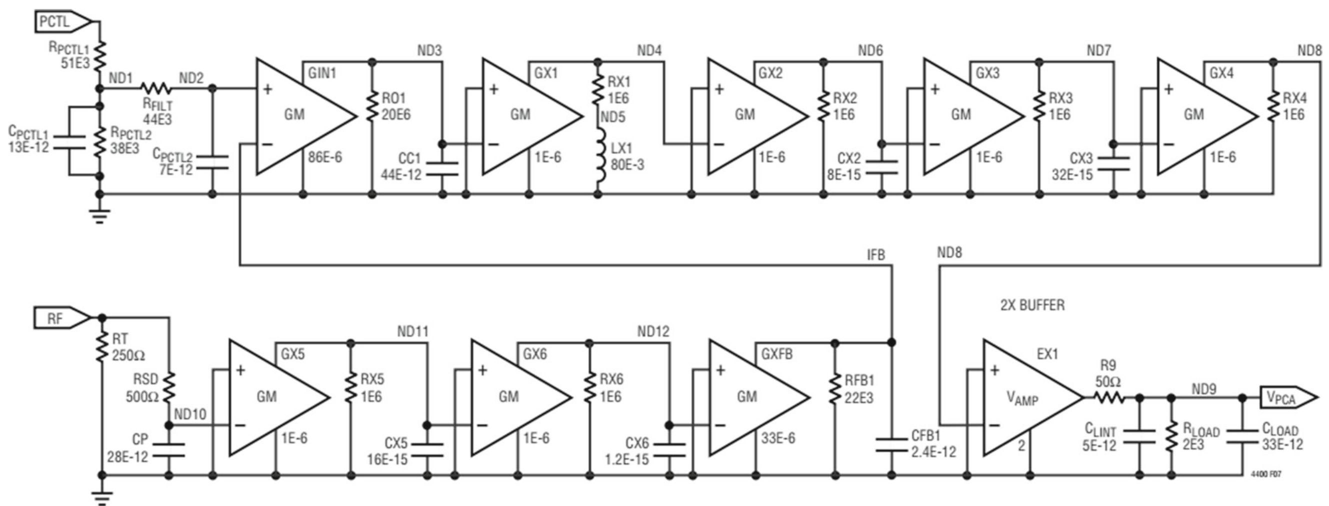

Fig. 6 Small signal equivalent circuit schematic of radio frequency power controller LTC4400, reproduced from data-sheet [15], showing nominal values of components

of LTC 4400 are created. The component values for circuit instances are sampled as follows:

- Inductor, resistor and capacitor values are random samples from a normal distribution with mean as the nominal value noted on the corresponding component in Fig. 6 and standard deviation as 15 % of the nominal value. These values for absolute variation are typical for passive components such as diffusion-based polycrystalline-resistors [16], metal-oxide-metal (MOM) capacitors [29], and high metal layer inductors [19] that are normally used in integrated circuits [11, 31, 32].
- Transconductance, GM, and voltage gain, V_{AMP}, are sampled from a normal distribution with mean as nominal value noted on the corresponding element in Fig. 6 and standard deviation as 20 % of the nominal value [11, 20, 31, 32].

Inaccuracies in Monte Carlo simulations result from two sources 1) small number of samples used for sampling the distribution of an input parameters, and, 2) periodicity bias of the pseudo random number generator used to generate samples. To eliminate the first source of inaccuracy, we use 10,000 samples in the Monte Carlo simulation so that the standard error in the sample mean is less than 5 % for each of the input parameters. To eliminate the second source of inaccuracy, we rely on a pseudo-random number generator, with a return period of 2^{1492}, which is much greater than the number of samples (10,000) generated for the simulation.

Table 5 RF Power Controller specifications from LTC4400 data-sheet [15] used in case study II

Specification		Values			Unit
Label		Minimum	Nominal	Maximum	
S_1	Shutdown current		10	20	μA
S_2	Operating current		1.2	1.9	mA
S_3	V_{PCA} bandwidth	350	450	560	kHz
S_4	V_{PCA} slew rate	1.8	2.5	3	V/μs
S_5	V_{PCA} start voltage	270	450	550	mV
S_6	V_{PCA} output current	7	10		mA
S_7	PCTL input resistance	60	90	120	kΩ
S_8	RF inputresistance	150	250	350	Ω
S_9	PCTL referenced output voltage (@RF_{in}=-10dBm)	40	50	60	mV
S_{10}	PCTL referenced output voltage (@RF_{in}=-6dBm)	90	100	110	mV
S_{11}	PCTL referenced output voltage (@RF_{in}=6dBm)	375	400	425	mV
S_{12}	PCTLreferenced output voltage (@RF_{in}=10dBm)	650	700	750	mV

Table 6 Probabilities p_{ij} for RF power controller LTC 4400

Specification	p_{ij} values for tests T_1 through T_{12}											
	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9	T_{10}	T_{11}	T_{12}
S_1	1.00	0.55	0.66	0.50	0.50	0.94	0.80	0.63	0.46	0.63	0.68	0.73
S_2	0.45	1.00	0.65	0.58	0.73	0.92	0.45	0.80	0.85	0.76	0.62	0.77
S_3	0.91	0.46	1.00	0.61	0.76	0.63	0.50	0.81	0.78	0.85	0.91	0.54
S_4	0.50	0.52	0.55	1.00	0.75	0.89	0.85	0.77	0.84	0.66	0.67	0.46
S_5	0.77	0.57	0.62	0.54	1.00	0.65	0.53	0.65	0.86	0.69	0.75	0.46
S_6	0.69	0.79	0.62	0.46	0.49	1.00	0.86	0.89	0.46	0.59	0.48	0.70
S_7	0.55	0.47	0.59	0.76	0.80	0.56	1.00	0.52	0.78	0.94	0.71	0.50
S_8	0.93	0.93	0.76	0.49	0.46	0.81	0.93	1.00	0.58	0.95	0.46	0.73
S_9	0.64	0.56	0.78	0.77	0.60	0.55	0.72	0.72	1.00	0.78	0.50	0.63
S_{10}	0.92	0.66	0.56	0.49	0.66	0.84	0.81	0.83	0.53	1.00	0.76	0.65
S_{11}	0.83	0.91	0.56	0.51	0.69	0.49	0.86	0.62	0.69	0.76	1.00	0.71
S_{12}	0.57	0.75	0.93	0.47	0.67	0.81	0.48	0.80	0.51	0.56	0.61	1.00

Table 7 Summary of ILP based optimization of specification tests of LTC 4400

Defect level	ILP result: $x_i = 1$, T_i selected, else discarded												Number of	Test size
dl in PPM	x_1	x_2	x_3	x_4	x_5	x_6	x_7	x_8	x_9	x_{10}	x_{11}	x_{12}	selected tests	reduction (%)
1	1	1	1	1	1	1	1	1	1	0	1	1	11	8.3
10	1	1	1	1	1	1	1	1	0	0	1	1	10	16.6
100	1	1	1	1	1	1	0	1	0	1	0	1	9	25.0
250	1	1	1	1	1	1	0	0	0	1	0	1	8	33.3
500	1	1	0	1	0	1	0	0	1	1	0	1	7	41.67
700	1	1	0	1	0	0	1	0	0	1	0	1	6	50.0
1,000	1	1	0	0	0	1	0	0	0	1	0	1	5	58.3

As a result, we expect no bias due to periodicity in sampling the input parameters.

To compute p_{ij}, we consider twelve specifications S_1 through S_{12} listed in Table 5 and their dedicated tests T_1 through T_{12}. These tests are outlined in the LTC 4400 datasheet [15]. We use Eq. 9 to compute p_{ij} entries of Table 6. For example, 455 circuit instants failed test T_8. Of these 455 circuits, 287 circuits also failed test T_1 for specification S_1, thereby giving $\frac{287}{455} = 0.63$ as the eighth entry in the first row. It can be seen that the overall correlation among tests for various specifications is fairly high, majority of the entries being above 0.5, and one can expect significant reduction in tests.

7.3 ILP Solution

We constrained the defect level to seven different values starting from 1 PPM through 1,000 PPM, minimizing the tests at each of these defect level thresholds. We list the corresponding optimized test set in Table 7. The column on the extreme right shows the percentage reduction in test set size relative to the original test set size of 12. Figure 7 shows a plot of percentage reduction in test set size versus defect

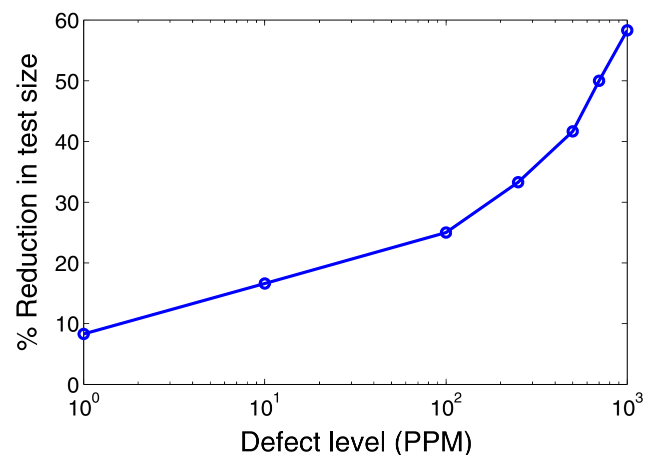

Fig. 7 Plot of percentage reduction in test set size versus defect level for the RFPC LTC 4400

level. As seen here, even for a conservative defect level of 100 PPM, a 25 % reduction in test size is achieved. Relaxing the defect level constraint to 1,000 PPM allows test set reduction by 58 %.

8 Conclusion

Considering that there is a pressing need to reduce testing costs of analog, RF and mixed signal circuits we have shown how to leverage the cross-correlations among circuit specifications and tests. An integer linear program optimally minimizes the test set while ensuring that the quality of the tested circuit does not degrade below a given defect level threshold. An illustrative example shows test size reduction of 40 % at defect level of 1,000 PPM. Even more test reduction is possible if there is better correlation among circuit specifications, or if a higher defect level can be tolerated. Test reduction by 30 % and 58 % for a commercially available opamp (LM 741) and an RF power controller (LTC 4400), respectively, at a defect level of 1,000 PPM are obtained by the ILP approach, making it viable for real-world analog and RF circuits.

In Section 4, the objective function of Eq. 1 gives equal weight to all tests. In reality, however, different tests may have different complexities and they may require different application times. The test application time of test T_i can be used as a weight factor w_i to redefine the objective function as,

$$\text{minimize} \sum_{i=1}^{k} w_i x_i \tag{10}$$

While deriving (3) we made a simplifying assumption that each of the k specifications was equally significant. We thus distributed the defect level (dl) equally over all specifications, which allowed us to derive the linear constraints of Eq.7. Lifting this assumption, i.e., treating some specifications as more critical (or expensive) than others, will require reformulation of the ILP model. Cost asymmetry in specification tests as described in [23] could be used for guiding such an ILP model formulation.

Improving the efficiency of compute-intensive Monte Carlo simulation and meaningful modeling of parameter variations are problems to be explored. We are investigating the application of recently published techniques [25].

Any test minimization that preserves the defect level can, in general, reduce the diagnostic capability of tests. In high-volume production testing, test time reduction is usually a priority. In characterization testing, such as during the initial yield ramp up, diagnosis is important. An alternative criterion for test optimization might be to preserve or maximize the diagnostic resolution instead of defect level. Our future research will focus on diagnostic tests as well. The ILP formulation described in this paper can also be used for minimizing alternate tests [30] for a given circuit, much like minimizing conventional specification tests demonstrated here.

Another application of the defect level preserving test minimization method is in generation of tests. New tests may be generated to cover multiple specifications. New tests may also be supplied by users after a device has been in production. Once such tests are inserted in the minimization procedure, further reductions are possible.

Acknowledgments The authors thank Dr. R. A. Parekhji for suggesting the problem of specification based test minimization and for his interest in this work. This research is supported in part by the National Science Foundation Grants CNS-0708962, CCF-1116213 and IIP-0738088.

References

1. Asratian AS, Denley TMJ, Häggkvist R (1998) Bipartite graphs and their applications. Cambridge University Press. Tracts in Mathematics 131
2. Biswas S, Blanton RD (2008) Test compaction for mixed-signal circuits using pass-fail test data. In: Proc. 26th IEEE VLSI Test Symposium, 299–308
3. Biswas S, Li P, Blanton RD, Pileggi LT (2005) Specification test compaction for analog circuits and MEMS [Accelerometer and Opamp Examples]. In: Proc. IEEE Design, Automation and Test in Europe, 164–169
4. Brockman JB, Director SW (1989) Predictive subset testing: Optimizing IC parametric performance testing for quality, cost, and yield. IEEE Trans Semicond Manuf 2(3):104–113
5. Burns M, Roberts G (2000) Introduction to Mixed-Signal IC Test and Measurement. Oxford University Press, New York
6. Bushnell ML, Agrawal VD (2000) Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits. Springer, Boston
7. Chang H.-M, Cheng K-T, Zhang W, Li X, Butler KM (2011) Test cost reduction through performance prediction using virtual probe. In: Proc. International Test Conference, 1–9. Paper 1.3
8. Devarayanadurg G, Soma M, Goteti P, Huynh SD (1999) Test set selection for structural faults in analog IC. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 18(7):1026–1039
9. International Technology Roadmap for Semiconductors (ITRS) 2009 (2015) http://bit.ly/1cCvuY3
10. Kaminska B (1999) Is analog fault simulation a key to product quality? practical considerations. In: Proc. International Test Conference, 648–648
11. Kuhn KJ (2010) CMOS transistor scaling past 32nm and implications on variation
12. Kupp N, Drineas P, Slamani M, Makris Y (2008) Confidence estimation in Non-RF to RF correlation-based specification test compaction. In: Proc. IEEE European Test Symposium, 35–40
13. Kupp N, Huang K, Carulli JM, Makris Y (2012) Spatial correlation modeling for probe test cost reduction in RF devices. In: Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 23–29
14. LP Solve (2015) http://sourceforge.net/projects/lpsolve/

15. LTC 4400 Datasheet – RF Power Controllers with 450kHz Loop BW and 45dB Dynamic Range (2015) Linear Technology, http://cds.linear.com/docs/en/datasheet/4400fas.pdf
16. Lu N. C-C, Gerzberg L, Lu C-Y, Meindl JD (1981) Modeling and optimization of monolithic polycrystalline silicon resistors. IEEE Trans on Electron Devices 28(7):818–830
17. Milor L, Sangiovanni-Vincentelli AL (1994) Minimizing production test time to detect faults in analog circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 13(6):796–813
18. Nagi N, Chatterjee A, Yoon H, Abraham JA (1998) Signature analysis for analog and mixed-signal circuit test response compaction. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 17(6):540–546
19. Niknejad AM, Meyer RG (1997) Analysis and Optimization of Monolithic Inductors and Transformers for RF ICs. In: Proc. IEEE Custom Integrated Circuits Conference, 375–378
20. Razavi B (1999) CMOS technology characterization for analog and RF design. IEEE Journal of Solid-State Circuits 34(3):268–276
21. Schaub KB, Kelly J (2004) Production testing of RF and system-on-a-chip devices for wireless communications. Boston: Artech House
22. Sindia S, Agrawal VD (2014) Specification test minimization for given defect level. In: Proc. IEEE Latin American Test Workshop, 1–6
23. Stratigopoulos H, Drineas P, Slamani M, Makris Y (2010) RF specification test compaction using learning machines. IEEE Trans on Very Large Scale Integration (VLSI) Systems 18(6):998–1002
24. Stratigopoulos H-G, Drineas P, Slamani M, Makris Y (2007) Non-RF to RF test correlation using learning machines: A case study. In: Proc. 25th IEEE VLSI Test Symposium, 9–14
25. Stratogopoulos H-G, Sunter S (2014) Efficient monte Carlo-based analog parametric fault modelling. In: Proc. 32nd IEEE VLSI Test Symposium, 1–6
26. The Spice Page (2015) http://bit.ly/1b72tyv
27. TI LM 741 Datasheet (2015) http://www.ti.com/lit/ds/symlink/lm741.pdf
28. TI LM 741 SPICE model (2015) http://www.ti.com/lit/zip/snom211
29. Tuinhout HP, Elzinga H, Brugman JTH, Postma F (1995) Accurate Capacitor Matching Measurements using Floating Gate Test Structures. In: Proc. International Conference on Microelectronic Test Structures, 133–137
30. Variyam PN, Cherubal S, Chatterjee A (2002) Prediction of analog performance parameters using fast transient testing. IEEE Trans Computer-Aided Design of Integrated Circuits and Systems 21(3):349–361
31. Yelten MB, Franzon PD, Steer MB (2011) Surrogate-model-based analysis of analog circuits – Part I: Variability analysis. IEEE Transactions on Device and Materials Reliability 11(3):458–465
32. Yelten MB, Natarajan S, Xue B, Goteti P (2013) Scalable and efficient analog parametric fault identification. In: Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 387–392
33. Zhang W, Li X, Liu F, Acar E, Rutenbar RA, Blanton RD (2011) Virtual probe: A statistical framework for low-cost silicon characterization of nanoscale integrated circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 30(12):1814–1827

Suraj Sindia is a Quality and Reliability R&D Engineer at Intel Corporation, Hillsboro, Oregon, USA. He received his PhD degree from Auburn University, Auburn, Alabama, USA in 2013 and a Master?s degree in Electronic Systems Design from the Indian Institute of Science, Bangalore, India in 2009. From 2009-2010 he worked as a design engineer at Analog Devices Inc., Bangalore, India, on precision digital to analog converters, and in spring of 2013 as a research intern at Intel Corporation, Hillsboro, Oregon on radio frequency test development. His research interests are in low cost test methods, reliability, and fault-tolerance with a focus on radio frequency, analog, and mixed-signal integrated circuits. He is a member of the IEEE.

Vishwani D. Agrawal is James J. Danaher Professor of Electrical and Computer Engineering at Auburn University, Alabama, USA. He has over forty years of industry and university experience, working at Bell Labs, Murray Hill, NJ, USA; Rutgers University, New Brunswick, NJ, USA; TRW, Redondo Beach, CA, USA; IIT, Delhi, India; EG&G, Albuquerque, NM, USA; and ATI, Champaign, IL, USA. His areas of expertise include VLSI testing, low-power design, and microwave antennas. He obtained his BE degree from the Indian Institute of Technology Roorkee, Roorkee, India, in 1964; ME degree from the Indian Institute of Science, Bangalore, India, in 1966; and PhD degree in electrical engineering from the University of Illinois at Urbana-Champaign, in 1971. He has published over 350 papers, has coauthored five books and holds thirteen United States patents. He is the Editor-in-Chief of the Journal of Electronic Testing: Theory and Applications, and a past Editor-in-Chief (1985-87) of the IEEE Design & Test of Computers magazine. He was the Keynote Speaker at the 25th International Conference on VLSI Design, Hyderabad, India, 2012, Keynote Speaker at the Ninth Asian Test Symposium, Taipei, Taiwan, 2000, and an invited Plenary Speaker at the 1998 International Test Conference, Washington, D.C., USA. He served on the Board of Governors (1989-90) of the IEEE Computer Society, and in 1994 chaired the Fellow Selection Committee of that Society. He has received eight Best Paper Awards and several other awards including two Lifetime Achievement Awards, and the 2014 James Monzel Award from the IEEE North Atlantic Test Workshop. Agrawal is a Fellow of the ACM, IEEE and IETE-India. He has served on the Advisory Boards of the ECE Departments of the University of Illinois at Urbana-Champaign, New Jersey Institute of Technology, and the City College of the City University of New York. See his website: http://www.eng.auburn.edu/vagrawal.