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RESEARCH

Modeling and Parasitic Extraction of the MM9 Transistor for GHz/THz CMOS RF Circuit Design

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Abstract
The goal of this paper is to decrease the number of complicated mathematical calculations for extracting the values of parasitic components and to examine the RF behavior of CMOS circuits rapidly by proposing a simple, bias-independent, three-capacitor π network small signal equivalent circuit of the sub-micrometer Philips MOS Model 9 (MM9) for high-frequency operations in the range of millimeter and terahertz. The performance of the suggested equivalent model and MM9 is compared by analyzing the simulated S-parameters in three distinct conditions: zero bias, active region, and saturation region. The frequency range considered for the analysis is from 1 GHz to 1 THz. Furthermore, the suggested model's suitability is shown by its implementation in a bilateral buffer amplifier operating at frequencies 1 GHz, 10 GHz, 50 GHz, and 100 GHz. The simulation results of the suggested equivalent model have shown excellent agreement with MM9, ranging from 10 GHz to frequencies exceeding 1 THz.

Keywords Philips MM9 · Millimeter wave · Terahertz · Small-signal model

1 Introduction

The most recent advancements in CMOS technology have made it feasible to utilize CMOS RFICs for millimeter wave and terahertz operations [1–5]. While CMOS is well known for its subpar performance as an RFIC technology, it does include intriguing characteristics that make it suitable for developing competitive radio transceiver systems. One of the key benefits is the ability to combine RF analog circuits with large-scale digital circuits, as well as the significant potential for affordable. One significant challenge in designing CMOS RFICs is the inadequate availability of accurate models that can accurately anticipate the behavior of devices operating at millimeter wave frequencies and the terahertz range. To forecast circuit performance and improve the first-time successful tape out, MOSFET model accuracy is essential [6].

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Compact MOS models like MM9 (MOS model 9), BSIM3v3 [7], and EKV [8] are often used for analog and digital circuit design. However, when these models are used at very high frequencies (VHF) without considering parasitic effects, the results are erroneous.

The Philips compact MOS Model 9 (MM9) is a physics-based analytical model used for electrical circuit modeling. It is highly suitable for both analog and digital applications. It provides an excellent description of the electrical characteristics in all relevant regions of transistor operation such as the sub-threshold current, the substrate current and the output conductance. The MM9 model is the first compact MOS model to successfully meet the benchmark tests for analog models. Since the 1970s, simulation and testing of numerous small signal equivalent circuits has been developed [9–12] to predict the correctness of the MOSFET behavior. MM9's two port common source-bulk equivalent circuit [13] consists of 7 capacitors, 3 resistors and 8 dependent sources. To reach a GHz frequency range of up to 12 GHz for 0.25 µm CMOS RF circuit design, three more capacitors are included into the MOS model 9 [14, 15]. This is necessary owing to the presence of connection metal in a multi-finger arrangement, which ensures accurate alignment between measured and simulated data. Here the values of the parasitic components have been calculated by using the measured

S-parameters at 18 different bias points. S-parameters fitting and capacitance measurements have been performed adding an extra gate-bulk zero bias capacitance to the MOSFET equivalent circuit to increase the accuracy of MOS Model 9 up to 10GHz [16]. In the sub-circuit of 0.25 µm CMOS, a substrate network [17] is included to mitigate signal coupling at high frequencies (up to 10GHz) between the drain, source, and bulk. This network allows for the extraction of the equivalent model's components using Y parameters and transit frequency. A parallel gate-drain branch is included to account for the effects of parasitic gate-drain coupling at high frequencies up to 40 GHz, as well as the influence of substrate loss, terminal resistances, and inductances. A novel extraction process called cold extraction has been devised to extract all extrinsic parasitic components from zero bias Z-parameters and intrinsic components from ON state Y-parameters [18]. The MOSFET equivalent model includes the additional gate-bulk capacitance to accurately represent the gate-bulk coupling effect. To determine the parasitic components up to 60 GHz, the S-parameters undergo standard open short de-embedding [19]. Transfer length method and dual-sweep combinational transconductance technique are combined with channel resistance method to extract the Gate Bias-Dependent Parasitic Resistances of MOSFET [20]. Focusing on precise substrate parasitic modeling up to 40 GHz utilizing a curve-fitting technique to improve model accuracy while accounting for the parasitic effects introduced at high frequencies in order to extract the MOSFET extrinsic parameters for small-signal modeling [21]. A high-frequency small-signal MOSFET model till 10 GHz is presented by utilizing the linear regression technique carried out by Y parameter analysis, substrate-related parameters, and nonreciprocal capacitors [22]. A RF MOSFET model is suggested to extract the drain-to-source conductance, the subthreshold swing, the source/drain resistance, the effective gate length, and the threshold voltage up to 60 GHz using the experimental S-parameters in linear region [23]. The aforementioned methods use multiple voltage bias testing conditions, rough assumption of frequency to calculate S parameters, diverse passive elements, bias-dependent components, and dependent current sources to accurately examine the characteristics of MOSFETs, with a maximum frequency limit of Giga Hertz range. To extract the values of parasitic components, it is essential to use Kirchhoff's Current Law (KCL) and Kirchhoff's Voltage Law (KVL), which include complicated real/imaginary equations for two-port network S parameters. These equations need intricate calculations based on the assumption of frequency.

This research presents a simple small signal equivalent model to MM9 for precise estimation of NMOS (n channel MOS transistor) S-parameters over a broad range of frequencies from GHz to terahertz and effectively addresses the aforementioned issues. Here, a small signal equivalent model with just three bias-independent capacitors is proposed for all three conditions, such as zero bias, active, and saturation operating regions, which facilitate the quick extraction of parasitic components and the easy analysis of RF CMOS behavior at millimeter and terahertz frequencies with minimal, simple and quick calculations. In order to simplify the mathematical equations, the magnitudes of S and Y parameters are used instead of the real and imaginary portions for calculating the values of parasitic components.

2 Proposed Small Signal Equivalent Model

The small signal equivalent circuit of Philips Mos Model 9 model is shown in the Fig. 1 [11]. Here the MOSFET is represented in two port common source-bulk configuration, includes the overlap capacitances (Cgso and Cdgo), terminal resistances (Rg, Rb), junction capacitances (Cjun,s and Cjun,d), and intrinsic capacitances (Cgg, Cbb, Cgd, Cgb, Cbd, Cbg, and Cdd). Considering the cold extraction method (Vgs = Vds = 0) and neglecting the influence of terminal resistors (Rb = Rg = 0) at higher frequencies, the impact of dependent current

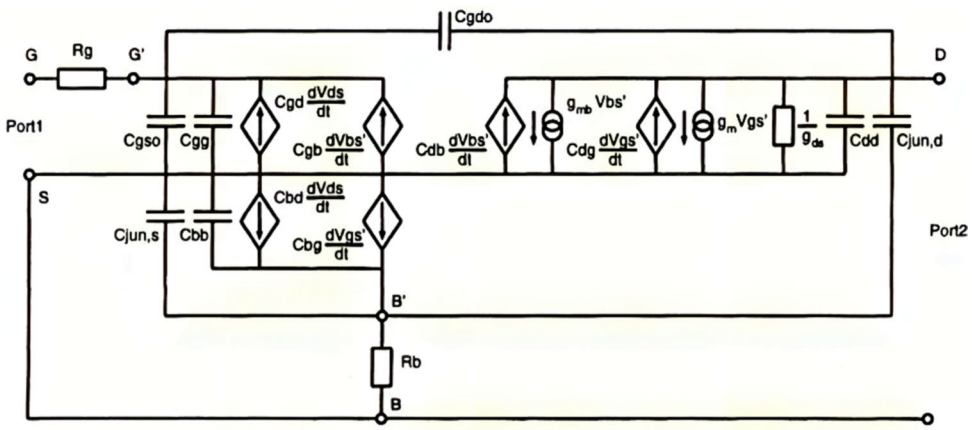

Fig. 1 Equivalent circuit of MOS MODEL 9 in two-port common source-bulk configuration

sources, Cjun,s and Cbb on the circuit will be negligible. Finally the small signal equivalent circuit is remained with Cgso, Cgg, Cdd, Cjun,d and Cgdo passive elements and these capacitors equivalent circuit is shown in Fig. 2 as a proposed 3 capacitors π network small signal equivalent model. The readily defined Y (admittance) matrix of the π network makes analysis and simulations easier, particularly in RF and microwave design. Since it can be used directly to calculate voltage and current relationships across the network and is compatible with network cascading, which is typical in RF amplifier designs, a Y-matrix in many SPICE-based tools makes the simulation process easier. This is a significant benefit for designers who analyze and optimize RF circuits using SPICE or other simulation software.

where, C1 is the parallel combination of Cgso and Cgg. i.e. C1 = Cgso+Cgg, C3 is the parallel combination of Cdd and Cjun,d. i.e. C3 = Cdd + Cjun,d.

The admittance matrix (Y) of the proposed π equivalent capacitive network is

$$Y = \begin{bmatrix} jwC1 + jwCgdo & -jwCdgo \\ -jwCdgo & jwC3 + jwCdgo \end{bmatrix} = 1/Z$$

where, w is the angular frequency and Z is the impedance matrix.

The two-port vector network analyzer is used to measure the S-parameters of the Philips MM9 MOSFET, rather than impedance/admittance parameters. Therefore, it is necessary to transform the S parameters into Z parameters initially. In the case of a typical two-port network, the conversion process can be accomplished using eqs. (1)–(4), with Zo representing the characteristic impedance of 50 Ω [24].

$$Z_{11} = \left[\frac{(1+S11)(1-S22)+S12S21}{(1-S11)(1-S22)-S12S21}\right]Zo \quad (1)$$

$$Z_{12} = \left[\frac{2S12}{(1-S11)(1-S22)-S12S21}\right]Zo \quad (2)$$

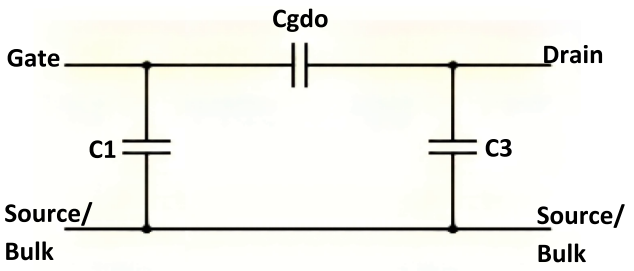

Fig. 2 Proposed capacitive equivalent circuit of MOS MODEL 9 at high frequencies

$$Z_{21} = \left[\frac{2S21}{(1-S11)(1-S22)-S12S21}\right]Z0 \quad (3)$$

$$Z22 = \left[\frac{(1-S11)(1+S22)+S12S21}{(1-S11)(1-S22)-S12S21}\right]Z0 \quad (4)$$

Our innovative technique involves characterizing the parasitic/intrinsic capacitances of a four-terminal Philips MM9 NMOSFET via two-port S-parameters measurement is as the following:

Step 1: Perform S-parameter measurements on the common source-bulk configuration of 0.25 × 400 µm MM9 at a lower cutoff frequency of 1 GHz, as depicted in Fig. 3;

Step 2: Transform the recorded magnitudes of S-parameters into Z-parameters using eqs. (1)–(4), and subsequently convert them into Y-parameters;

Step 3: The intrinsic/parasitic capacitances C1, Cdgo, and C3 depicted in Fig. 2 are extracted by utilizing the calculated Y-parameters and the admittance matrix Y at frequency 1 GHz.

The parameters obtained from the three steps mentioned above are presented in Table 1. The entire MM9 small signal model, which consists of three resistors, eight dependent current sources, and seven capacitors, is perfectly replaced by the suggested three capacitors π network small signal equivalent model with extracted parasitic capacitances at high frequency.

3 Results

Figure 4 displays the simulated S-parameters of the MM9 model and the suggested capacitive π network equivalent model at zero bias, allowing for a direct comparison. Here the Philips MOS Model 9 NMOS transistor and suggested equivalent model are used in common source configuration with a source and load impedance of 50 Ω. Figure 4(a)-(d), shows the main (0.001–1 THz) and sub graphs (1–10 GHz) of input reflection (S11), reverse transmission (S12), forward transmission (S21) and output reflection (S22) coefficients respectively in decibels. Similarly, Fig. 4(e)-(h), shows the phase angle of these S parameter coefficients in degree. To draw the quick conclusion from these eight graphs, an absolute error is calculated as per eq. (1) and represented in Fig. 5. The following observations have been made based on this figure. 1. From 0.52 at 0.1 GHz to 44.88 at 1.4 GHz, the error is increasing. The poor electrical performance has been noted at low frequencies because capacitors tend to restrict low-frequency signals due to their frequency-dependent impedance, even though there is less inaccuracy at 0.1 GHz with regard to S parameters. 2. After 1.4 GHz; error begins to decrease till 0.54 at

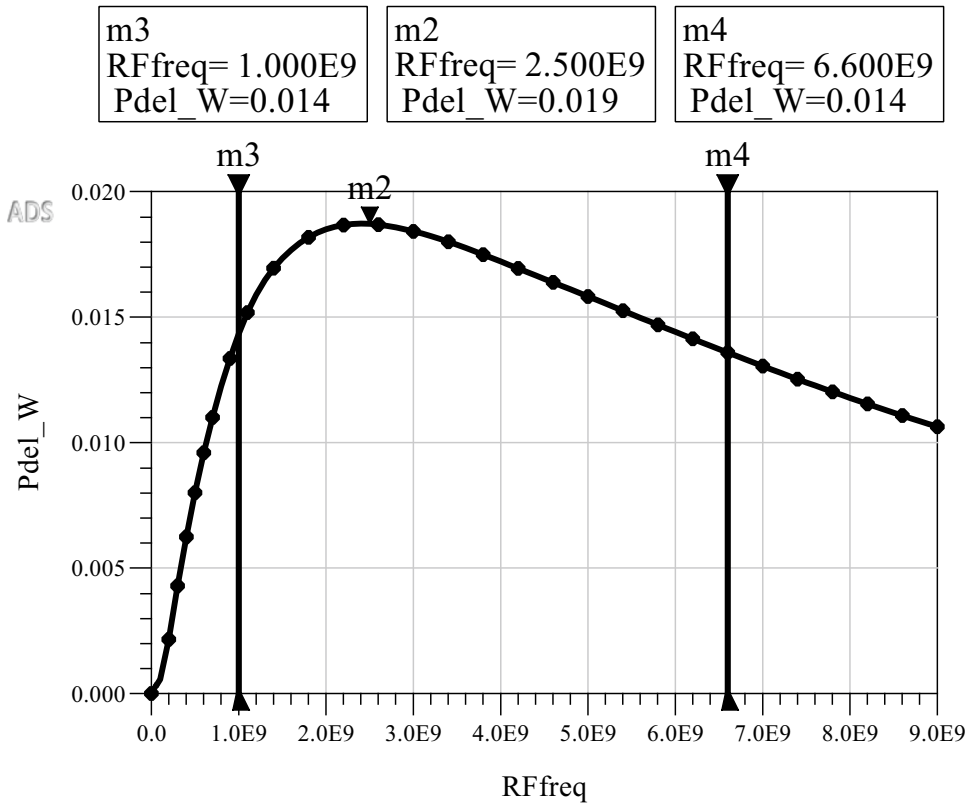

Fig. 3 Philips MM9 NMOS output power (Pdel_W) in watts with lower and upper cutoff frequencies

Table 1 Simulated S-parameters, calculated Y-parameters and extracted parasitic capacitances

Magnitudes of MM9 S-parameters at 1 GHz				Converted Y-parameters (mS)				Extracted Parasitic capacitances (pF)		
|S11|	|S12|	|S21|	|S22|	|Y11|	|Y12|	|Y21|	|Y22|	C1	Cdgo	C2
0.893	0.451	0.451	0.893	9.9	4.23	4.23	9.9	0.82	0.67	0.32

100 GHz. These findings suggest that the proposed model can be used in the place of MM9 at higher frequencies, especially starting at 10 GHz.

$$\text{Absolute error} = |\text{True Value} - \text{Measure Value}|$$

$$= \left|\sum \text{MM9 S parameters} - \sum \text{proposed model S parameters}\right| \quad (1)$$

Table 2 sows the comparison of S-parameters between MM9 NMOS and the proposed equivalent model in terms of the linear and saturation operating regions at a frequency of 100GHz. To maintain the linear operating region, the gate-source terminals connect to a 5 V DC and 20 dBm AC power source, while the drain-source terminals are kept at a 0.5 V DC level. Similarly, to maintain the saturation operating region, the gate-source terminals connect to a 0.1 V DC and 1 dBm AC power source, while the drain-source terminals are kept at a 5 V DC level.

4 Circuit Example

In 5G, IOT, Satellite and Radar applications, transceivers plays the crucial role by buffering signals in bidirectional for facilitating the full duplex communication. As a part of transceiver, Bilateral Buffer Amplifier (BBA) remains an essential component. A single transistor BBA, as depicted in Fig. 6, and a two transistors wideband cascode bilateral buffer amplifier [25], as depicted in Fig. 7, are taken into consideration in order to evaluate the performance of the suggested equivalent model at the circuit level and application point of view. As indicated in Tables 3 and 4, respectively, these two circuits are designed and simulated using the MM9 NMOS (0.25×400 µm) and the proposed π network capacitors equivalent model for comparison in terms of S-parameters in decibels and phase angle of S-parameters in degrees. Table 5 compares electrical performance metrics of amplifier such as peak source current (Is), peak load

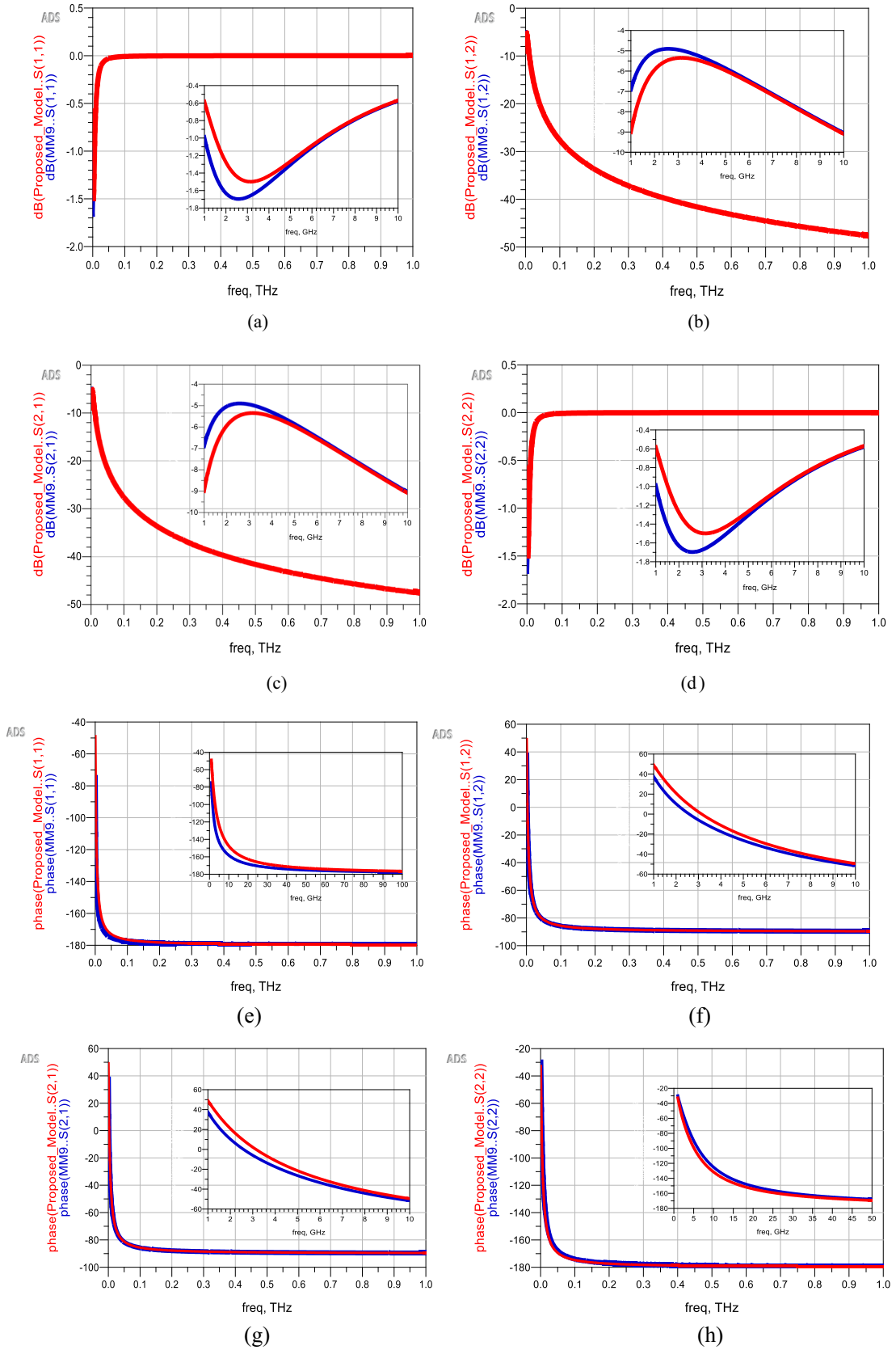

Fig. 4 Simulated S-parameters of the MM9 NMOS and Proposed capacitive π network equivalent model at zero bias

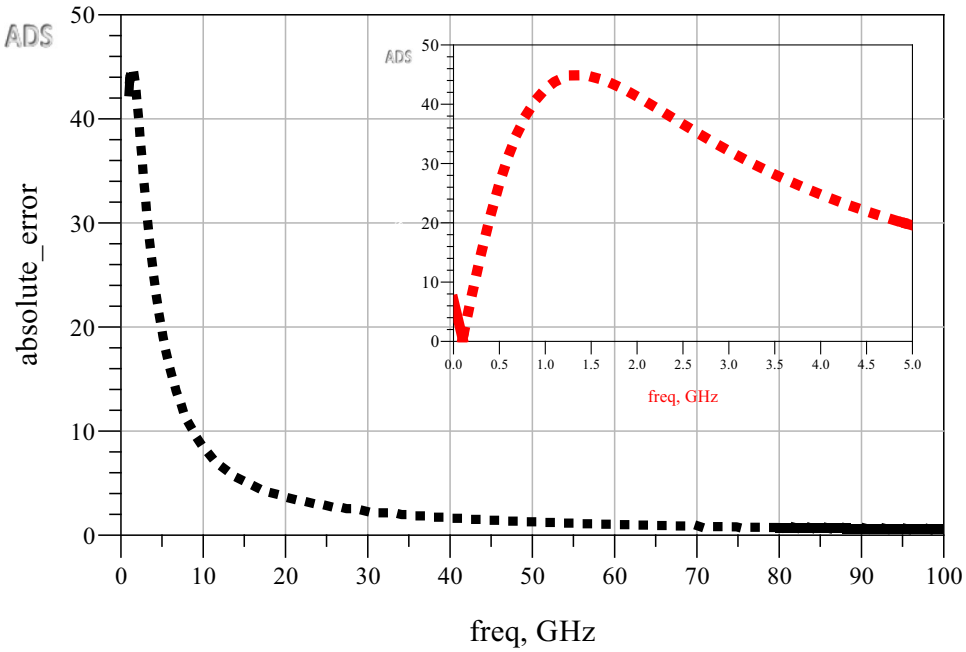

Fig. 5 S parameters Absolute error of proposed model

Table 2 S-parameters comparison between the proposed equivalent model and the MM9 NMOS in terms of linear and saturation region at 100 GHz

MM9 NMOS	Linear operating region							
	S11	S12	S21	S22	∠S11	∠S12	∠S21	∠S22
	−0.009	−26.9	−26.9	−0.009	−177.4	−86.1	−86.1	−174.8
	Saturation region							
	S11	S12	S21	S22	∠S11	∠S12	∠S21	∠S22
	−0.002	−33.3	−33.3	−0.002	−178.7	−87.5	−87.5	−176.9
Proposed Equivalent model	Linear operating region							
	S11	S12	S21	S22	∠S11	∠S12	∠S21	∠S22
	−0.007	−27.6	−27.6	−0.007	−176.4	−85.5	−85.5	−174.7
	Saturation region							
	S11	S12	S21	S22	∠S11	∠S12	∠S21	∠S22
	−0.005	−32.6	−32.6	−0.005	−178.4	−86.5	−86.5	−176.7

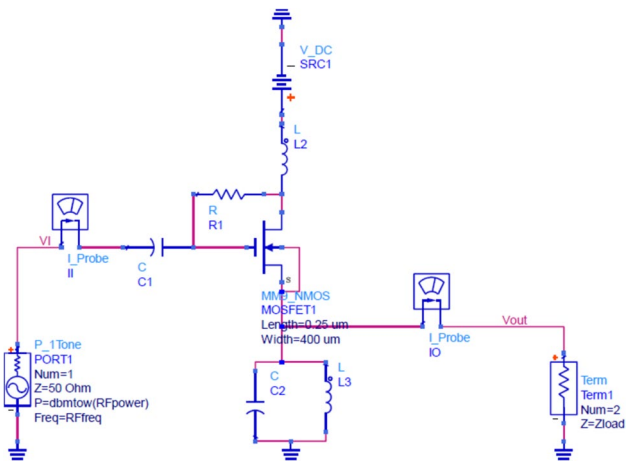

Fig. 6 Single stage Buffer Amplifier

voltage (Vo), and peak load current (Io) at various frequencies with source power of 10 dBm. Four distinct frequencies i.e. 1 GHz, 10 GHz, 50 GHz, and 100 GHz that roughly span L-band to W-band have been used in this comparative analysis. Error % is computed for MM9 and the proposed model at the circuit level for improved comparison and better conclusion. The error percentage is often determined using eq. (2), and similarly, the percentage error tabulated in 3, 4, and 5 is computed using eq. (3).

$$\text{Error\%} = \frac{|\text{True Value} - \text{Measured Value}|}{\text{True Value}} \times 100 \tag{2}$$

$$= \frac{|\sum \text{MM9 Parameters} - \sum \text{Proposed Model Parameters}|}{\sum \text{MM9 Parameters}} \times 100 \tag{3}$$

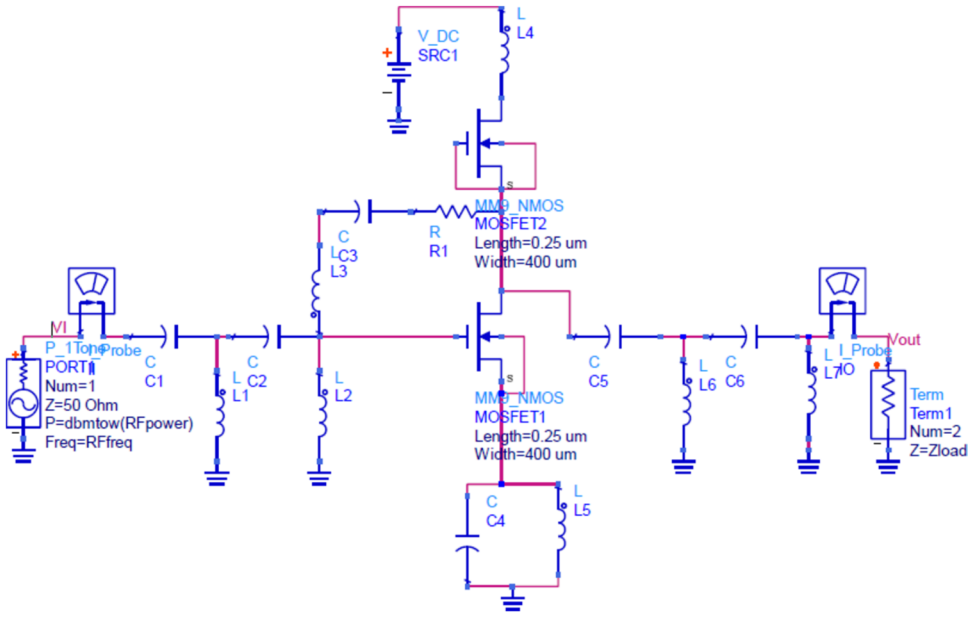

Fig. 7 Cascode Buffer Amplifier

Table 3 Comparison of S-parameters between the bilateral buffer amplifier (BBA) with MM9 NMOS and the proposed equivalent model at various frequencies

Signle stage Bilateral Buffer Amplifier									
Frequency (GHz)	BBA with MM9 NMOS				BBA with Equivalent Model				Error (%)
	S11(dB)	S12(dB)	S21(dB)	S22(dB)	S11(dB)	S12(dB)	S21(dB)	S22(dB)	
1	−9.16	−0.77	−0.77	−8.70	−4.85	−1.76	−1.76	−4.78	32.2
10	−20.60	−0.04	−0.04	−20.60	−18.00	−0.07	−0.07	−18.00	12.4
50	−31.57	−0.00	−0.00	−31.57	−29.61	−0.00	−0.00	−29.61	6.2
100	−32.05	−0.00	−0.00	−32.04	−30.95	−0.00	−0.00	−30.95	3.4
Cascode Wide band Bilateral Buffer Amplifier									
Frequency (GHz)	BBA with MM9 NMOS				BBA with Equivalent Model				Error (%)
	S11(dB)	S12(dB)	S21(dB)	S22(dB)	S11(dB)	S12(dB)	S21(dB)	S22(dB)	
1	−6.66	−4.67	−4.67	−4.74	−1.74	−8.16	−8.16	−6.24	17.1
10	−19.42	−0.05	−0.05	−19.41	−20.25	−0.04	−0.04	−20.24	4.2
50	−16.49	−0.09	−0.09	−16.49	−16.71	−0.09	−0.09	−16.71	1.5
100	−23.46	−0.02	−0.02	−23.46	−23.70	−0.01	−0.01	−23.70	1.6

Table 4 Comparison of phase angle of S-parameters between the BBA with MM9 NMOS and the proposed equivalent model at various frequencies

Signle stage Bilateral Buffer Amplifier									
Frequency (GHz)	BBA with MM9 NMOS				BBA with Equivalent Model				Error (%)
	∠S11	∠S12	∠S21	∠S22	∠S11	∠S12	∠S21	∠S22	
1	81.94	129.8	129.8	2.27	106.6	145.0	145.0	3.36	16.3
10	−77.85	12.83	12.83	−76.27	−77.05	14.17	14.17	−75.47	3.3
50	−86.91	2.14	2.14	−88.74	−86.30	2.52	2.52	−88.37	1.0
100	−88.49	0.39	0.39	−90.70	−88.03	0.58	0.58	−90.47	0.3
Cascode Bilateral Buffer Amplifier									
Frequency (GHz)	BBA with MM9 NMOS				BBA with Equivalent Model				Error (%)
	∠S11	∠S12	∠S21	∠S22	∠S11	∠S12	∠S21	∠S22	
1	−68.7	103.1	103.1	19.0	−51.0	134.4	134.4	63.8	80.0
10	168.7	38.2	38.2	87.8	179.0	39.3	39.3	79.5	1.2
50	119.9	27.4	27.4	114.9	120.2	27.6	27.6	114.9	0.2
100	105.0	13.1	13.1	101.8	105.1	13.2	13.2	101.3	0.08

Table 5 Comparison of performance parameters between the BBA with MM9 NMOS and the proposed equivalent model at various frequencies

Signle stage Bilateral Buffer Amplifier							
Frequency (GHz)	BBA with MM9 NMOS			BBA with Equivalent Model			Error (%)
	Vo(mV)	Io (mA)	Is(mA)	Vo(mV)	Io (mA)	Is(mA)	
1	917	18	20	812	16	25	15.4
10	971	19	20	960	19	19	1.1
50	999	20	20	998	20	20	0.09
100	1000	20	20	999	20	20	0.09
Cascode Bilateral Buffer Amplifier							
Frequency (GHz)	BBA with MM9 NMOS			BBA with Equivalent Model			Error (%)
	Vo(mV)	Io (mA)	Is(mA)	Vo(mV)	Io (mA)	Is(mA)	
1	337	7	9	332	7	15	0.3
10	996	20	20	993	20	20	0.2
50	984	20	21	985	20	21	0
100	997	20	20	997	20	20	0

The following inferences can be made by comparing the S parameters in degrees, decibels, and electrical performance metrics from the tables above with respect to error percentage. (1) At higher frequencies, such as centimeter wave (>10GHz), millimeter wave (30–300 GHz), and terahertz frequency (0.1–10 THz) range, the suggested equivalent model is effectively replicating the MM9, as evidenced by the error percentage decreasing as the operating frequency increases and maintaining a considerable error % from 10 GHz onward. (2) This operating frequency is not recommended for the suggested model since the largest error % is shown at the lower cutoff frequency of MM9, which is 1 GHz. (3) Although multi-transistor or cascode buffer amplifiers are advantageous at high frequencies, they will pose issues at low frequencies due to the addition of poles to the frequency response. This can cause unfavorable phase shifts and instability in systems, which is why the lowest frequency of 1 GHz exhibits the highest percentage inaccuracy i.e., 80% in terms of phase angles of S parameters. But for higher frequencies (> 10 GHz), a positive improvement is noted comparing with single transistor buffer amplifier. (4) The error percentage in single and multi transistor buffer amplifiers is almost negligible at 50 and 100 GHz. Finally, it is determined that the proposed simple small signal equivalent model can be replaced with the MM9 MOSFET for easy and quick analysis of CMOS circuits at high frequencies, such as in millimeter and terahertz applications.

5 Future Scope

The proposed MOSFET small signal equivalent model is unsuitable for applications where the gain requirement is greater than 0 dB because it only includes passive components (capacitors). To date, the aforementioned gain need has been satisfied in all literature by using a dependent current source that is not portable. However, there is a possibility that when Schottky diodes are used in the suggested model, the gain could rise over 0 dB, as in the Cockcroft-Walton Voltage Multiplier [26].

6 Conclusion

A novel and concise small signal equivalent model has been introduced to precisely forecast the RF characteristics of Philips MOS Model 9 transistor operating at millimeter and terahertz frequencies. The proposed model consists of three capacitors arranged in a pi network configuration. A 0.25×400 µm CMOS technology model has been developed. This model provides high accuracy over a broad range of frequencies especially for applications where the gain requirement is less than or equal to 0 dB. Ultimately, an assessment was carried out at the circuit level using single and multi transistor bilateral buffer amplifiers. The outcomes indicate a favorable correspondence between the suggested model and MM9 from 10 GHz onwards.

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Declarations

Competing Interests The authors declare no competing interests.

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