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Editorial

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Seven articles in this issue cover the topics of built-in self-test (BIST), hardware security, printed circuit board (PCB) failures, test optimization, and radio frequency (RF) transistor modeling.

The first paper replaces the linear feedback shift register (LFSR) of a self-testing circuit by hardware that combines arithmetic logic with machine intelligence components. The objectives are to reduce test power and enhance coverage efficiency. Authors are Thangam from St. Mother Theresa Engineering College, Vagaikulam, Thoothukudi, Tamilnadu, India, and Manjith from Dr. Sivanthi Aditanar College of Engineering, Tiruchendur, Thoothukudi, Tamilnadu, India.

The next three papers focus on hardware security. The first among those, the second paper of this issue, addresses the problem of side channel attack (SCA) to maliciously decode the data encoded by the secAES encryption algorithm. The authors are Wu, Li and R. Zhang from Guilin University of Electronic Technology, Guilin, China, and H. Zhang from University of Chinese Academy of Sciences, Beijing, China.

The third paper, continuing the theme of countermeasures against side channel attacks, evaluates tradeoffs between the cost of protection in terms of power, performance, and area against the levels of protection. Resilience of protection against device aging is also considered. Authors are Anik, Reefat and Karimi from University of Maryland Baltimore County, Baltimore, Maryland, USA, and Cheng, Danger, and Guilley from Institut Polytechnique de Paris, Palaiseau, France and Secure-IC S.A.S., Paris, France.

The fourth paper examines existing hardware Trojan detection approaches for scalability, application to large-scale circuits, and inability to cover various types of Trojans. It then proposes hardware Trojan features, which are easily identifiable for circuit nodes and help detect Trojans, effectively. Authors are Liu, Li, Guo, Zhu, Wang, Zhong, Zhang from Information Engineering University, Zhengzhou, Henan, China.

The fifth paper presents a study of printed circuit board (PCB) with mounted chips. Those chips use plastic packages with ball-grid arrays tied to the PCB by solder joints. The study examines the expected duration of failure-free operation in the presence of random mechanical vibrations. Results also show that solder failure chances vary with position of the chip on PCB. Authors are Muthuram and Sarvanan from PSG College of Technology, Coimbatore, India.

The sixth paper provides a test optimization procedure. The basic idea introduced here is to reduce the cost of testing without sacrificing either the yield or quality. Starting with simple tests, statistical and machine learning methods identify devices that should be subjected to increasingly rigorous tests as wafer testing progresses. The authors are Wu, Hao, and Zhan from Anqing Normal University, Anqing, China.

The seventh paper presents a simplified model for an RF CMOS transistor in the form of a pi-network consisting of three capacitors. Authors are Gadige and Paremesha from Central University of Karnataka, Kalaburagi, India.

We end the year 2024 by completing Volume 40 of *JETTA*. This volume contains fifty-three papers. In the first eleven months of 2024, we received over two hundred submissions, maintaining the trend of recent years.

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