Journal of Electronic Testing (2024) 40:625–644
https://doi.org/10.1007/s10836-024-06143-5

RESEARCH

Investigating and Improving the Performance of Radiation-Hardened SRAM Cell with the Use of Multi-Voltage Transistors

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Received: 25 July 2024 / Accepted: 24 September 2024 / Published online: 3 October 2024

Abstract

This research introduces a proposed energy-efficient radiation-hardened and improved read stability (RHIRS)-12T SRAM cell with a polarity hardening technique, which lowers the vulnerable nodes and allows all single-event upset (SEU) techniques to recover from single-event multiple-effect (SEME). To evaluate the relative performance using UMC 65nm CMOS technology of the proposed cell, a comparison analysis is conducted with various radiation-hardened SRAM cells currently in use, such as RHPD-12T, RHWC12T, HPHS12T, RHBD12T, RHD-12T, and EDP12T. When compared to the existing 12T SRAM cells, the proposed RHIRS-12T radiation-hardened SRAM cell has the highest read and hold stability. Compared to EDP12T, RHPD-12T, and RHWC12T SRAM cells, the simulation results demonstrate improvements in write delay of 33.63%, 21.41%, and 9.58%, respectively. It exhibits the lowest read delay as compared to the other considered SRAM cells. It saves 76.34%, 43.68%, 2.77%, and 0.13% energy consumption compared with RHBD12T, HPHS12T, RHPD-12T, and RHWC12T, respectively, during the read operation and it also saves 55.59%, 21.44%, and 6.04% energy compared with EDP12T, RHD-12T, and RHWC12T, respectively, during the write operation. It also shows enhancements of 78.55%, 61.06%, 44.87%, 20.11%, and 0.12% in critical charge value compared to RHBD12T, HPHS12T, RHWC12T, RHPD-12T, and RHD-12T, respectively. Additionally, we evaluate the relative performance of the proposed RHIRS-12T, a comparison analysis is performed with RHD-12T radiation-hardened SRAM cells having low-voltage transistor (LVT), standard-voltage transistor (RVT or SVT), high-voltage transistor (HVT), and super-high voltage transistor (SHVT). It exhibits the highest improvement in read stability at LVT compared to RHD-12T SRAM cell. It can also be used for aerospace applications due to its improved performance and stability.

Keywords SRAM · Radiation effects · Access time · Stability · Energy · Multi-voltage transistors

1 Introduction

As technology advances, the vulnerability of circuits to radiation has increased, making circuit reliability a top concern for circuit designers [1]. Static-random-access-memory (SRAM) cell is the memory cell chosen for data storage in aerospace applications due to its higher packaging density and enhanced logic performance [2, 3]. This indicates that there is a greater chance of soft errors affecting SRAM. According to earlier experimental findings, conventional 6T SRAM might need more dependability to withstand space radiation [4].

The design of a digital hardware application-specific integrated circuit (ASIC) comprises not only the implementation of complicated logic but also the reduction of power consumption and operating time. We try to simplify this explanation here from the viewpoint of a firmware programmer. Many logic cells are found in an ASIC. Like bricks in the construction of a house, each logic cell can be utilized in design to accomplish different functionalities and this logic cell consists of several transistors, or switching elements. Therefore, the overall qualities of a final product are determined by the power and processing time of these cells. In

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this case, it is important to note that the processing time and power consumption of the switching element must be regulated to get the desired outcome. Both the static and dynamic power are involved in power usage. Dynamic power is consumed to switch ON the transistors. Leakage current occurs when a transistor is switched ON (in the logical OFF state), and this causes static power. In this article, we focus on the parameters performance of radiation-hardened 12T SRAM cell to understand the effects of low-voltage transistor (LVT), standard-voltage transistor (RVT or SVT), high-voltage transistor (HVT), and super-high voltage transistor (SHVT) cells.

According to recent research, there is a high resilience among different types of RHBD SRAM cells. Calin et al. [10] introduced a dual-interlocked-storage-cell (DICE), an SRAM cell architecture that consists of twelve transistors. This SRAM cell also consists of interlocking junctions for storing inverted data. In the case that radiation impacts any of its nodes, it employs positive feedback to preserve the logic that has been stored. Single-event-multiple-effect (SEME) refers to the possibility of data alterations in a DICE cell if radiation hits two neighboring nodes. This implies that it is immune to SEU and tolerant of SEME. The RHD12 [11] is a different radiation-hardened SRAM cell, that can regain its initial stored data following an SEME but is unable to do so following a SEU at its QB storage node. Its enhanced variant, RSP-14T [12], is capable of withstanding elevated charges at the QB node. However, it remains incapable of retrieving data that has been stored in case the QB storage node switches from '0' to '1' and presents a noticeable write delay. As illustrated in Fig. 1, the radiation-hardened SRAM cells that have been recently reported, EDP12T [1], RHPD-12T [5], RHWC-12T [6], HPHS12T [7], RHBD12T [8], and RHD-12T [9], can be regained from SEUs of any polarity [13] and the SEMEs. However, both EDP12T [1] and RHBD12T [8] have low read and hold stability and are vulnerable to radiation during read and hold operations, respectively. EDP12T [1] and RHWC-12T [6] have high write delay and consume more energy during write operation. HPHS12T [7] and RHBD12T [8] have a high read delay and also consume higher energy under read operation. Moreover, RHBD12T [8], HPHS12T [7] and RHWC-12T [6] have less radiation tolerance.

To address the problems mentioned above, we propose an energy-efficient radiation-hardened and improved read stability (RHIRS)-12T SRAM cell that is immune to SEME and capable of regaining from any polarity of SEUs that can affect the sensitive nodes. Due to having the same radiation tolerance of RHD-12T [9] as compared to the proposed RHIRS-12T radiation-hardened SRAM cell. We evaluate and compare different parameters of the proposed RHIRS-12T

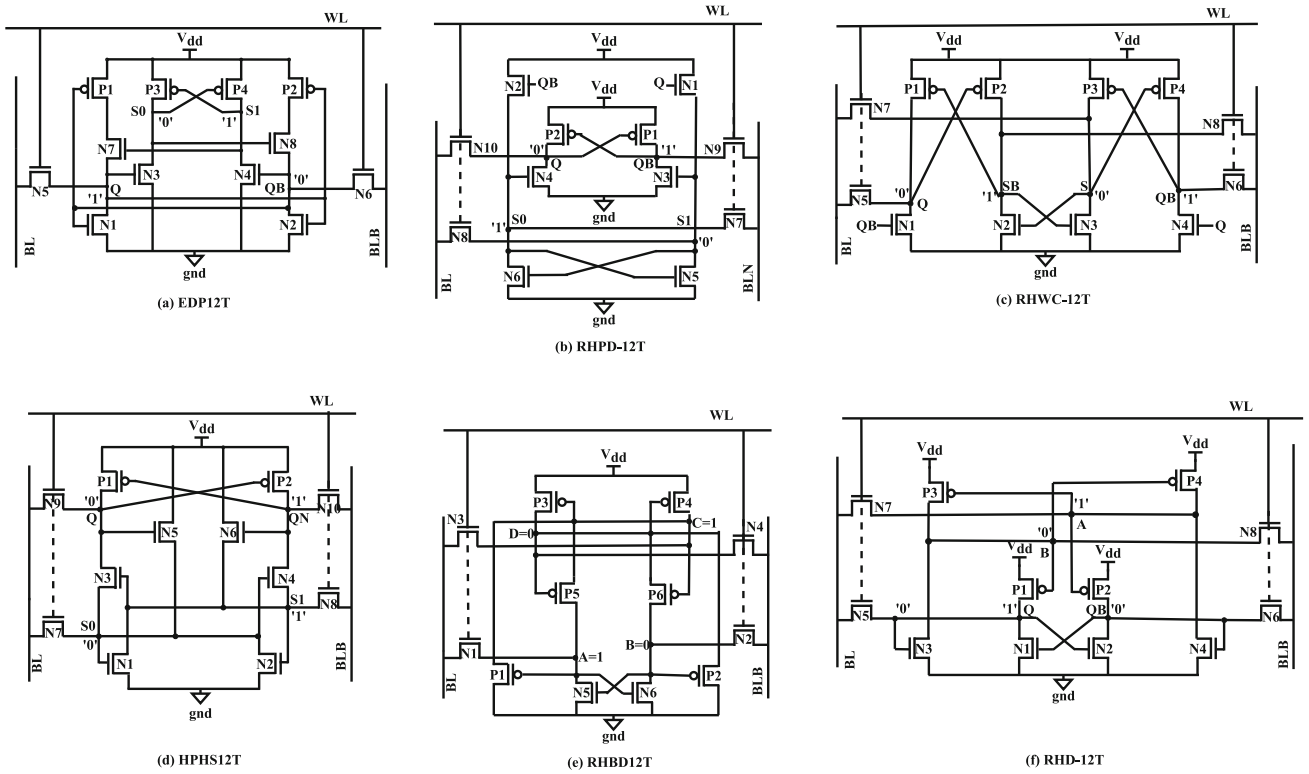


Fig. 1 Circuit diagrams of the existing radiation-hardened 12T SRAM cell (a) EDP12T [1], (b) RHPD-12T [5], (c) RHWC-12T [6], (d) HPHS12T [7], (e) RHBD12T [8], and (f) RHD-12T [9]

and RHD-12T radiation-hardened SRAM cell using multi-voltage transistor. It has the following properties that are mentioned below :

1) The proposed RHIRS-12T radiation-hardened SRAM cell can recover from SEME and has superior resistance from SEUs compared to its rivals.
2) The proposed RHIRS-12T radiation-hardened SRAM cell offers better readability when compared to RHD-12T SRAM cell.
3) The proposed RHIRS-12T having LVTs or RVTs or HVTs radiation-hardened SRAM cell is faster during the write operation compared to the RHD-12T SRAM cells.
4) In comparison to other SRAM cells, the proposed RHIRS-12T having LVT radiation-hardened SRAM cells requires less energy during the write operations.
5) The LVT-based radiation-hardened SRAM cell consumes less delay and energy during read operations than the other 12T SRAM cells.
6) In comparison to the compared cells, the proposed RHIRS-12T radiation-hardened SRAM cell is more stable during hold and read operations.

This research paper is organized in the following manner. Section 2 demonstrates the circuit representation of the proposed RHIRS-12T radiation-hardened SRAM cell with its transient analysis during the read, and write operations and its evaluation of soft errors. Section 3 describes a detailed description of the simulations that have been performed and demonstrates the comparison of the results, pointing out the advantages and characteristics of the proposed RHIRS-12T radiation-hardened SRAM cell in terms of radiation tolerance and total performance. Section 4 concludes this research paper.

2 The Proposed Radiation-Hardened-by-Design 12T SRAM Cell

2.1 Cell Design and Structural Diagram

The proposed RHIRS-12T radiation-hardened SRAM cell is illustrated in Fig. 2. It is based on polarity hardening technology, which lowers the number of feedback loops and data instabilities. It consists of four PMOS and eight NMOS transistors. For the pull-up PMOS transistors (P1, P2, P3, and P4), the width-to-length ratio (W/L) is 80 nm/65 nm, and for the drive NMOS transistors (N1, N2, N3, and N4), the W/L is 280 nm/65 nm. The four additional NMOS transistors N5-N8 are referred to as access transistors (ATs), and the W/L is 140 nm/65 nm. It includes four storage nodes, indicated

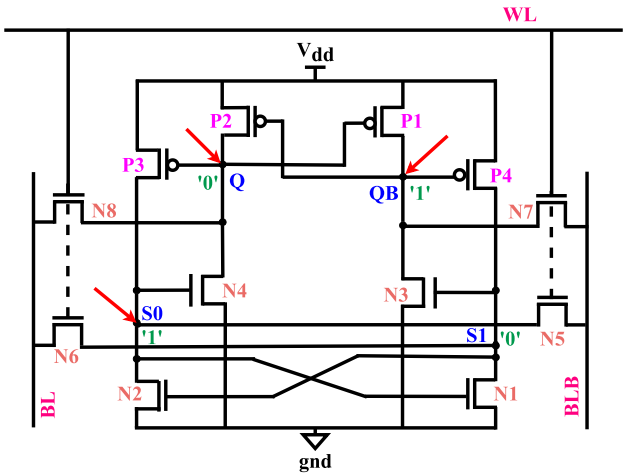


Fig. 2 Schematic view of the proposed RHIRS-12T radiation-hardened SRAM cell

as Q, QB, S1, and S0, wordlines, indicated as WL, and two bitlines, denoted as BL and BLB. All the access transistors that are operated by WL, connect all the storage nodes. The ATs N6 and N8 are connected to BL and the ATs N5 and N7 are connected to BLB.

Figure 3 illustrates the block diagram of an SRAM array which consists of the proposed cell. Assume that Q = '0' and QB = '1' represent the logic '0' stored state of the proposed cell. As a result, S0 and S1 are holding '0' or '1', respectively. Taking this into consideration, the following describes its fundamental operation and analysis of the SEU and SEME recovery.

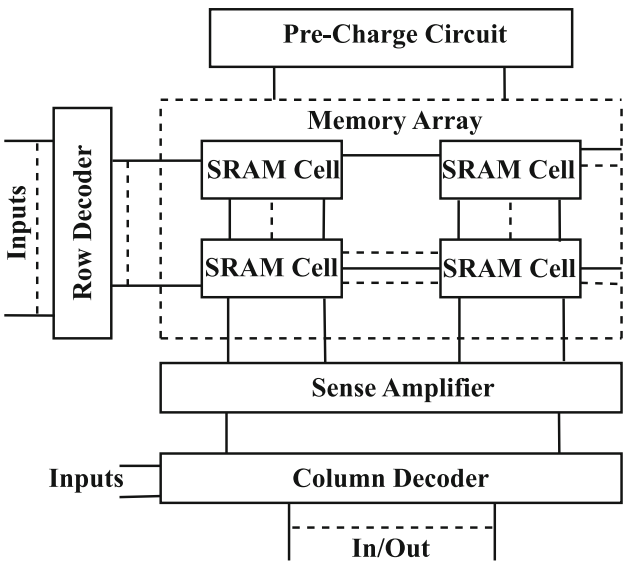


Fig. 3 Block diagram representation of an SRAM array containing the proposed RHIRS-12T radiation-hardened SRAM cell

2.2 Working Principle

Various signals are applied to an SRAM cell during its various operations, including its write, read, and hold functions. The logic voltage supplied to the wordlines (WL), the bitlines, and their related states throughout each operation is detailed in Table 1, which specifies these signals. This table provides an overview for interpreting the particular signal combinations needed for the various SRAM cells to operate.

2.2.1 Hold Operation

The proposed RHIRS-12T radiation-hardened SRAM cell works in hold mode by connecting all wordlines (WL) at low supply voltage (gnd), due to it all the ATs (N5-N8) are turned OFF. At the same instant, all the bitlines (BL and BLB) are precharged at high supply voltage (Vdd) to reduce wake-up time [1]. To ensure that the cell can keep the stored data, inside the proposed RHIRS-12T radiation-hardened SRAM cell, transistors P1, P3, N1, and N4 are switched ON, and transistors P2, P4, N2, and N3 are switched OFF because the nodes Q and S1 store at logic state 1, and the nodes QB and S0 store at logic state 0 at this time.

2.2.2 Write Operation

For a write operation, a high supply voltage is supplied to each wordline (Vdd). As a result, the N5, N6, N7, and N8 ATs are all turned activated. To write '1' at node Q, Vdd is connected to BL, whereas BLB is connected to gnd to change the data that was originally stored there. Nodes S0 and QB through N5 and N7, respectively, are pulled down by BLB since it is connected to gnd. At a subsequent time, node QB switched ON P2 and P4, while node S0 switched OFF N1 and N4. BL simultaneously pulls up Q and S1 nodes through N8 and N6, respectively. This means the Q node turned OFF P1 and P3. Similarly, node S1 switched ON N2 and N3 which is shown in Fig. 4(a).

Cross-coupling [14] across P1 and P2 transistors increases the voltage difference across the Q and QB storage nodes. Similarly, cross-coupling across N1 and N2 transistors increases the voltage difference across S0 and S1 nodes. This cross-coupling method enhances the voltage differential in the proposed RHIRS-12T radiation-hardened SRAM cell, enabling efficient data storage and retrieval. As a result, the write operations illustrated in Fig. 5 are accomplished effectively.

2.2.3 Read Operation

For a read operation, all the wordlines (WLs) are connected to a high supply voltage (Vdd). Consequently, all the ATs (N5-N8) are activated. To perform a read operation, all bitlines must initially be precharged to Vdd. When the proposed RHIRS-12T SRAM cell sets at a low logic value, BL discharges via N6 and N8 transistors, and the BLB is unchanged since transistor N3 is in the deactivated mode. The sense amplifier finds a 200 mV potential difference across the bitlines (BL and BLB), which indicates the stored logic value, the read operation is regarded as successful as illustrated in Fig. 4(b). The transient analysis of different signals during read operations is shown in Fig. 6.

2.3 Analysis of Soft-Errors

This subsection within the proposed RHIRS-12T radiation-hardened SRAM cell discusses the effects of a SEU induced at sensitive nodes. Radiation exposure causes the drain diffusion region, which holds binary values around reverse-biased OFF transistors to become sensitive. The stored data may alter as a result of this sensitivity, which could impact the cell's logic state. For instance, if a particle of radiation strikes the drain area of an NMOS/PMOS transistor, it may alter its output from a '1' to a '0', based on the value that was previously stored. But NMOS transistors surround the storage node (S1), where this cell stores '0', which helps to shield the logic state from these radiation-induced alterations. The nodes Q, QB, and S0 are the ones that are sensitive in this instance. For altering the original stored logic value at the node, we use the analogous circuits [15] that produce a positive and negative transient pulse, respectively.

Furthermore, as was already noted, SEMEs are frequently seen in technological advancements at the nanoscale since a single particle of radiation striking one node can produce a charge that affects nearby nodes. The analysis of charges is required to ascertain their possible influence on the operational condition of an SRAM cell during an SEME to be considered for charge sharing. This analysis ensures the trustworthiness of the SRAM cells in the presence of SEMEs by evaluating the potential for charge diffusion and radiation

Table 1 Signals applied of an SRAM cell for different functions

Signal name	Hold mode	Write'1' mode	Write'0' mode	Read mode
BL	high logic	high logic	low logic	precharged
BLB	high logic	low logic	high logic	precharged
WL	low logic	high logic	high logic	high logic

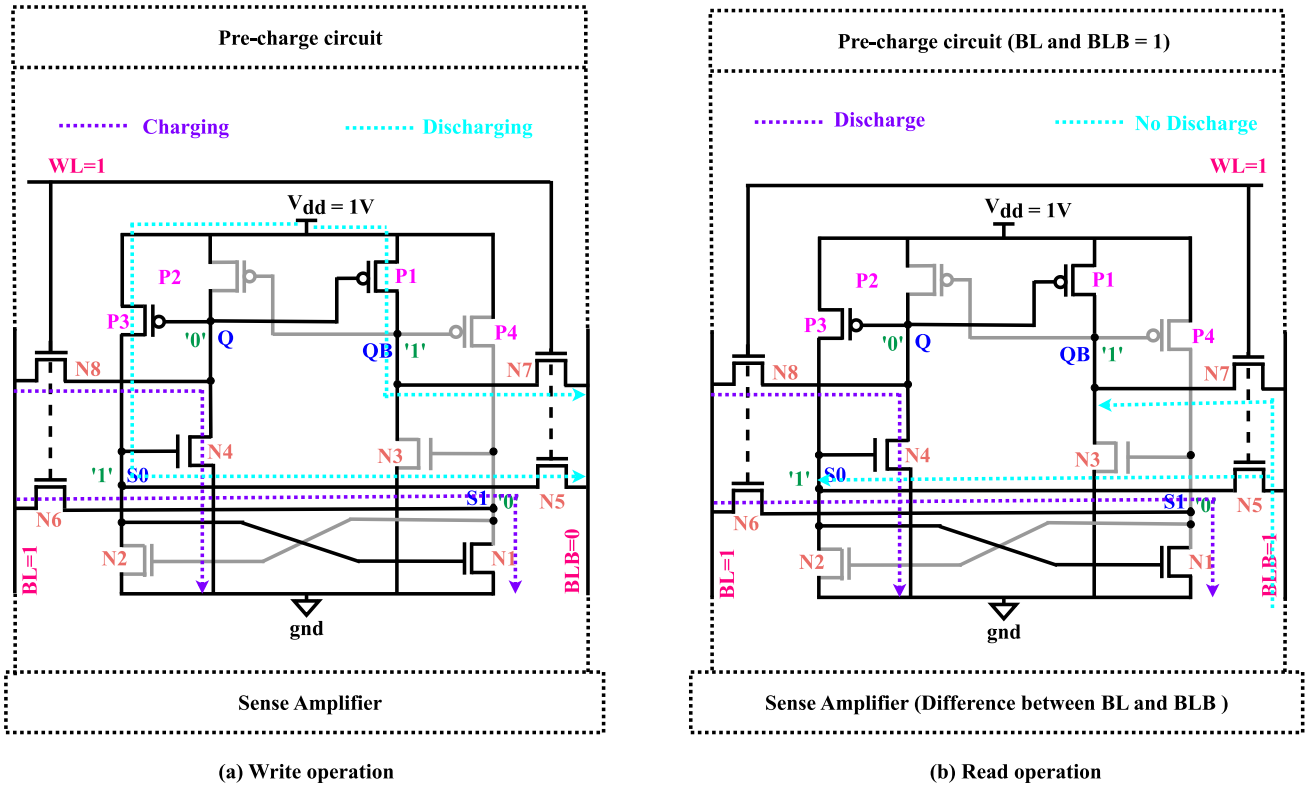


Fig. 4 Circuit diagrams of the proposed RHIRS-12T radiation-hardened SRAM cell during (a) Write operation, and (b) Read operation

strikes to change the state of an SRAM cell. To begin with, first, a primary node is recognized to achieve this. The primary node is the sensitive node that can endure the lowest critical charge out of all the other sensitive nodes [3]. All possible combination sensitive node-pairs involving the primary node are connected with a current source to determine which node-pair is the critical one. There is a greater probability for the critical node-pair to reverse the logic value of the SRAM. According to [13], the secondary node is mentioned as the critical node-pair. For evaluating the critical node-pair, different current sources are employed to deposit the charge on both nodes simultaneously.

1) When the radiation particle (a positive transient pulse) injects the Q node of the proposed RHIRS-12T radiation-hardened SRAM cell, its initial stored logic value alters from '0' to '1'. This causes the P1 and P3 transistors to turn OFF temporarily, and the node QB will alter its original logic value, i.e., from '1' to '0'. Nodes S1 and S0 will remain in their original logic state because N1 and N2 transistors are stronger than P4 and P3 transistors. Therefore, as illustrated in Fig. 7(a), the node Q will be carried downward to its original logic value '0'.
2) When the radiation particle i.e., a negative transient pulse injects the QB storage node only, this alter its original logic state i.e., from '1' to '0'. It causes P2 and P4 transistors to be temporarily turned ON, and the node Q will alter its initial stored logic value from '0' to '1'. The width of the N3 NMOS transistor is larger than the width of the P4 PMOS transistor, due to this the S1 node keeps its original stored logic value i.e., '0'. Similarly, the S0 node remains its initial stored logic value i.e., '1' [16]. As illustrated in Fig. 7(b), the logic state of node Q will eventually be lowered to the logic value '0', after which the logic value of QB node is raised to the logic value '1'.
3) When a positive transient pulse injects the node S0, this flips its original stored logic state from '1' to '0'. It causes N1 and N4 transistors to be turned OFF temporarily. According to the physical mechanism study of SEU, the S0 node has a connection with P3, N2, and N4 transistors. As reported by earlier studies [17], an OFF-state NMOS transistor will only suffer a negative transient pulse if hitting a heavy ion. This means that the S0 node will experience a transient pulse of type "1 → 0" while S1 will experience a transient pulse of type "0 → 0" as illustrated in Fig. 7(c). These two transient pulses will not have an impact on other storage nodes because of the capacity effect. The proposed RHIRS-12T radiation-hardened SRAM cell as illustrated in Fig. 2 has no sensitive nodes for both S0 and S1 nodes due to this polarity reversal effect.

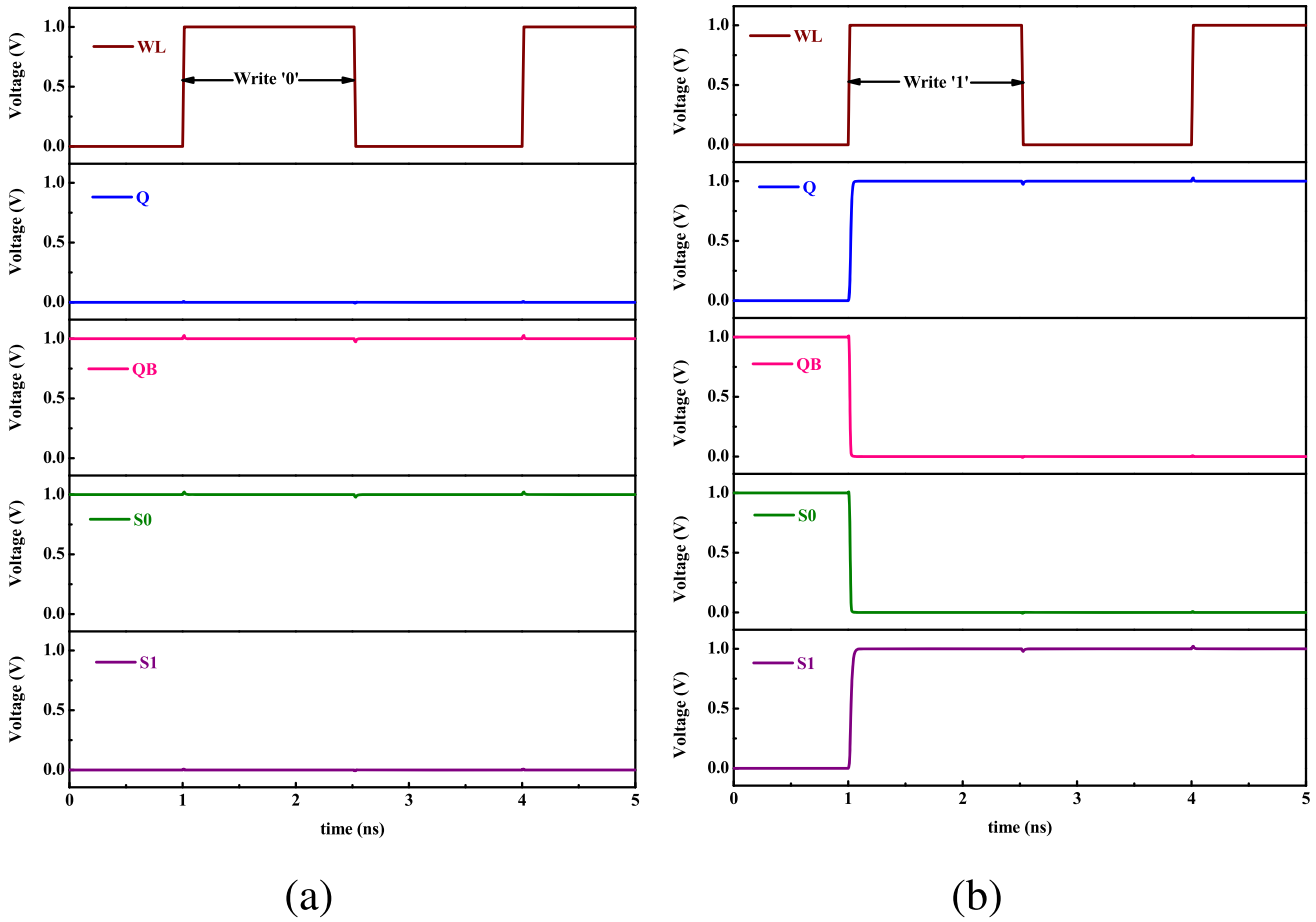


Fig. 5 Simulation waveforms of the proposed RHIRS-12T radiation-hardened SRAM cell during (a) write '0', and (b) write '1' operations

4) When a SEME happens at the internal node-pair Q-QB causes Q changes from its original stored logic '0' to logic '1', and QB changes from its original stored logic '1' to logic '0'. This causes P1 and P3 transistors to be switched OFF and P2 and P4 transistors to be turned ON temporarily. Only an external trigger, such as an operation to write, can alter the S0-S1 storage nodes, which represent the outputs of a cross-coupled latch [18]. Therefore the logic states of the S0-S1 nodes are preserved, and the transistors N1/N2 stay in their respective states (ON/OFF). This indicates that until a particular trigger occurs, the data stored in the latch remains unaltered. When Q eventually returns to '0', P1 and P3 are activated, and QB becomes '1'. The Q and the QB nodes, as seen in Fig. 7(d), both return to their initial logic states as a result.

The recovery study outlined above shows that when Q, QB, or S0 are affected by an SNU or when Q-QB are affected by an SEME, the proposed RHIRS-12T radiation-hardened SRAM cell is capable of returning its initial logic values. By doing this, the data stored inside the SRAM cell is ensured to be stable and reliable. It should be noted that after putting down a significant charge dose at Q-S0 or QB-S0 nodes, the logic values of Q/QB and node S0 can change to '1'/'0' and '0', respectively. This allows the stored data of the cell to flip. It is possible to avoid SEME, the distance across NMOS-PMOS and NMOS-NMOS transistors should be greater than or equal to 0.6 μm and 2 μm, respectively [13]. It is observed that because of charge sharing, the probability of a single ion strike affecting more than two nodes simultaneously and flipping the stored data of the cell is extremely low. The event as mentioned above occurred due to the widely dispersed radiation ion impact and the considerable charge diffusion in the storage element. This event results from radiation hitting a cell and changing its state, flipping the data that has been stored [1].

3 Evaluation of Different Parameters and Discussions

To analyze and compare the performance parameters of the proposed RHIRS-12T radiation-hardened SRAM cell

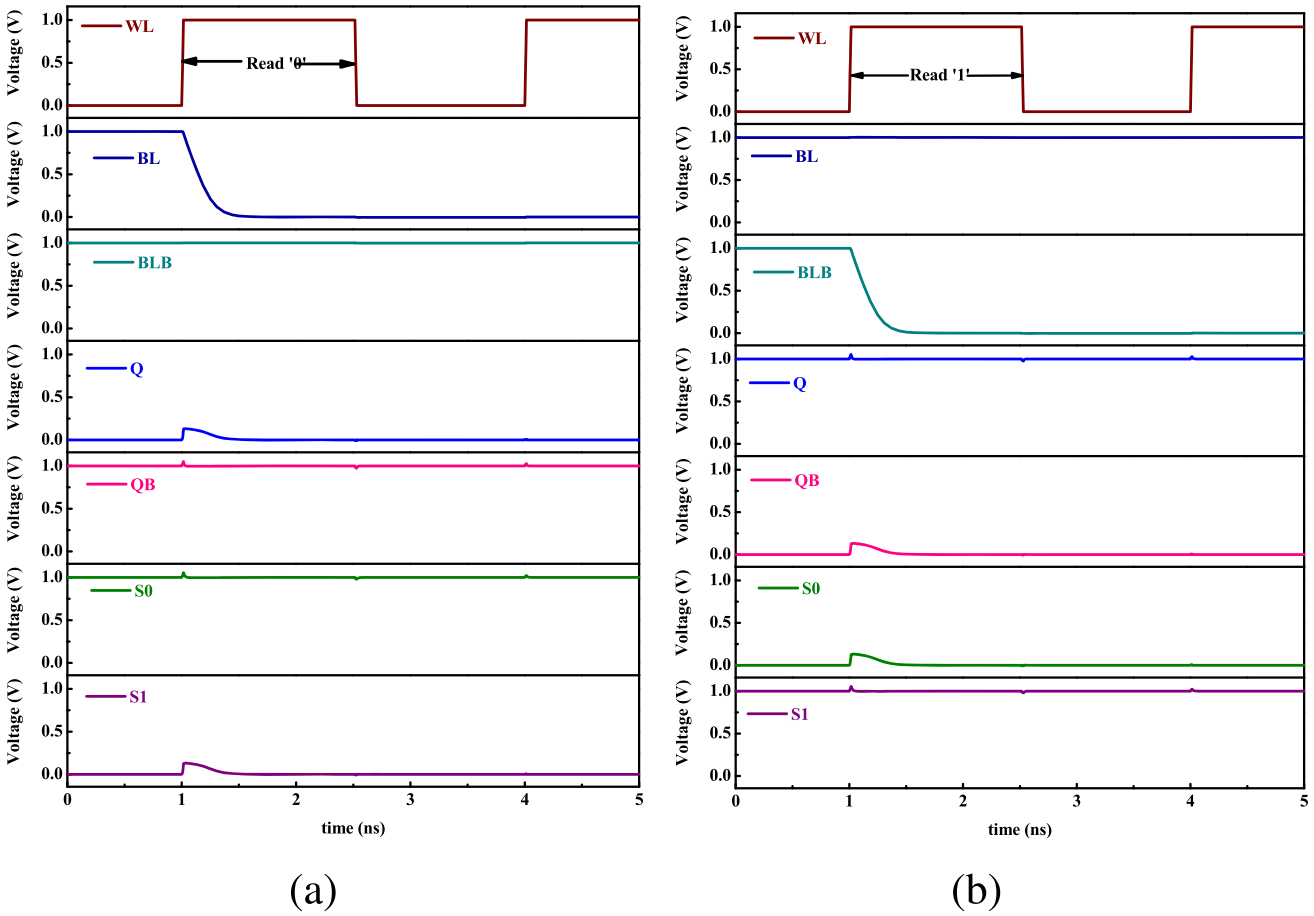


Fig. 6 Simulation waveforms of the proposed RHIRS-12T radiation-hardened SRAM cell during (a) read '0', and (b) read '1' operations

with existing radiation-hardened 12T SRAM cells, namely EDP12T [1], RHPD-12T [5], RHWC-12T [6], HPHS12T [7], RHBD12T [8], and RHD-12T [9].. With CADENCE Virtuoso, all of the SRAM cell simulations that were taken into consideration were carried out in 65-nm CMOS technology at a typical-typical (tt) process corner, temperature of 27 °C and a supply voltage of Vdd = 1 V. To establish a fair comparison, all SRAM cells with pull-up, driver, and access transistor

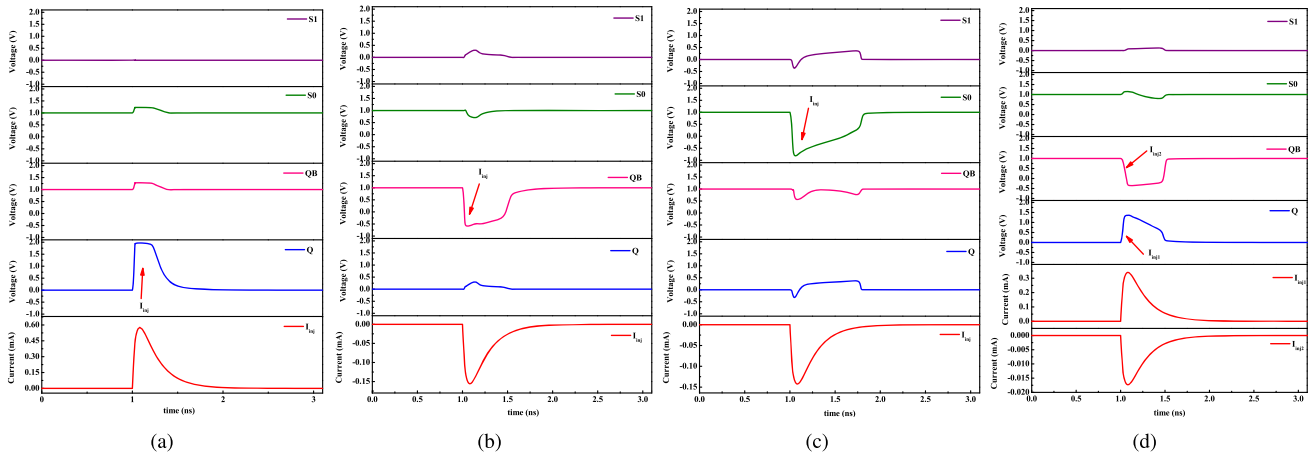


Fig. 7 Transient analysis after injecting an SEU at (a) node Q, (b) node QB, (c) node S0, and (d) node-pair Q-QB

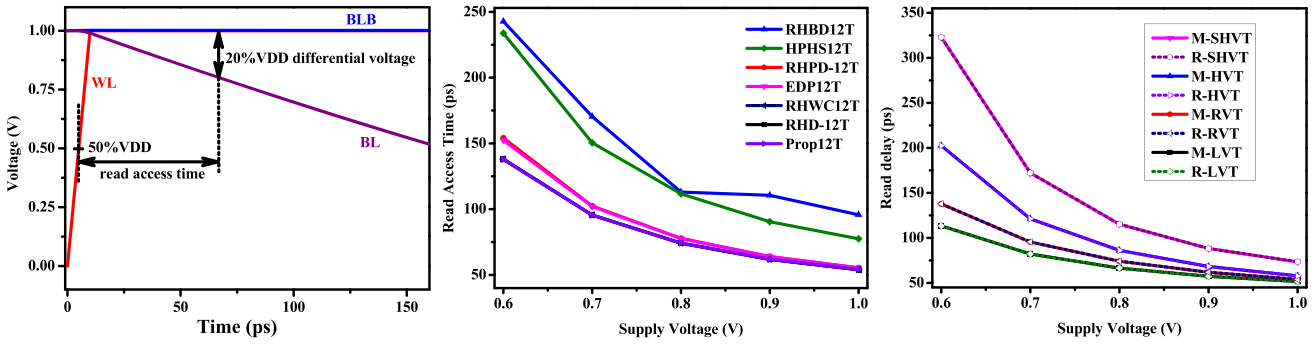


Fig. 8 (a) Calculation for read access time (T_{RA}), (b) T_{RA} Comparisons of the proposed RHIRS-12T and existing 12T SRAM cells, and (c) T_{RA} Comparisons of the proposed RHIRS-12T with RHD-12T SRAM cell by using multi-voltage transistors at different supply voltage

sizes that are the same are used [19, 20]. Additionally, we also evaluate and compare the proposed RHIRS-12T with RHD-12T SRAM cell by using multi-voltage transistors.

3.1 Analyzing and Comparing Read Delay

The time interval across the bitlines (BL and BLB) generating a 200 mV potential differential and the wordline WL reaching 50% of Vdd from its original high/low state is the read delay, also referred to as read access time (T_{RA}), as seen in Fig. 8(a). The read current and bitlines capacitance are important factors that affect read delay [13]. Figure 8(b) and (c) demonstrate T_{RA} of all evaluated SRAM cells. The supply voltage rises with a gradual reduction in T_{RA}. It implies a gradual increase in reading speed. In contrast to the other evaluated SRAM cell, EDP12T [1] contains only two access transistors. Due to this, EDP12T [1] has low bitlines capacitance and this causes shorter T_{RA} compared to most of the cells. the proposed RHIRS-12T radiation-hardened SRAM cell requires an optimized path during read operation since it has a lesser number of transistors in the feedback latch than the other SRAM cells. Therefore, the proposed RHIRS-12T radiation-hardened SRAM cell shows less T_{RA} than the other considered SRAM cells. It indicates that it can drive a read operation more effectively than other considered SRAM cells due to the corresponding pull-down transistors.

All RHD-12T SRAM cells at different voltage transistors which are expressed as R-LVT, R-RVT, R-HVT, and R-SHVT have the same read delay as the proposed RHIRS-12T SRAM cells which are represented as M-LVT, M-RVT, M-HVT, and M-SHVT, respectively due to having same reading operations as shown in Fig. 8(c). It is verified that the delay of an SRAM cell is lower for low-voltage transistors and higher for super-high voltage transistors. In contrast to the other evaluated SRAM cells, the radiation-hardened SRAM cell with low-voltage transistors (LVTs) shows less T_{RA} than the other considered SRAM cells as shown in Fig. 8(c). It indicates that it can drive a read operation more effectively than other considered SRAM cells due to the corresponding pull-down transistors.

3.2 Analyzing and Comparing Read Stability

3.2.1 Static Current Noise Margin and Static Voltage Noise Margin

An SRAM cell's stability criteria is defined by its noise margin which is calculated from N-curve [16]. By precharging BL and BLB to Vdd and enabling WL, an SRAM cell is operated into read operation, which is necessary for evaluating read stability. The N-curve for characterizing the stability during a read operation is retrieved, by monitoring the current that is externally fed into the node Q and sweeping the voltage at the '0' storage node, Q. For analyzing read stability, the N-curve provides voltage and current data [16]. Tables 2, 3 and Fig. 9(a) and (c) illustrate the N-curve comparison cells. The maximum direct current (DC), a cell can withstand without changing its originally stored data is measured by the peak current between the first two points of the N-curve, referred to as the static current noise margin (SINM). The potential difference across these two points in the N-curve provides the static voltage noise margin (SVNM) as given in Fig. 9(a)

Table 2 Comparison of SINM and SVNM from N-curve

SRAM cells	SINM (μA)	SVNM (mV)
Prop12T	**230.7**	**798.46**
EDP12T [1]	58.65	422.42
RHPD-12T [5]	144.9	676.92
RHWC12T [6]	163.5	514.42
HPHS12T [7]	56.26	652.99
RHBD12T [8]	115.1	389.14
RHD-12T [9]	163	474.41

Table 3 Comparison of SINM and SVNM from N-curve

SRAM cells	SINM (μA)	SVNM (mV)
R-LVT	163.59	453.81
R-RVT	162.43	474.41
R-HVT	154.70	515.14
R-SHVT	125.34	535.59
M-LVT	236.93	778.37
M-RVT	229.35	798.46
M-HVT	206.41	798.25
M-SHVT	159.11	778.37

and (c). The stability of the cell improves with increasing values of SVNM and SINM.

The read margins comparisons of the proposed and the existing 12T radiation-hardened SRAM cells are given in Fig. 9(b). It is important to note that the proposed RHIRS-12T radiation-hardened SRAM cell has the highest stability at the read operation even after examining the N-curve [see Fig. 9(a)], as it shows the highest SINM and SVNM than the other existing radiation-hardened 12T SRAM cells.

Similarly, the read margins comparisons of the proposed RHIRS-12T and the existing RHD-12T radiation-hardened SRAM cells are given in Fig. 9(d). It is important to note that the M-RVT radiation-hardened SRAM cell has the highest stability at the read operation even after examining the N-curve [see Fig. 9(c)], as it shows the highest SINM and SVNM than the other radiation-hardened 12T SRAM cells. It is noted that SVNM is increasing in RHD-12T with increasing voltage transistors but for the proposed RHIRS-12T cell i.e., M-RVT has a higher value of SVNM and SINM due to different storage nodes taken as consideration for measuring read stability that increases the read margin (RM) as compared to the RHD-12T SRAM cell.

3.3 Analyzing and Comparing Write Delay

The write delay or write access time (T_{WA}), is the duration of time across the Q and QB nodes crossing each other and the WL reaching 50% of Vdd in its rising edge. The duration

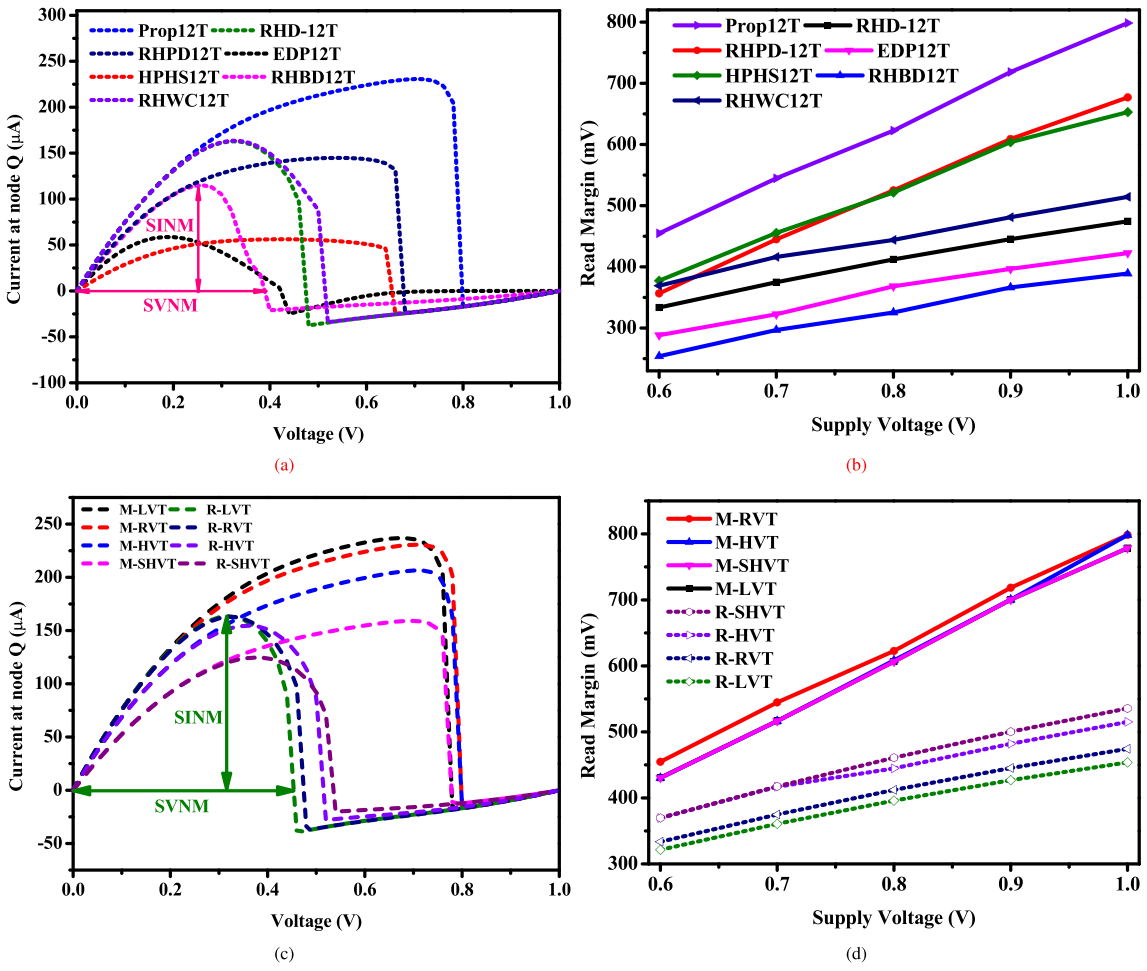


Fig. 9 (a), (c) Estimation of SINM and SVNM from N-curve, and (b), (d) Read margin comparison at different supply voltage

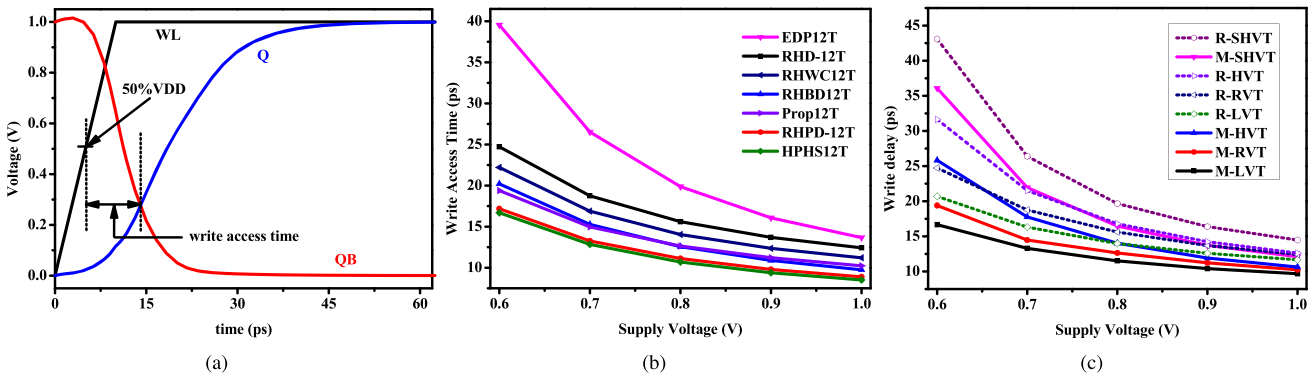


Fig. 10 (a) Calculation for write access time, (b), and (c) Write access time (T_{WA}) comparisons at different supply voltages

of this time is seen in Fig. 10(a), (b) and (c) demonstrate the write delay for all radiation-hardened 12T SRAM cells at various supply voltages. The SRAM cells under consideration, namely EDP12T [1], RHD-12T [9], RHWC12T [6], and RHBD12T [8], exhibit longer feedback paths for altering the originally stored data, demonstrating higher T_{WA}. The two pairs of access transistors are connected to the storage nodes of the HPHS12T [7], RHPD-12T [5], and the proposed RHIRS-12T radiation-hardened SRAM cell to change the stored data simultaneously. Hence, they exhibit a lower T_{WA}. It indicates that their access transistors provide a stronger operating capacity during write operation to change the data that is stored at their storage nodes.

In Fig. 10(c), it shows that the proposed RHIRS-12T cell has lower T_{WA} than the RHD-12T cell at different voltage transistors. The RHD-12T [9] exhibits longer feedback paths for altering the originally stored data, demonstrating higher T_{WA}. The two pairs of access transistors are connected to the storage nodes of the proposed RHIRS-12T radiation-hardened SRAM cell to change the stored data simultaneously. Hence, they exhibit a lower T_{WA}. It indicates that their access transistors provide a stronger operating capacity to change the data stored at their storage nodes during write operation.

3.4 Analyzing and Comparing Write Ability

A far more accurate technique for assessing the write capacity of an SRAM is to measure the word line write trip voltage (WWTV), confirming recent research [13]. According to [13], it is calculated as the potential difference between the supply voltage (Vdd) and wordline (WL) at the intersection of storage nodes Q and QB. WWTV is measured by first loading the data that is desired onto the bitlines and then gradually increasing the WL voltage. Figure 11 illustrates the WWTV comparisons of all considered radiation-hardened 12T SRAM cells under various supply voltages. The results from the Fig. 11(a) demonstrate that the proposed RHIRS-12T radiation-hardened SRAM cell shows a higher WWTV

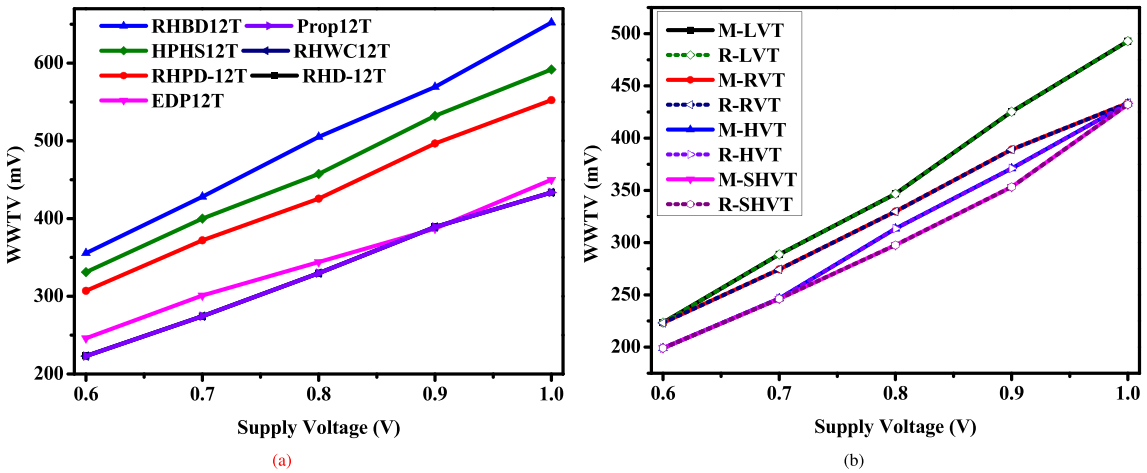


Fig. 11 Word line write trip voltage (WWTV) comparisons of (a) the various radiation-hardened 12T SRAM cells, and (b) the proposed RHIRS-12T with RHD-12T SRAM cell by using multi-voltage transistors

than RHWC12T [6] and RHD-12T [9]. It indicates that it has stronger write stability than RHWC12T [6] and RHD-12T [9], respectively. In the positive feedback path, RHBD12T [8] has more numbers of PMOS transistors than the other considered 12T SRAM cells. Consequently, in comparison to other SRAM cells, it exhibits a higher WWTV. Similarly, from Fig. 11(b), the results show that an SRAM cell with low-voltage transistors (LVTs) has a high value of WWTV as compared to an SRAM cell having high-voltage transistors (HVT). It indicates that an SRAM cell by using LVTs has stronger write stability.

Additionally, the simulations for stability were performed at different process corners such as slow NMOS-fast PMOS (SF), fast NMOS-slow PMOS (FS), typical-typical (TT), slow NMOS-slow PMOS (SS), and fast NMOS-fast PMOS (FF) to find the worst process corner during read and write operations at room temperature (27°C) and nominal supply voltage (1 V). The proposed RHIRS-12T and RHD-12T radiation-hardened SRAM cells are compared for WWTV, and RM is given in Fig. 12(a), (b),(c) and (d), respectively. The SF and the FS are the worst process corners for write and read stability, respectively, (see Fig. 12).

3.5 Hold Stability and Hold Power Comparison

Figure 13 shows the hold margin (HM) of all considered SRAM cells at various supply voltages. The hold stability is calculated from the N-curve method [16] as discussed in the read stability subsection. For estimating the hold margin, the bitlines, BL, and BLB are precharged to Vdd, and wordlines, WL are connected to a lower supply voltage (gnd), during hold mode. The RHBD12T [8] cell has a lower HM than the other SRAM cells, which implies weaker hold stability. In contrast, the proposed RHIRS-12T radiation-hardened SRAM cell shows higher HM at different supply voltages, indicating better hold stability than the

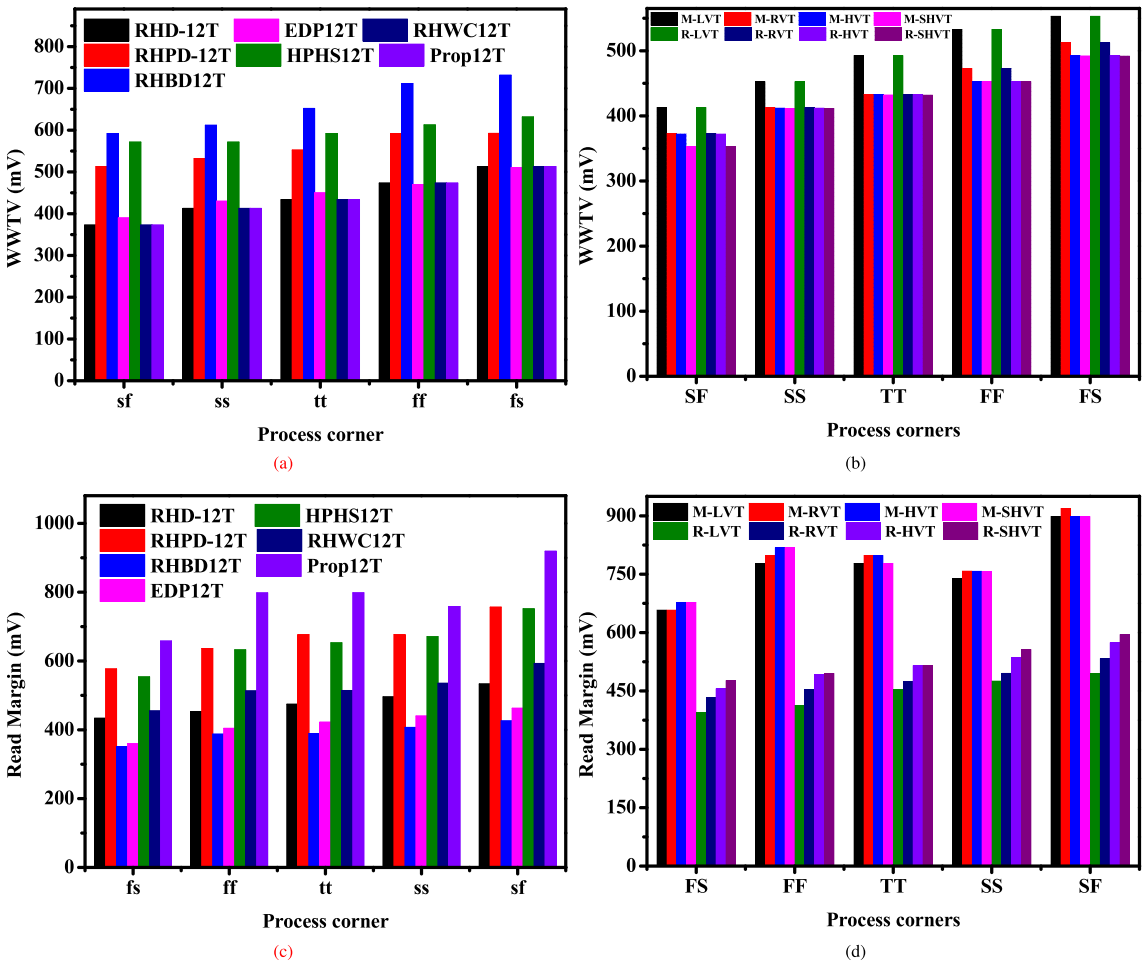


Fig. 12 (a), (b) Word line write trip voltage (WWTV), (c), and (d) Read margin comparison of proposed radiation-hardened 12T and considered SRAM cells at different process corners

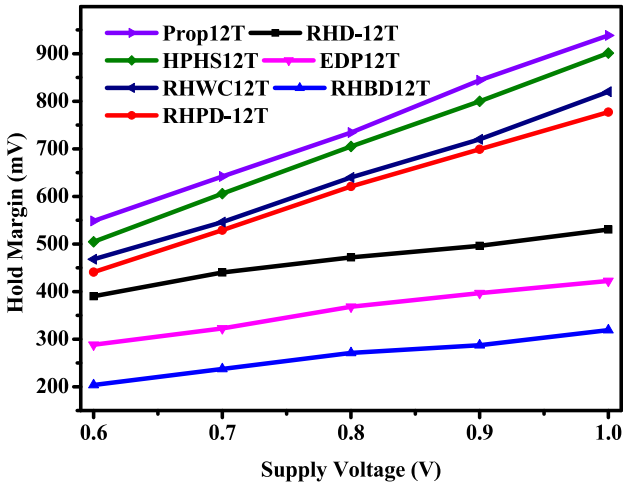


Fig. 13 Hold margin comparison of various SRAM cells

earlier reported radiation-hardened 12T SRAM cells that have been examined.

Figure 14 represents power dissipation during the hold state. By varying the supply voltage (Vdd) from 0.6 V to 1.0 V at room temperature (27 °C), the holding power (H_{PWR}) is measured for all considered SRAM cells. Bitline leakage and inverter leakage are the main causes of H_{PWR} consumption. RHBD12T sources less current from Vdd compared to other considered SRAM cells due to only two PMOS transistors being connected to Vdd in RHBD12T [8]. Thus, RHBD12T [8] consumes less power during hold mode. Since RHPD-12T [5], RHWC12T [6], RHD-12T [9], and the proposed RHIRS-12T radiation-hardened SRAM cells have less number of transistors in stacking. As a result, they dissipate higher H_{PWR} compared to HPHS12T [7].

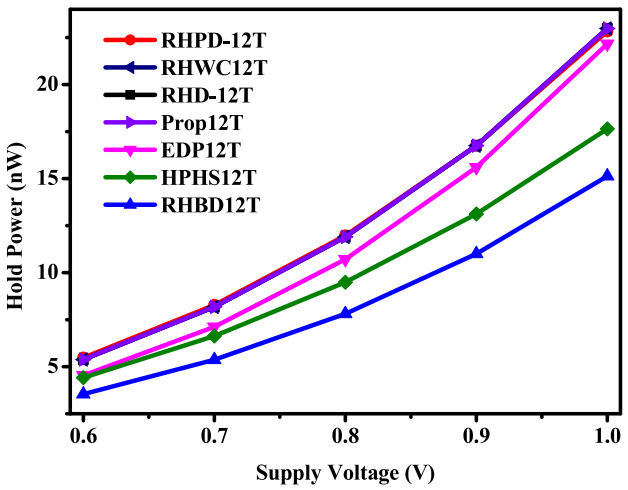


Fig. 14 Hold power comparison of the proposed radiation-hardened 12T with all the existing SRAM cells under various supply voltages

3.6 Analyzing and Comparing of Energy Consumption

In an SRAM cell, dynamic power is divided into two parts: write and read power. In the case of a write operation, the voltage swing on the bitlines must be fully utilized, whereas, in a read operation, it is limited to a lower value [1]. Consequently, compared to the reading process, writing operations use considerably more power. With the scaling of supply voltage, dynamic power consumption decreases, and the delay increases in an SRAM cell. Due to this, the battery life has been affected. It is noticed to consider the consumption of energy per read/write cycle for all of the SRAM cells.

3.6.1 Read Energy Comparisons

Figure 15 illustrates the energy consumption of all the considered radiation-hardened 12T SRAM cells under various supply voltages during the read operation. EDP12T [1] consists of a single access transistor corresponding to each bitline, due to this capacitance of bitline is lower. This causes less energy consumption than the other evaluated SRAM cells under read operation. Furthermore, this cell requires less dynamic power compared to other SRAM cells. All radiation-hardened 12T SRAM cells, except EDP12T [1], exhibit larger bitlines capacitance. RHBD12T [8] consumes high energy during read operation since it consumes high dynamic power and high T_{RA} than other SRAM cells. The proposed RHIRS-12T radiation-hardened SRAM cell has lower T_{RA} and consumes less dynamic power. Therefore, it consumes the least energy than the other considered SRAM cells during a read operation (see Fig. 15(a)). From the simulation results, an SRAM cell consisting of low-voltage transistors (LVTs) has less delay and consumes high power during the read operation. It means the delay increases and the leakage power decreases from a low-voltage transistor (LVT) to a high-voltage transistor (HVT) SRAM cell during read operation. Thus, the multiplication of delay and power referred to as energy increases of an SRAM from a low-voltage transistor to a high-voltage transistor during a read operation (see Fig. 15(b)).

3.6.2 Write Energy Comparisons

The energy consumption of different radiation-hardened 12T SRAM cells during write operation at various supply voltages is given in Fig. 16. EDP12T [1] consumes high dynamic power and high T_{WA} compared to the other SRAM cells. Thus, EDP12T [1] consumes higher energy during the write operation. HPHS12T [7] and RHPD-12T [5] have lower T_{WA} and lower dynamic power consumption than the other SRAM cells. Thus, they have lower energy consumption

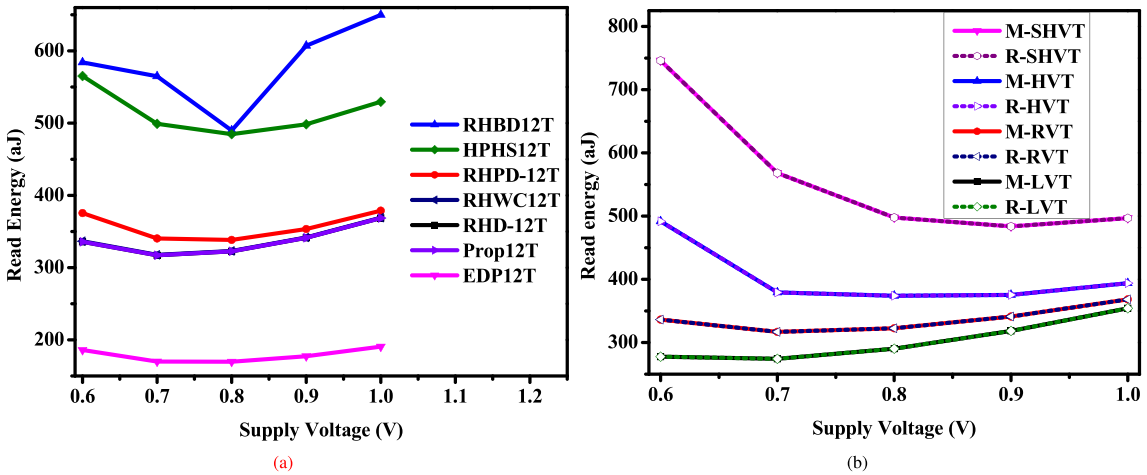


Fig. 15 Read energy comparison of (a) all the considered radiation-hardened 12T SRAM cells, and (b) the proposed RHIRS-12T with RHD-12T SRAM cell by using multi-voltage transistors under various supply voltages

during write operations. Similarly, the proposed RHIRS-12T radiation-hardened SRAM cell consumes less energy since it has a low T_{WA} and dissipates less dynamic power compared to the RHD-12T [9], and RHWC12T [6]. The proposed RHIRS-12T radiation-hardened SRAM cell has less T_{WA} and consumed high dynamic power compared to RHBD12T [8]. Therefore, it requires more energy than RHBD12T [8] during the write operation.

It is noted that the delay of a proposed RHIRS-12T and RHD-12T SRAM cell is different during write operation but the leakage power consumption is the same for an SRAM cell having the same voltage transistors. Therefore, energy consumption differs for a proposed RHIRS-12T and RHD-12T SRAM cell. The results state that the energy consumption of an SRAM cell with LVT and RVT increases corresponding to supply voltage increases.

Table 4 presents the performance comparison of radiation-hardened 12T SRAM cells having different voltage transistors at Vdd = 1V. It provides a detailed analysis of the relative overheads such as read access time (T_{RA}), write access time (T_{WA}), write energy (E_{write}), read energy (E_{read}), and readability. The relative write access times between the proposed RHIRS-12T and RHD-12T SRAM cells are calculated and shown in the ΔT_{WA} column. Similarly, we can interpret the meaning of the ΔE_{write}, and ΔRM. Δ is defined as [2, 8]

$$\Delta = (\text{compared cell} - \text{proposed cell})/\text{proposed cell}. \quad (1)$$

We have observed from the result analysis that the proposed RHIRS-12T radiation-hardened SRAM cell has the highest read stability compared with RHD-12T with different voltage transistors SRAM cells during the read operation. The proposed RHIRS-12T radiation-hardened SRAM cell has improvements of 71.52%, 68.31%, 54.96%, and 45.33% in read margin value compared with respective different voltage transistors of RHD-12T i.e., R-LVT, R-RVT, R-HVT, and R-SHVT SRAM cell respectively, during the read operation. It indicates that the proposed RHIRS-12T SRAM cell has the highest improvement in read stability compared to RHD-12T consisting of LVTs. It means the proposed RHIRS-12T can be used as low-voltage applications for having higher improved read stability. It is faster at 20.68%, 21.41%, 18.83%, 19.59% and it also saves 20.69%, 21.44%, 17.89, 18.58% energy compared with respective different voltage transistors of RHD-12T i.e., R-LVT, R-RVT, R-HVT, and R-SHVT SRAM cell respectively, during the write operation (see Table 4).

From the Table 5, the proposed RHIRS-12T radiation-hardened SRAM cell has the lowest read delay during a read operation. It exhibits improvements of 33.63%, 21.41%, and 9.58% in write access time compared to EDP12T [1], RHD-12T [9], and RHWC12T [6], respectively. The proposed RHIRS-12T SRAM cell saves 76.34%, 43.68%, 2.77%, and 0.13% energy consumption compared with RHBD12T [8], HPHS12T [7], RHPD-12T [5], and RHWC12T [6], respectively, during the read operation. It also saves 55.59%, 21.44%, and 6.04% energy compared with EDP12T [1], RHD-12T [9], and RHWC12T [6], respectively, during the write operation.

Similarly, Table 6 represents a comparison analysis of various parameters such as writing ability, read stability, hold stability, and critical charge. We observed from the result analysis that the proposed RHIRS-12T radiation-hardened SRAM cell has the highest read and hold stability compared with other SRAM cells during the read, and the hold operations, respectively. The proposed RHIRS-12T

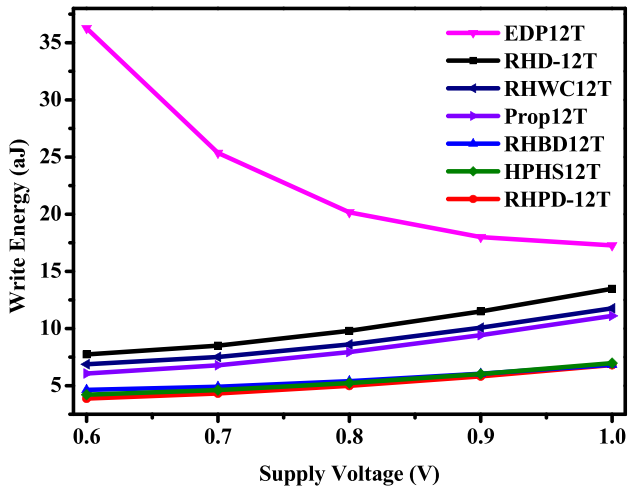


Fig. 16 Write energy comparison of (a) all the considered radiation-hardened 12T SRAM cells, and (b) the proposed RHIRS-12T with RHD-12T cell by using multi-voltage transistors under various supply voltages

radiation-hardened SRAM cell has the highest critical charge value compared with other existing 12T SRAM cells except EDP12T [1]. A detailed discussion of critical charge is explained in the next subsection.

3.7 Comparing all the Radiation-Hardened 12T SRAM Cells Through Statistical Analysis

During the fabrication process, the alterable properties of the transistor, like the oxide thickness, channel width, and channel length, can change. The statistical variation in a design parameter can be evaluated through a computational technique described as Monte Carlo (MC) Simulation [8]. To help designers evaluate the variation and make sensible decisions about design changes, MC Simulation provides the mean (μ) value and standard deviation (σ) value. Foundry companies provide MC Simulation model files, which enable designers to analyze output variances and adjust their designs accordingly [21]. According to the MC simulations, the proposed and other radiation-hardened 12T SRAM cells have been demonstrated to be stable during the read and write operations, as indicated in Tables 7 and 8 at typical-typical (tt) process corner, nominal supply voltage (Vdd = 1V), and room temperature (27 °C).

3.8 Soft-Error Robustness Analysis

The circuit output value is altered with a significant quantity of current flowing in it, as an outcome of radiation striking vulnerable nodes, or the drain area of NMOS and PMOS, as illustrated in Ahirwar et al. [15]. It causes the generation of a transient current pulse that resembles a double exponential (DE) function. The rapid increase and gradual decrease are characteristics of this transient current. In SPICE, the DE current pulse expression [1], $I_{inj}(t)$, is described as

$$I_{\text{inj}}(t) = I_0 \left(e^{\frac{-t}{\tau_\alpha}} - e^{\frac{-t}{\tau_\beta}} \right) \tag{2}$$

$$Q_{cr} = \int_0^{T_{cr}} I_{\text{inj}}(t)\, dt, \tag{3}$$

Where Q_{cr} is the minimum charge or critical charge required to upset its initial stored value at a sensitive node, and τ_α (50 ps) and τ_β (200 ps) are the collection time constant of the p-n junction and the time constant of ion-track formation, respectively [6]. Therefore, circuits are more susceptible to radiation threats at lower functioning voltages. We determine which node has the lowest critical charge by evaluating each one to obtain this. In this article, the $I_{inj}(t)$ during the time interval 0 to critical time (T_{cr}) is integrated to get the critical charge (Q_{cr}). The basic simulation flow graph and calculation for a Q_{cr} of all the considered radiation-hardened 12T SRAM cells are shown in Figs. 17 and 18, respectively.

The effective Q_{cr} of each considered cell is illustrated in Fig. 19(a). It demonstrates that the proposed RHIRS-12T radiation-hardened SRAM cell is the most radiation tolerant compared with the other existing SRAM cells except EDP12T. The effective Q_{cr} of the proposed RHIRS-12T and RHD-12T SRAM cell consisting of multi-voltage transistors is illustrated in Fig. 19(b). It demonstrates that the proposed RHIRS-12T and the RHD-12T radiation-hardened SRAM cell have the same radiation tolerance. It is noted from

Table 4 Parameters comparison of the proposed RHIRS-12T and RHD-12T SRAM cells consisting of multi-voltage transistors

SRAM cells	T_{WA} (ps)	ΔT_{WA} (%)	P_{WA} (μW)	T_{RA} (ps)	P_{RA} (μW)	E_{write} (aJ)	ΔE_{write} (%)	E_{read} (aJ)	RM (mV)	ΔRM (%)
R-LVT	11.67	**20.68**	1.11	51.56	6.87	12.95	**20.69**	354.22	453.81	**71.52**
M-LVT	9.67	–	1.11	51.56	6.87	10.73	–	354.22	778.36	–
R-RVT	12.42	**21.41**	1.09	53.94	6.83	13.54	**21.44**	368.41	474.41	**68.31**
M-RVT	10.23	–	1.09	53.94	6.83	11.15	–	368.41	798.46	–
R-HVT	12.62	**18.83**	1.01	57.84	6.81	12.65	**17.89**	393.89	515.14	**54.96**
M-HVT	10.62	–	1.01	57.84	6.81	10.73	–	393.89	798.25	–
R-SHVT	14.47	**19.59**	0.93	73.38	6.78	13.34	**18.58**	496.78	535.59	**45.33**
M-SHVT	12.10	–	0.93	73.38	6.78	11.25	–	496.78	778.37	–

For differentiate the proposed work and other related works

Table 5 Parameters comparison of the proposed RHIRS-12T with existing radiation-hardened 12T SRAM cells at nominal supply voltage

SRAM cells	T_{WA} (ps)	ΔT_{WA} (%)	T_{RA} (ps)	ΔT_{RA} (%)	E_{write} (aJ)	ΔE_{write} (%)	E_{read} (aJ)	ΔE_{read} (%)
Prop12T	**10.23**	–	**53.94**	–	**11.10**	–	**368.59**	–
EDP12T [1]	13.67	33.63	55.41	2.73	17.27	55.59	190.67	−48.27
RHPD-12T [5]	8.89	−13.09	55.38	2.67	6.81	−38.65	378.81	2.77
RHWC12T [6]	11.21	9.58	53.98	0.07	11.77	6.04	369.08	0.13
HPHS12T [7]	8.51	−16.81	77.52	43.72	6.97	−37.21	529.60	43.68
RHBD12T [8]	9.75	−4.69	95.74	77.49	6.84	−38.38	649.95	76.34
RHD-12T [9]	12.42	21.41	53.94	0	13.48	21.44	368.57	−0.01

For differentiate the proposed work and other related works

Table 6 Parameters comparison of the proposed RHIRS-12T with existing radiation-hardened 12T SRAM cells at nominal supply voltage

SRAM cells	Q_{cr} (fC)	ΔQ_{cr} (%)	WWTV (mV)	ΔWWTV (%)	RM (mV)	ΔRM (%)	HM (mV)	ΔHM (%)
Prop12T	**16.36**	–	**444.8**	–	**797.9**	–	**938.5**	–
EDP12T [1]	17.63	−7.76	449.2	−0.99	422.4	47.06	422.4	54.99
RHPD-12T [5]	13.07	20.11	561.0	−26.12	674.6	15.45	777.2	17.19
RHWC12T [6]	9.02	44.87	444.9	−0.02	520	34.83	820	12.63
HPHS12T [7]	6.37	61.06	595.6	−33.90	663.1	16.89	879.1	6.33
RHBD12T [8]	3.51	78.55	659.2	−48.20	395.4	50.45	319.1	66
RHD-12T [9]	16.34	0.12	444.6	0.04	469.8	41.12	530.4	43.49

For differentiate the proposed work and other related works

Table 7 Statistical analysis of the proposed RHIRS-12T with the existing radiation-hardened 12T SRAM cells

SRAM Cells	WWTV			RM		
	μ (mV)	σ (mV)	σ/μ	μ (mV)	σ (mV)	σ/μ
Prop12T	**444.8**	**42.98**	**0.097**	**797.9**	**60.80**	**0.076**
EDP12T [1]	449.2	42.61	0.095	428.9	26.74	0.062
RHPD-12T [5]	561.0	33.25	0.059	674.6	58.99	0.087
RHWC12T [6]	444.9	42.43	0.095	520	42.23	0.081
HPHS12T [7]	595.6	28.89	0.049	663.1	66.70	0.101
RHBD12T [8]	659.2	43.15	0.065	395.4	30.58	0.077
RHD-12T [9]	444.6	43.31	0.097	469.8	37.20	0.079

For differentiate the proposed work and other related works

Table 8 Statistical analysis of the proposed RHIRS-12T and RHD-12T SRAM cells consisting of multi-voltage transistors

SRAM cells	WWTV			RM		
	μ (mV)	σ (mV)	σ/μ	μ (mV)	σ (mV)	σ/μ
R-LVT	488.39	41.52	0.085	445.62	34.83	0.078
M-LVT	488.56	40.94	0.084	778.16	62.51	0.083
R-RVT	444.64	43.31	0.097	469.83	37.20	0.079
M-RVT	444.85	42.98	0.096	797.9	60.80	0.076
R-HVT	439.33	54.18	0.123	507.23	48.37	0.095
M-HVT	439.53	54.57	0.124	786.65	68.16	0.087
R-SHVT	427.98	41.89	0.098	529.34	35.03	0.066
M-SHVT	428.04	41.42	0.096	779.74	57.70	0.074

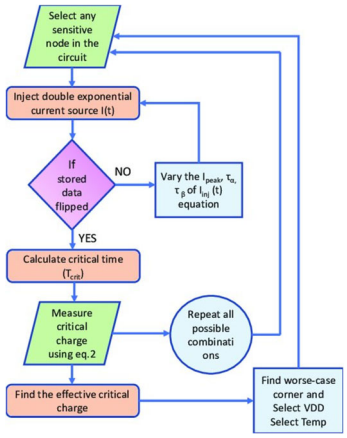


Fig. 17 Simulation flow chart for calculating the critical charge of an SRAM cell [22]

the results that a SEU introduced on an SRAM cell having super high-voltage transistors (SHVT) has a higher value of critical charge. This means an SRAM cell that consists of SHVT has more radiation tolerance than the other SRAM cells for SEU, but it has less radiation tolerance for SEME. Figure 20 represents the process, voltage, and temperature (PVT) variations of the proposed RHIRS-12T (M-RVT) radiation-hardened SRAM cell on I_0, T_{cr}, and Q_{cr}. The simulation results indicate that the Q_{cr} increases with the supply voltage increments. One thousand MC simulations of the proposed RHIRS-12T (M-RVT) radiation-hardened SRAM cell given in Fig. 21 have verified the recovery from SEUs and SEME.

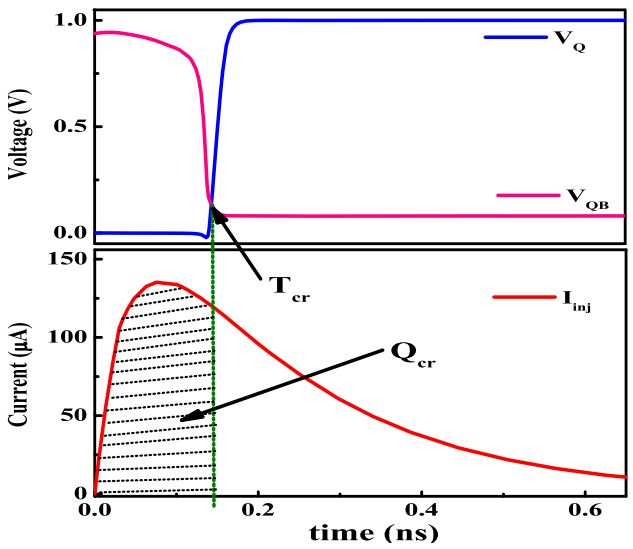
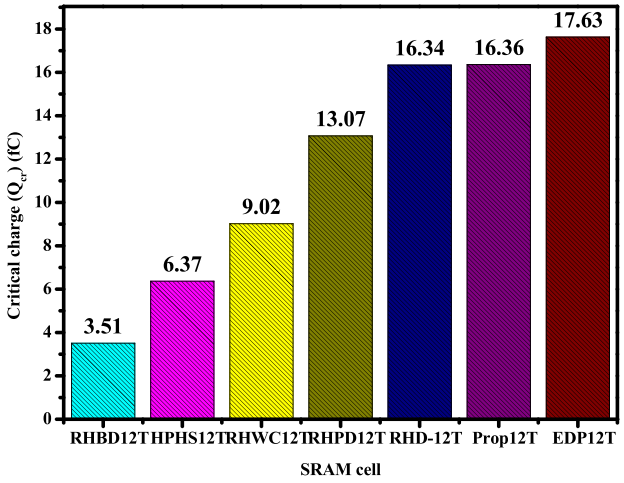
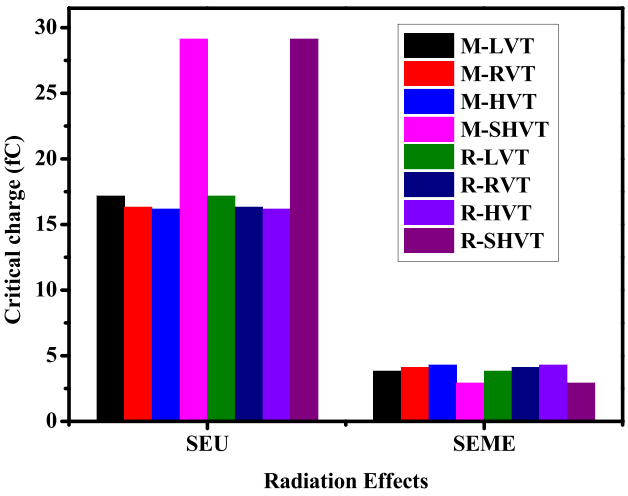


Fig. 18 Estimation of critical charge for an SRAM cell



(a)

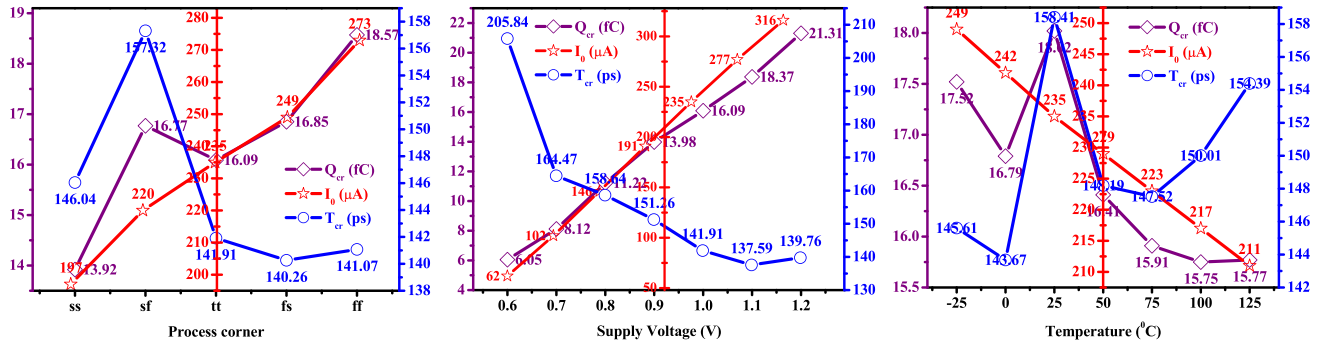


(b)

Fig. 19 Comparison of Q_{cr} of all the considered radiation-hardened 12T SRAM cells

3.9 Radiation-Hardened 12T SRAM Cells Overall Performance

In the previous sections, we evaluated and compared many essential design features between the proposed radiation-hardened SRAM cell and other radiation-hardened 12T SRAM cells. It is necessary to note that the parameters for the design of an SRAM cell are fundamentally conflicting. In this instance, if the supply voltage (Vdd) is enhanced improvements in hold stability (HM), read stability (RM), write stability (WWTV), Q_{cr}, and delay during write and read operations can all be accomplished at the expense of higher power and energy consumption. Introducing the wider transistors is another option to increase Q_{cr}, which will increase the area overhead. In basics, a design parameter will



(a) (b) (c)

Fig. 20 Transient analysis of the proposed RHIRS-12T SRAM cell after an SEU injection at (a) process corner, (b) supply voltage, and (c) temperature variations

be required to determine the total performance of an SRAM cell. It is achieved through the use of an electrical quality metric (EQM), which may measure the total performance of an SRAM cell and is described in Pal et al. [18]:

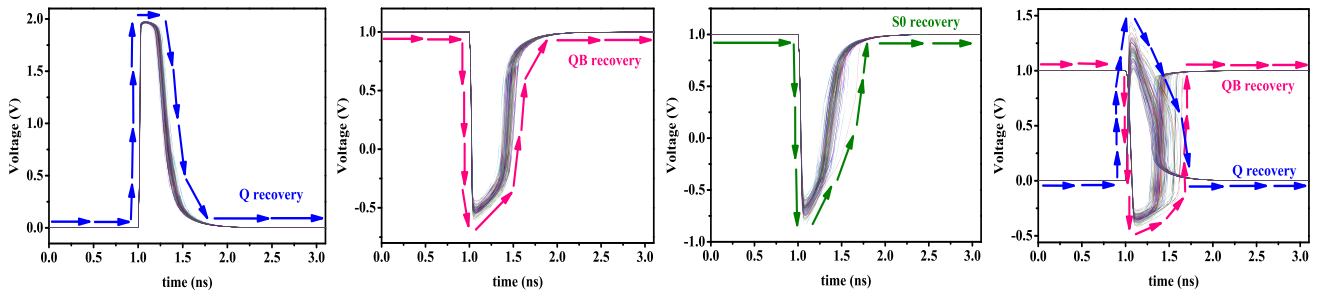
$$EQM = \frac{Q_{\text{cr}} \times \text{RM} \times \text{HM} \times \text{WWTV}}{E_{\text{READ}} \times E_{\text{WRITE}} \times H_{\text{PWR}}}. \tag{4}$$

An SRAM cell with a higher EQM has improved total performance. The relative EQM values for the radiation-hardened 12T SRAM cell presented in Fig. 22 indicate that the proposed RHIRS-12T radiation-hardened SRAM cell has the highest EQM, demonstrating its improved performance. Thus, the radiation-hardened 12T SRAM cell that has been proposed can be applied in aerospace.

4 Discussion and Conclusion

This research paper proposes a radiation-hardened 12T SRAM cell. It can recover its initial stored data at its storage nodes, even if a radiation strike flips the node logic values. Moreover, it also regains from single-event-multiple-effect at its node-pair. It exhibits the highest read stability and hold stability among all existing radiation-hardened 12T SRAM cells. Compared with the other radiation-hardened SRAM cells, the proposed RHIRS-12T radiation-hardened SRAM cell consumes the least delay and energy during read operations, and it also saves energy compared with most of the existing SRAM cells during the write operations. Because of its enhanced overall performance, the proposed RHIRS-12T radiation-hardened SRAM cell is more suitable for SRAM designs that require high reliability.

Additionally, this research paper investigates the proposed RHIRS-12T SRAM cell with different voltage transistors. Using multi-voltage transistors, we evaluated and compared the proposed RHIRS-12T with RHD-12T radiation-hardened SRAM cells. The proposed RHIRS-12T exhibits less write delay and consumes less energy compared to RHD-12T SRAM cell during the write operation. The proposed RHIRS-12T exhibits the highest improvement in read stability at low-voltage transistor compared to RHD-12T SRAM cell. It indicates that the proposed RHIRS-12T SRAM cell can be used for low voltage applications. The proposed RHIRS-12T radiation-hardened SRAM cell offers a decent compromise between circuit performance and radiation robustness. Therefore, it can be suitable for aerospace applications.



(a) (b) (c) (d)

Fig. 21 Voltage response of (a) node Q, (b) node QB, (c) node S0, and (d) node-pair Q-QB after MC simulation

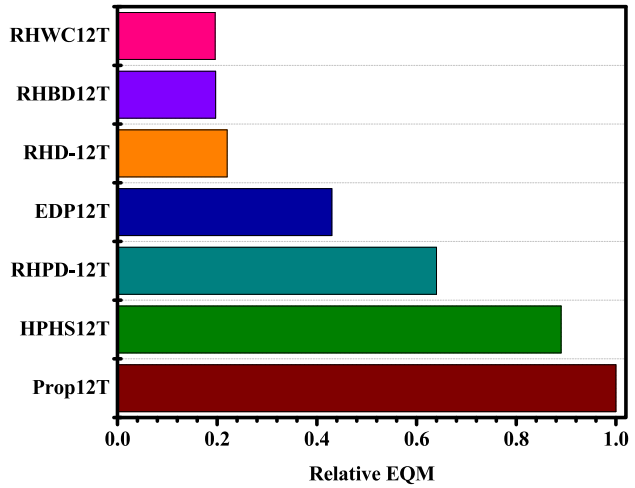


Fig. 22 Relative EQM comparison for various radiation-hardened 12T SRAM cells

Author Contributions Rachana Ahirwar: Conception and design, or result analysis, Interpretation of the data, Investigation, Methodology, Software, Validation, Visualization, Writing - original draft, Writing - review & editing. Prof. Manisha Pattanaik: Project administration, Resources, Software, Supervision, Writing - review & editing. Prof. Pankaj Srivastava: Project administration, Supervision, Writing - review & editing.

Funding Not applicable.

Availability of Data and Materials Not applicable.

Declarations

Ethics Approval Not applicable.

Consent for Publication Not applicable.

Consent for Participate Not applicable.

Competing Interests The authors declare that they have no competing interests.

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