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RESEARCH

Test Modules for Enhanced Testability of Single Flux Quantum Integrated Circuits

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Abstract
On-chip testability of superconductive electronic circuits is challenging due to the high clock frequencies and cryogenic environment, which in turn complicates the test/debug process. In this paper, circuit solutions to support design for testability (DFT) in single flux quantum (SFQ) systems are proposed. Two test modules, a test extraction module and a hybrid test module, are presented to enhance the controllability and observability of the internal nodes within SFQ systems. These test modules are validated on several benchmark circuits. A methodology is further proposed to explore tradeoffs (power, delay, area, and detection speed) of the modules. Additionally, controllability and observability testability measures are proposed. This methodology can be used to determine the quantity, type, location, and overhead of the proposed test modules to enhance DFT in SFQ systems with the fewest number of test vectors and highest possible fault coverage.

Keywords Design for testability (DFT) · Single flux quantum (SFQ) · Superconductive integrated circuits · Superconductive digital electronics

1 Introduction

Superconductive electronics is a promising technology with important characteristics, such as low energy per operation [1], lossless interconnects at DC, zero static power, operation at clock frequencies exceeding 100 GHz [2], and a natural interface with quantum computing systems [3]. Single flux quantum (SFQ) logic is a superconductive logic family for low power, high performance cryogenic computing [4–6].

Resistive SFQ (RSFQ) electronic systems are based on Josephson junctions (JJs). A JJ consists of two superconductive electrodes separated by a thin barrier. When a small voltage is applied across the junction, superconducting elctrons (Cooper pair) flow through the junctions, and the phase difference between the two superconducting electrodes changes. As the current flows, a magnetic field is generated around the junction. The magnetic field induces a magnetic flux in the junction, which becomes quantized due to the superconducting properties of the material. When the quantized magnetic flux reaches a critical value, a single fluxon is formed [5].

In RSFQ technology the existence and absence of fluxons are used to represent binary information, 0s and 1s, and are manipulated to perform digital logic operations. The ability to control and manipulate these fluxons enables these ultrafast and low-power digital circuits [1].

The complexity of SFQ circuits has reached 800,000 Josephson junctions (JJs), operating at subterahertz clock frequencies [7]. High reliability is a necessary requirement for superconductive integrated systems. The challenge of achieving high performance with high reliability is escalating due to dimensional scaling, novel materials and devices, and operation in severe conditions (extreme cryogenic temperatures and sub-terahertz frequencies).

These reliability challenges, combined with yield issues, are exacerbated by exotic manufacturing technologies. Reliability and yield can be categorized by the failure paths (sequence of faults due to a physical failure) and failure

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mechanisms (physical cause of the failure). Determining the defects and faults is essential to enhance the lifetime of superconductive systems. This capability is achieved by improving the fault coverage, where the system is evaluated to identify the characteristics of the faults, such as the quantity, location, and type.

Fault coverage is improved by exploiting design for testability (DFT) techniques to enhance the controllability and observability of the internal nodes within a system. An understanding of the physics of each failure mechanism and the development of effective and reliable algorithms that exploit these DFT techniques prior to fabrication are vital to the development of superconductive systems.

A methodology is proposed here to include DFT within SFQ systems, a topic currently in an embryonic stage. This objective is achieved by enhancing the controllability and observability of the internal nodes within an SFQ system to identify specific defects and faults. This capability can be accomplished by exploiting embedded hardware solutions such as test insertion and/or test extraction.

Several significant differences exist between conventional CMOS logic and SFQ logic. SFQ logic operates at subterahertz clock frequencies in a cryogenic environment. As previously mentioned, an SFQ signal is represented by the existence or absence of an SFQ pulse. The following additional differences prevent the use of standard CMOS-based DFT techniques [8],

1) observation of an internal node within a CMOS system is achieved by direct probing, while in SFQ systems, a test extraction module is required to non-destructively readout the signal of an internal node,
2) most (but not all) SFQ logic gates are clocked and latched within at least one storage loop, where several clock cycles are required to produce an output [9]. Additional information, such as the number of cycles, is required by a test controller.
3) limited fan-out of SFQ gates and flip flops [10]. A splitter is required to provide an additional output [10]. A test technique is proposed here to enhance the controllability and observability of the internal nodes within SFQ systems.

An SFQ-based test point insertion module to enhance the controllability at any node has previously been proposed [11, 12]. The test point insertion module consists of blocking gates and a confluence buffer (CB) at each bit along the data path. The blocking gates are supplied by a clock signal. This clock signal is gated by a non-destructive read out T flip flop controlled by a test controller. Test_enable controls the bias current of the input JTL, preventing or enabling the propagation of an incoming SFQ pulse. The test insertion mode is on when less current is supplied, and consequently, the test insertion mode is off when more current is supplied to the input JTL. This method requires a test controller to control the bias current and a controlled current source.

The test insertion module selects between the input test signal and a data signal. For example, applying clocked blocking gates to insert test points within a 64 bit register requires 35% fewer Josephson junctions as compared to using multiplexers [11]. This advantage increases with current controlled blocking gates. This test insertion module supports both set/scan chains and test point insertion. These techniques can be applied to evaluate the fault characteristics of SFQ systems and to demonstrate built-in self-test (BIST) of SFQ compatible memory systems [12].

The primary contributions described in this paper lie in two areas. One aspect is a circuit solution to support DFT in SFQ systems, where two test modules are presented. The pro-

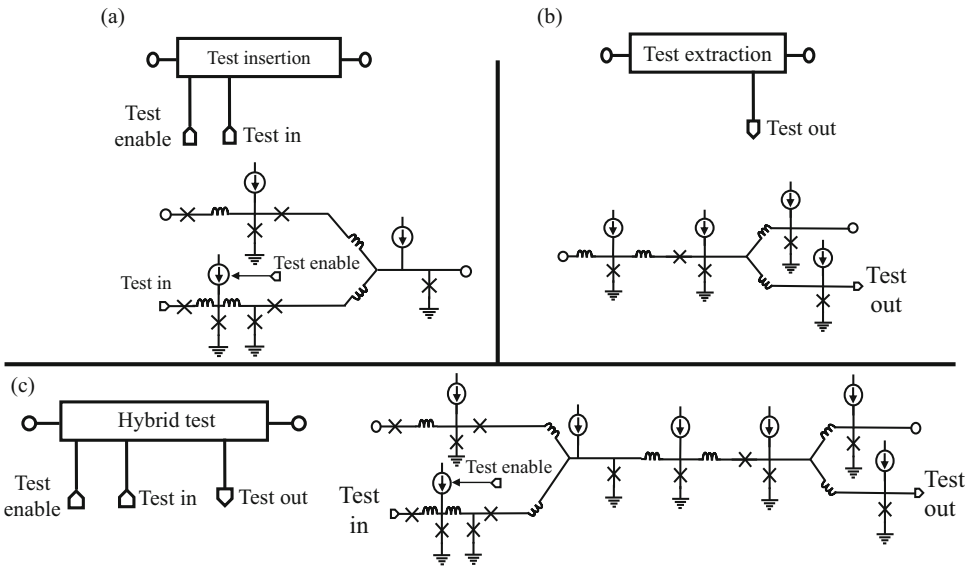

Fig. 1 Circuit- and block-level diagram of DFT approaches for SFQ systems, (a) test insertion module [11], (b) test extraction module, and (c) hybrid test module

posed test modules are; a test extraction module that observes the internal nodes of an SFQ system, and a hybrid test module to observe and control the internal nodes. A second aspect is a methodology for evaluating tradeoffs of inserting these circuit solutions on the observability and controllability of the internal nodes and hence the system testability.

This paper is organized as follows. In Section 2, the proposed test modules are described. The effects of incorporating the proposed test modules on certain test measures are discussed in Section 3. A methodology and related tradeoffs that consider these test modules in terms of power, area, detection speed, and overall testability are presented in Section 4. The paper is concluded in Section 5.

2 Test Modules

To support DFT in SFQ, a test extraction module and a hybrid test module are proposed to enhance the observability and controllability of SFQ systems, as shown in Fig. 1. The proposed test extraction module consists of a transmission line and a splitter that generates in real-time a copy of the propagated data. An additional hybrid module to improve the controllability and observability at the same node is also proposed.

As an example, the proposed hybrid test module is inserted to control or observe the output of the XOR gate in a single bit full adder, as illustrated in Fig. 2. The functionality of the proposed test modules is validated on a single bit full adder, as illustrated in Fig. 3. The detection speed, area overhead, and performance of the proposed test modules on a circuit under test are discussed in Section IV. These results validate the feasibility of these approaches to enhance the testability of SFQ systems.

3 Test Measures

To quantify the influence of the proposed test modules on testability quality measures, the Sandia controllability observabil-

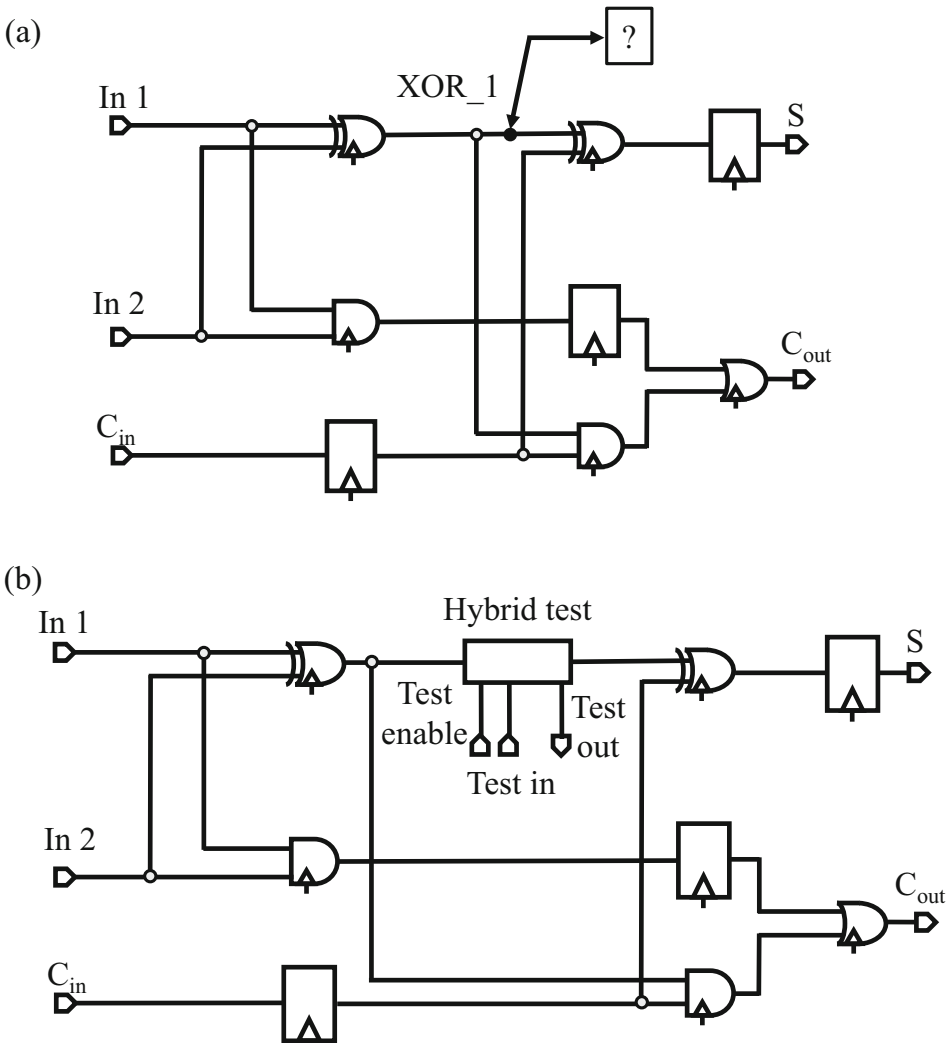

Fig. 2 Test circuit to validate the functionality of the proposed test modules, a) SFQ-based single bit full adder where the node under test (XOR_1) is the target node being observed/controled, and b) proposed hybrid test module inserted at the target node being observed/controled. Note that the hollow circle indicates a splitter cell [10]

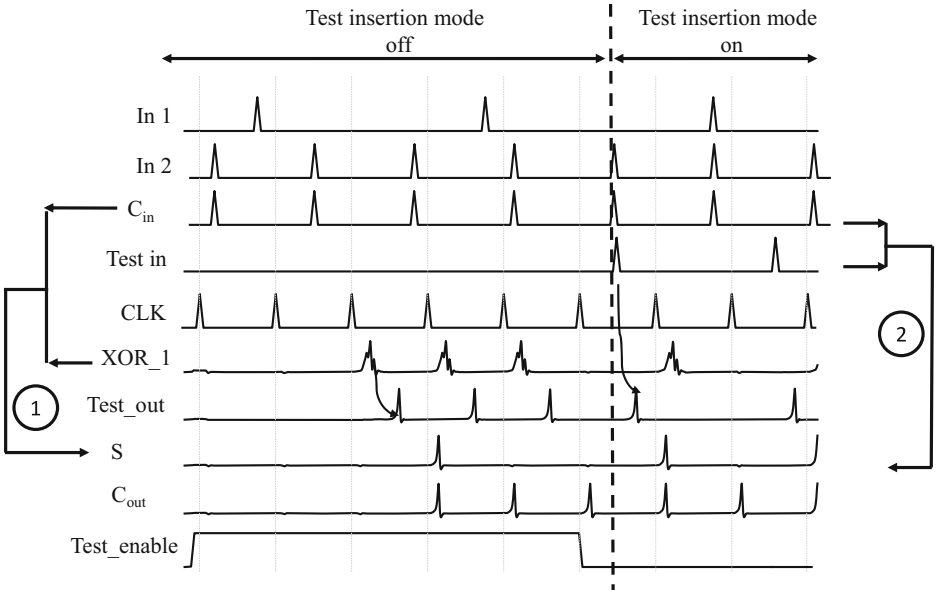

Fig. 3 Operation of proposed hybrid test module located at the XOR_1 node of a full adder, as illustrated in Fig. 2. The proposed hybrid test module operates as both a test insertion module and test extraction module with two modes of operation. *Test insertion mode off*, as indicated by label 1, when the signal at the XOR_1 node (the input to the test module) is produced at the output. In this case, the S output is the sum operation of the $In1$ and $In2$ signals, and the *Test insertion mode on*, as indicated by label 2, where the $Test\_in$ signal is passed to the output of the module. Hence, the S output is the XOR operation of the $Test\_in$ signal and the C_{in} signal. The $Test\_out$ signal is a real-time copy of the output of the test module. $Test\_enable$ switches between the two test modes

ity analysis program (SCOAP) is used [13]. SCOAP analyzes and quantifies the difficulty to control or observe internal nodes within a circuit, guides test generation, estimates fault coverage, and determines the test vector length. SCOAP measures the combinational circuits as follows. A combinational controllability of zero ($CC0$) describes the difficulty to set an internal node to logic 0 (ranging from 1 to ∞). A combinational controllability of one ($CC1$) measures the difficulty of setting an internal node to logic 1 (ranging from 1 to ∞). A combinational observability (CO) measures the difficulty of observing an internal node (ranging from 0 to ∞). Higher values of $CC0$, $CC1$, and CO indicate greater difficulty in controlling or observing an internal node.

Benchmark circuits such as ISCAS'85 C17 are used to explore and validate the proposed test modules to enhance the controllability and observability of the internal nodes within an SFQ system [14]. The SCOAP testability and controllability measures of the internal nodes are determined before and after inserting the proposed test modules, as illustrated in Fig. 4 and listed in Table 1. The SCOAP measures are described as ($CC0$,$CC1$)CO. As shown in Fig. 4(a), before inserting a test module, the SCOAP measures at node X are (2,5) 6 with $CC0$=2, $CC1$=5, and CO=6.

The test point location process is determined, as follows:

1) evaluate the global test measures and identify those nodes with the lowest testability characteristics. Nodes with high fanout are preferable.
2) insert the test module and determine the updated testability characteristics.
3) iterate between steps (1) and (2) to identify the optimal node (the test node which produces the greatest enhancement of the testability characteristics upon insertion of a test module).
4) Based on the testability requirements of the system, a methodology is proposed to identify the number of test modules and testability characteristics.

The process of selecting the optimal test point location(s) is a computational complex problem, where a common algorithm to achieve this objective, for example, is the iterative test point insertion algorithm [15, 16]. In this algorithm, each test point location is individually evaluated to determine the optimal location(s).

As an example, before inserting a test module within benchmark circuit C17, it is important to evaluate the global test coverage to determine any testability bottlenecks. As shown in Fig. 4(a), nodes X and $\overline{X}$ exhibit the highest testability measures and highest fanout. These high measures are indicative of the difficulty of measuring these nodes. Nodes X and $\overline{X}$ are set as the nodes under test. The proposed hybrid test module is individually inserted at each of these nodes, and the SCOAP testability measures are recalculated.

SCOAP is used to analyze the structure of the circuit under test to guide the DFT insertion process. The location of the inserted modules is chosen to enhance the testability charac-

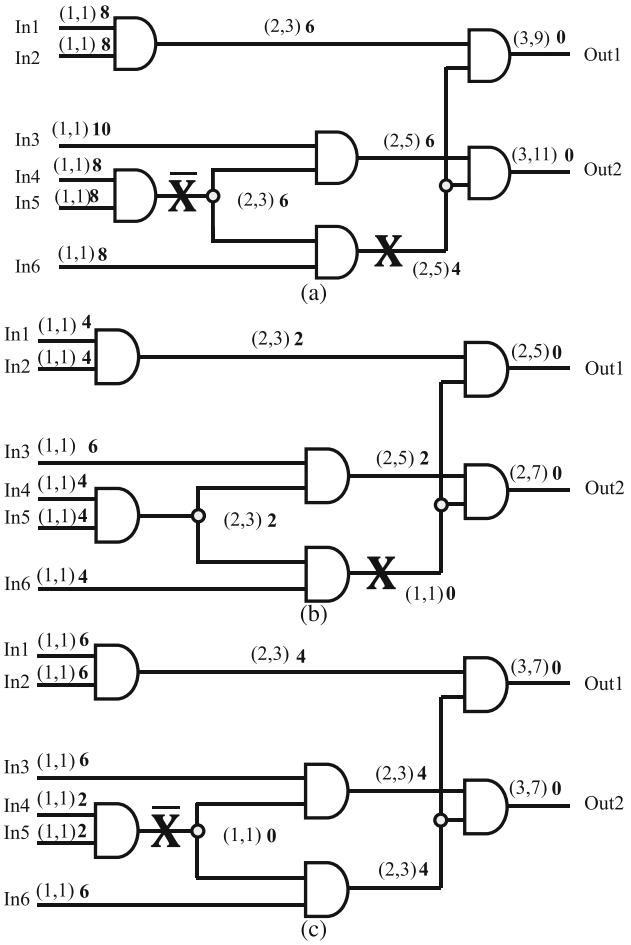

Fig. 4 SCOAP testability evaluation of ISCAS'85 C17 benchmark circuit, (a) before insertion of the proposed test modules, (b) after insertion of the hybrid test module at node X (the output of the second level AND gate), and (c) the output of the first level AND gate (at node $\overline{X}$)

teristics of the overall system. Due to the difference between the testability measures in the circuits shown in Figs. 4(b) and (c), node X is chosen for test point insertion over node $\overline{X}$. Inserting a test module at node X enhances the controllability and observability characteristics at most of the internal nodes of the circuit under test, as illustrated in Fig. 4(b).

Table 1 Comparison of the effects of inserting the proposed test modules into the ISCAS'85 C17 benchmark circuit in terms of SCOAP testability measures

	CC0 max	CC1 max	CO max	$\sum$CCO	$\sum$CC1	$\sum$CO
W/O test modules	3	11	10	20	42	72
Test extraction module	3	11	10	20	42	52
Test insertion module [9]	2	7	8	17	30	46
Hybrid test module	2	7	6	17	30	32

4 Methodology of Incorporating Test Modules

The objective of a methodology to incorporate the proposed test modules is to identify the number, type, and location of each of the test modules within an SFQ system. Each test module influences the testability characteristics differently, affecting the power, area, and delay. As an example, a comparison of the effects of inserting only one test module (test insertion, test extraction, or hybrid test module) at node X in the C17 benchmark circuit (shown in Fig. 4) is listed in Table 1. The overhead of inserting each of these modules is listed in Table 2.

After inserting a test extraction module at node X in the C17 benchmark circuit, as illustrated in Fig. 4, the sum of the combinational observability measure of all nodes ($\sum CO$) is enhanced by 28%. Inserting one test insertion module enhances both the sum of the combinational controllability to logic 1 ($\sum CC1$) and to logic 0 ($\sum CC0$) by, respectively, 29% and 15%, and $\sum CO$ by 36%. Inserting one hybrid test module improves $\sum CC1$ and $\sum CC0$ by, respectively, 29% and 15% and $\sum CO$ by 56%.

SFQ logic gates are inherently clocked and latched [18]. Moreover, each logic stage between sequentially-adjacent registers may require several clock cycles to produce an output [19]. The proposed test extraction module has no effect on system speed as long as $T_{Delay} + T_{Combinational} < T_{CLK}$, where T_{Delay} is the delay of the test extraction module, $T_{Combinational}$ is the delay of the circuitry between the two registers/logic cells connected to the test extraction module, and T_{CLK} is the clock period [20]. The detection time of the proposed test extraction module is 7 ps, and 18 ps for the proposed hybrid test module (in a 10 kA/cm^2 process technology [6, 17]).

As listed in Table 2, the proposed test extraction module exhibits an energy overhead of 0.2 fJ to extract one pulse. The test insertion module exhibits 0.11 fJ/pulse in normal mode - test insertion mode off - and 0.065 fJ/calculation in test mode. The hybrid test module exhibits 0.4 fJ/pulse in normal mode and 0.35 fJ/calculation in test mode (for a 10 kA/cm^2 process technology). Note that this power estimate is for the test module itself. Additional circuitry is needed to generate test vectors and communicate the data to room temperature.

The structure of the circuit under test determines the influence of inserting a test module [12, 21]. Certain parameters,

Table 2 Comparison of the overhead of inserting the proposed test modules on the area (number of resistively shunted JJs, inductors, and power resistors), power dissipation, detection time, and delay (for a 10 kA/cm^2 process technology, where JJ, L, and R, represent, respectively, the number of JJs, inductors, and resistors in the module. [6, 17])

	# Devices			Detection time (ps)	Advantage	Delay overhead τ_{Delay} (ps)	Energy overhead (fJ)/pulse
	JJ	L	R				
Test extraction module	5	4	4	7	Enhanced observability	7	0.2
Test insertion module [9]	8	5	3	N/A	Enhanced controllability	5	Normal: 0.11 Test: 0.065
Hybrid test module	13	9	7	18	and observability	18	Normal: 0.4 Test: 0.35

such as the number of nodes, number of logic gates, number of logic levels from the primary inputs (for controllability) or primary outputs (for observability), and fanout of each internal node, determine whether inserting a test module is an effective solution.

Multiple benchmark circuits have been analyzed to evaluate the effectiveness of the proposed modules for different circuit structures. One hybrid test module is inserted at a node in several benchmark circuits; ISCAS'85 circuits, C17 and C432, and 74X-series circuits, 74182 and 74283. In the data listed in Table 3, one hybrid test module is inserted at one of the target nodes. This node is selected after identifying the critical signal path with the most number of nodes with high fanout and worst testability characteristics (as previously discussed in Section 3). Inserting a hybrid test module into C17 and C432 is more effective in improving testability than into 74182 and 74283 since C17 and C432 contain a greater number of high fanout nodes and long signal paths.

Pseudocode describing the methodology and tradeoffs of inserting test modules into an SFQ system is shown in Algorithm 1. The algorithm is composed of three steps. First, all internal nodes are scanned to determine the nodes with high testability measures (possible test points). Second, one test module is inserted at each possible test point followed by evaluating the testability characteristics of the entire system. The overhead of these test modules may not exceed target performance limits. Finally, a test module is inserted at the internal node with the poorest testability characteristics. These three steps are repeated until the target testability characteristics are achieved or the system exceeds the target performance requirements.

Algorithm 1 Pseudocode of Algorithm for Inserting Test Modules into an SFQ System.

Input: Number of nodes N, location of each node ($Nloc$), target testability characteristics $Tcon$ and Tob, and performance overhead limit $Over_{limit}$
Output: Number n, type $Ttype$, and location $Tloc$ of test modules
Evaluate testability characteristics of all internal nodes $Ncon$ and Nob
for $k \leftarrow 1$ to N **do**
  if $(Ncon_k \geq Tcon)||(Nob_k \geq Tob)$ **then**
    $Pn \leftarrow Nloc_k$ ▷ Possible nodes for testpoints
  else
    exit
  end if
end for
for $k \leftarrow 1$ to size of Pn **do**
  Insert test module
  Evaluate testability characteristics Con_k and Obs_k
  Evaluate performance overhead $Overhead$
  Over power flag $OF = 1$
  if $(Overhead > Over_{limit})$ **then**
    continue
  end if
  $OF = 0$
  Pre-final node $PF_k \leftarrow (Nloc(Pn_k), Con_k, Obs_k)$
end for
if $(OF = 1)$ **then**
  exit
end if
final node $FN \leftarrow PF(i)$ with i is the index of lowest $Con(PF)$ and $Obs(PF)$
$n = n + 1$
$Tloc_n = Nloc(FN)$
go to Step 1

5 Conclusions

Advanced testing methodologies are required to support complex digital SFQ systems. In this paper, two solutions are presented to enhance the testability of SFQ systems by improving the controllability and observability of the internal nodes. A test extraction module with a detection time of 7 ps and a hybrid test module with a detection time of 18 ps are presented. The proposed test modules are validated on a suite of benchmark circuits. A comparison of the effects of inserting the test modules into different benchmark circuits in terms of the overhead and testability measures is provided. The proposed test modules, test insertion, extraction, and hybrid, for the ISCAS'85 C17 benchmark circuit exhibit an energy overhead of, respectively, 0.2, 0.11, and 0.4 fJ/pulse. The proposed test modules enhance the testability measures (controllability and observability) of the internal nodes, increasing overall fault coverage.

Table 3 Comparison of the effects of inserting a hybrid test module into ISCAS'85 C17 and C432 benchmark circuits, and 74X-series circuits 74182 and 74283 in terms of the per cent enhancement of the SCOAP testability measures before and after insertion of the hybrid test module

		CC0 max		CC1 max		CO max		$\sum$ CCO		$\sum$ CC1		$\sum$ CO	
		#	%	#	%	#	%	#	%	#	%	#	%
C17	Before	3	33%	11	36%	10	40%	20	15%	42	29%	72	56%
	After	2		7		6		17		30		32	
C432	Before	27	37%	25	40%	32	32%	145	25%	97	22%	360	24%
	After	17		15		22		108		75		273	
74182	Before	9	0%	9	11%	9	0%	63	5%	92	5%	134	11%
	After	9		8		9		60		88		119	
74283	Before	12	0%	15	13%	11	0%	95	3%	240	7%	383	7%
	After	12		13		11		92		223		356	

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Data Availability The datasets supporting the conclusions of this article are included within the article.

Declarations

Conflict of Interest The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

References

1. Mukhanov OA (2011) Energy-efficient single flux quantum technology. IEEE Trans Appl Supercond 21(3):760–769
2. Chen W, Rylyakov A, Patel V, Lukens J, Likharev K (1999) Rapid single flux quantum T-flip flop operating up to 770 GHz. IEEE Trans Appl Superconductivity 9(2):3212–3215
3. McDermott R, Vavilov MG, Plourde BLT, Wilhelm FK, Liebermann PJ, Mukhanov OA, Ohki TA (2018) Quantum-classical interface based on single flux quantum digital logic. Quantum Sci Technol 3(2):024004.1-024004.18
4. Krylov G, Friedman EG (2022) Single Flux Quantum Integrated Circuit Design. Springer
5. Krylov G, Jabbari T, Friedman EG (2024) Single Flux Quantum Integrated Circuit Design, 2nd edn. Springer
6. Tolpygo SK, Bolkhovsky V, Weir TJ, Wynn A, Oates DE, Johnson LM, Gouker MA (2016) Advanced fabrication processes for superconducting very large-scale integrated circuits. IEEE Trans Appl Supercond 26:1–10
7. Semenov VK, Polyakov YA, Tolpygo SK (2017) AC-biased shift registers as fabrication process benchmark circuits and flux trapping diagnostic tool. IEEE Trans Appl Supercond 27(4):1–9
8. Bushnell M, Agrawal V (2004) Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, vol 17. Springer Science & Business Media
9. Krylov G, Friedman EG (2019) Globally asynchronous, locally synchronous clocking and shared interconnect for large-scale SFQ systems. IEEE Trans Appl Supercond 29(5):1–5
10. Jabbari T, Krylov G, Kawa J, Friedman EG (2021) Splitter trees in single flux quantum circuits. IEEE Trans Appl Supercond 31(5):1–6
11. Krylov G, Friedman EG (2017) Design for testability of SFQ circuits. IEEE Trans Appl Supercond 27(8):1–7
12. Krylov G, Friedman EG (2017) "Test Point Insertion for RSFQ Circuits," Proceedings of the IEEE International Symposium on Circuits and Systems, pp 1–4
13. Goldstein LH, Thigpen EL (1980) "SCOAP: Sandia Controllability/Observability Analysis Program," Proceedings of the ACM/IEEE Design Automation Conference, pp 190–196
14. Hansen M, Yalcin H, Hayes J (1999) Unveiling the ISCAS-85 benchmarks: a case study in reverse engineering. IEEE Des Test Comput 16(3):72–80
15. Tsai H-C, Cheng K, Lin C-J, Bhawmik S (1997) "A Hybrid Algorithm for Test Point Selection for Scan-Based BIST," Proceedings of the ACM/IEEE Design Automation Conference, pp 478–483
16. Ma Y, Ren H, Khailany B, Sikka H, Luo L, Natarajan K, Yu B (2019) "High Performance Graph ConvolutionaI Networks with Applications in Testability Analysis," Proceedings of the ACM/IEEE Design Automation Conference, pp 1–6
17. Tolpygo SK, Bolkhovsky V, Weir TJ, Galbraith CJ, Johnson LM, Gouker MA, Semenov VK (2015) Inductance of circuit structures for MIT LL superconductor electronics fabrication process with 8 Niobium layers. IEEE Trans Appl Supercond 25:1–5
18. Gaj K, Friedman EG, Feldman MJ (1997) Timing of multi-gigahertz rapid single flux quantum digital circuits. J VLSI Signal Process Syst 16(2):247–276
19. Friedman EG (2001) Clock distribution networks in synchronous digital integrated circuits. Proc IEEE 89(5):665–692
20. Neves JL, Friedman EG (1996) Design methodology for synthesizing clock distribution networks exploiting nonzero localized clock skew. IEEE Trans Very Large Scale Integration (VLSI) Syst 4(2):286–291
21. Touba N, McCluskey E (1996) "Test Point Insertion Based on Path Tracing," Proceedings of IEEE VLSI Test Symposium, pp 2–8

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