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2023 JETTA-TTTC Best Paper Award

Hui Jiang, Fanchen Zhang, Jennifer Dworak, Kundan Nepal, and Theodore Manikas, "Increased Detection of Hard-to-Detect Stuck-at Faults during Scan Shift," *Journal of Electronic Testing: Theory and Applications*, Volume 39, Number 2, pp. 227–243, April 2023

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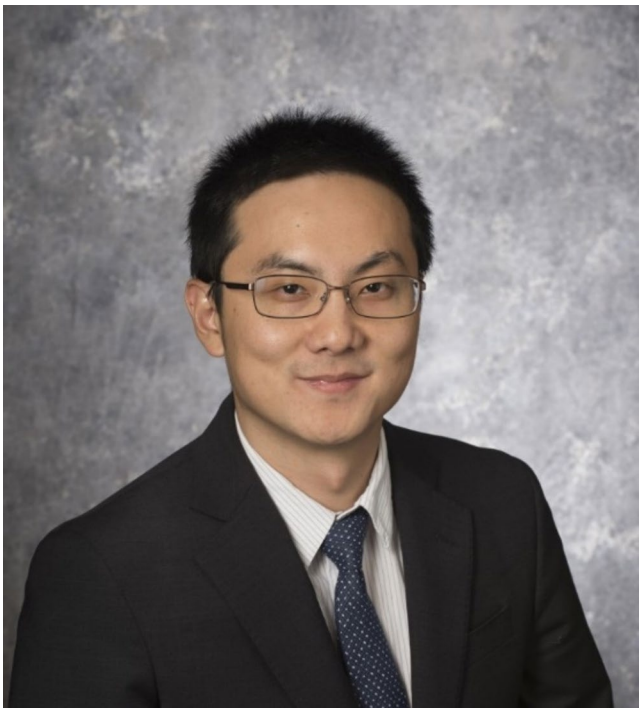
Abstract
Test sets that target standard fault models may not always be sufficient for detecting all defects. To evaluate test sets for the detection of unmodeled defects, n-detect test sets (which detect all modeled faults at least n times) have previously been proposed. Unfortunately, n-detect test sets are often prohibitively long. In this paper, we investigate the ability of shadow flip-flops connected into a MISR (Multiple Input Signature Register) to detect stuck-at faults fortuitously multiple times during scan shift. We explore which flip-flops should be shadowed to increase the value of n for the least detected stuck-at faults for each circuit studied. We then identify which circuit characteristics are most important for determining the cost of the MISR needed to achieve high values of n. For example, circuits that contain a few flip-flops with upstream fault cones that cover a large percentage of all faults in the circuit can often achieve high n-detect coverage fortuitously with a low-cost MISR. This allows a DFT engineer to predict the viability of this MISR-based approach early in the design cycle.

Hui Jiang received her Bachelor of Science degree in Electronic Engineering from Shandong University in 2014, a Master of Science degree in Computer Engineering from Southern Methodist University in 2016, and a Doctor of Philosophy degree in Computer Engineering from Southern Methodist University in 2022. Her research focuses on test set optimization and Design for Testability (DFT) circuitry to achieve high test quality with low test cost. In particular, her research explores how testing clock cycles can be most efficiently utilized to detect stuck-at and transition faults. During the summer of 2020 and 2021, she interned at Qualcomm Inc. in the Product Test Engineering team, working on timing violation modeling and diagnosis. Since January 2022, she has been working in the EDA area as a software engineer. Her work includes Boundary Scan Verification, Hierarchical Tests, and ATPG.



Fanchen Zhang earned his Ph.D. in Computer Engineering and M.S. in Electrical Engineering from Southern Methodist University. His research focused on advanced Design for Test (DFT) methodologies, including and the use of FPGAs for testing 3D stacked ICs, scan-based testing and probabilistic fault detection, improvement of cell-aware faults detection, contributing to multiple papers published in prestigious venues such as the IEEE International Test Conference (ITC), the Journal of Electronic Testing (JETTA), and the North Atlantic Test Workshop (NATW). A highlight of his work includes improving cell-aware fault coverage using scan shift cycles. Since 2018, Dr. Zhang has been a Design for Testability Engineer at Cisco Systems, where he develops and implements DFT methodologies for ASIC and COT chips. His work involves defining DFT architectures and implementing DFT design and IPs, generating and verifying ATPG test vectors, and supporting memory BIST design and verification. Dr. Zhang continues to lead innovations in post-silicon diagnostics and debugging, advancing the field of DFT. He is holding a patent for a method that enhances the testing process by simultaneously supplying test data to multiple test registers and storing test response data, improving test efficiency and data management.

Jennifer Dworak is a Professor in the Department of Electrical and Computer Engineering at Southern Methodist University and the Associate Director for the AT&T Center for Virtualization. Her research interests include manufacturing test, the reliability of digital circuits and systems, and hardware security. She is an author on multiple technical articles, including two papers that won a Best Paper Award from the VLSI Test Symposium and a paper that won a TTTC Naveena Nagi Award. She has also given over 30 invited talks and been an invited panelist at technical meetings on several continents. She is helping to lead the Texoma Semiconductor Tech Hub, which received official designation by the Economic Development Administration (EDA) of the U.S. Department of Congress in October of 2023. Jennifer holds PhD, MS, and BS degrees in electrical engineering from Texas A&M University in College Station, TX.

Kundan Nepal is a Professor of Electrical & Computer Engineering at the University of St. Thomas in Minnesota. He has a PhD from Brown University, RI. Kundan's expertise is in defect/fault tolerant circuits and systems, nanometer digital VLSI system design, reconfigurable computing, mobile robotics, embedded systems, and IoT. He teaches courses in Engineering Design, Electronics, and Embedded Systems. His current research explores power efficient testing, error detection and avoidance techniques in digital integrated circuits. In addition, his work also seeks the democratization of the exciting field of embedded computing and the Internet of Things by bringing these technologies to solve problems identified by traditionally under-served communities.

Theodore Manikas received the B.S. degree in electrical engineering from Michigan State University, the M.S. degree in electrical engineering from Washington University, St. Louis, Missouri, and the Ph.D. degree in electrical engineering from the University of Pittsburgh. He has been with Southern Methodist University since 2009 and is currently the Associate Chair of the Department of Computer Science. He is also a Licensed Professional Engineer in Texas and Oklahoma. His current research interests include computer systems design, security, and testing.