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RESEARCH

Investigation of Silicon Aging Effects in Dopingless PUF for Reliable Security Solution

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Abstract
Dopingless (DLFET) provides better reliability against any physically doped devices. Hence, this paper aims to provide a fair comparison between conventional junctionless (JLFET) and DLFET based ring oscillator (RO) physical unclonable function (PUF) that would lead to a better security solution against any aging constraints. To include aging challenges in our simulation, we stressed conventional JLFET and DLFET against channel hot carrier (CHC) and bias temperature instability (BTI) for 2000 secs. The maximum drain current deviation obtained in JLFET is 20.7 % and that of DLFET is 16 %. Hence, DLFET has more resistance against aging rollbacks than JLFET. Further, 256 staged DL-RO-PUF and JL-RO-PUF are implemented and it is observed that a DL-RO has 60 % better oscillating frequency as compared to a JL-RO. Also, we found that the DL-RO-PUF produce more unique keys than JL-RO-PUF as the inter hamming distance (HD) is 46.9 % for former and 44.6 % for later during normal working conditions. Also, we found that DL-RO-PUF is more reliable than JL-RO-PUF as the maximum intra-HD of former is 3.23 % and of later is 3.66 %. Hence, the novelty of this work is to introduce a highly unique and reliable security solution that helps to provide sustainable electronic systems.

Keywords Physical unclonable function (PUF) · Ring oscillator (RO) · Junctionless field effect transistor (JLFET) · Dopingless FET (DLFET) · Hardware security · Reliability

1 Introduction

Physical unclonable function (PUF) [1–3] is a security solution that is benefited by the already present random variations in semiconductor technology that arise during manufacturing process. These process variations are unclonable, unpredictable, unavoidable and random in nature and hence, act as unique hardware fingerprints. In a conventional ring oscillator (RO) PUF [4] a number of similar RO stages are fabricated through similar process and any two stages are selected and their frequencies are compared such that either 0 or 1 will be generated based on negative or positive delay difference. Therefore, PUF leverages through one of the reliability concern that is random variations, which are static and inevitable in nature [5]. However, other reliability issues are still prevailing in nature, such as environment and aging problems that are external conditions and time dependant [6]. Environment variations like temperature, humidity, noise and power supply variations surely affect system performance, but they return to normal conditions after some span of time and hence, adverse effects caused are not permanent in nature. Unlike environment variations, wear outs triggered due to aging are fixed in nature and does not recover over time and hence, life of an electronic product reduces drastically and only piles up to electronic waste periodically [7].

Considering these scenarios, our attempt is to provide security chips that would generate durable and robust keys for

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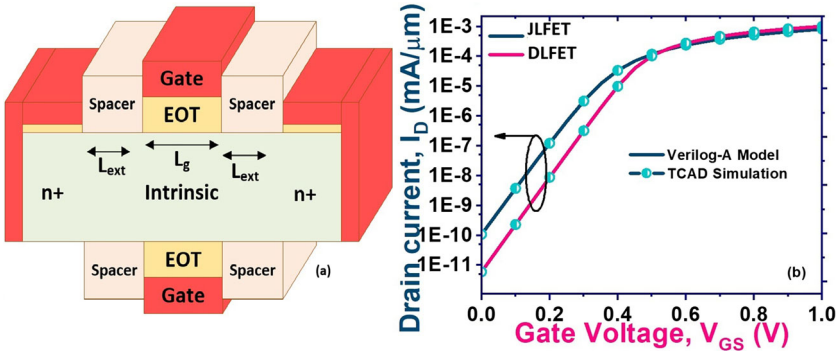

Fig. 1 (a) Physical structure of DLFET and (b) calibration results [20]

many years without fail [8]. Also, these keys should be different for each chip to authenticate large number of intellectual properties (IP) and should not be cracked through duplication or any counterfeiting over the time. Therefore, their uniqueness should be preserved against any aging wearout [9]. In this regard, we proposed a dopingless (DL) FET based 256 stage RO-PUF that would generate 128 keys as challenge response pairs (CRPs), which promise to provide reliable performance over time against traditional CMOS and junctionless (JL) FET based RO-PUF. Unlike MOSFET, JLFET is predominately doped with only one type of dopants and a high gate work function electrode control the short channel efforts (SCE) to a large extend. Therefore, ever decreasing transistor size and post CMOS technologies leverage high speed and low power electronic applications [10]. However, as the technology shrinks transistors face many reliability issues that arise due to random manufacturing variations, unpredictable environmental wear-outs and deteriorating aging factors. These factors not only reduce system performance but unknowingly create serious loopholes against security protocols [11, 12]. Unfortunately, we can not blindly trust software security algorithms as they may be unaware of any hardware disruptions at physical layer. Therefore, it is high time to resolve these reliability issues at transistor level itself, so strong lock-key combination can be manufactured and maintained in long run of time [13–15].

Table 1 Device design parameters

	JLFET	DLFET
Effective oxide thickness (t_{ox1})	1 nm	1 nm
Thickness of S/D oxide (t_{ox2})	–	0.5 nm
Silicon thickness (t_{si})	10 nm	10 nm
Gate length (L_g)	15 nm	15 nm
S/D extension (L_{ext})	15 nm	15 nm
Channel doping (N_D)	1e19 cm^{-3}	1e15 cm^{-3}
Gate work function (ϕ_g)	5.5 eV	4.73 eV
S/D work function ($\phi_{s,d}$)	–	3.9 eV

Alternatively, in DLFET regions are created using charge plasma (CP)[16] technique where work function difference between intrinsic Si substrate and metals over source/drain regions attract electrons and hence, avoid any doping related SCEs or reliability issues [17]. On the other hand, traditional JLFET suffers oxide traps formation and gate leakage due to high vertical electric field caused by large doping profiles. Therefore, this work not only delivers a device level optimization but also targeted to provide a high performing, secure, and reliable security hardware. In next sections, our first attempt is to do drain current variation analysis of JLFET and DLFET at device level for fresh and stressed conditions. Here, these devices are stressed for temperature related reliability issues such as bias temperature instability (BTI) and channel hot carrier (CHC) for 2000 secs at very high gate and drain voltages [18]. This indicates that a high stress has been applied for short duration of time and exaggeration of which on long time scale bring future aspects of FETs approximately. Later, the electrical characteristics for normal and stressed devices have been observed for 100 Monte Carlo (MC) simulations and are exported into individual look-up tables using Silvaco Atlas tool. Next, we imported these characteristics into spice and carefully created netlist for RO-PUF circuit using JLFET and DLFET for all cases separately, from here onwards we will use the terms JL-RO-PUF and DL-RO-PUF to refer them individually. Finally, a faithful comparison between JL-RO-PUF and DL-RO-PUF have been done in terms of uniqueness and reliability in Matlab by applying mathematical conditions on so generated output from spice. Hence, this whole process took rigorous computing and clock cycles to bring novel devices into circuit level applications.

2 Device Reliability

In conventional JLFET, a consistent but large doping profile is maintained in lateral direction along with a high gate work function helps to switch ON and OFF the device. Alterna-

Table 2 Stress conditions

Condition	Devices	CHC stress	NBTI stress	PBTI stress
Stress	n-type	$V_G = V_D = V_{STRESS} = 1.9$	–	–
	p-type	$V_G = V_D = V_{STRESS} = -1.9$	$V_G = V_{STRESS} = -1.9$	–
Measure	n-type	$V_{G\_MEASURE}$ sweep from 0 to 1V		
–	–	$V_{D\_MEASURE}$ 0.2, 0.4, 0.6, 0.8		
	p-type	$V_{G\_MEASURE}$ sweep from 0 to -1V		
–	–	$V_{D\_MEASURE}$ -0.2, -0.4, -0.6, -0.8		

tively, in DLFET a uniform low doping is used but Hafnium is deposited over source and drain create n^+ regions. This is called as charge plasma concept. Figure 1(a) represents DLFET device structure. Device parameters are tabulated in Table 1. In order to, encapsulate reliability affects on device electrical characteristics pre-stress and post-stress conditions are evaluated. Pre-stress condition includes normal device bias conditions and FET models. We call this as a fresh transistor, which provides maximum performance in ideal lab conditions. However, as time passes various reliability issues creep into the structure and reduce device performance. This affect has been evaluated in simulation set-up by first applying a large DC voltage for 2000s along with additional reliability related models such as hot-electron injection (HEI). Finally, this stressed device structure is investigated under normal working conditions and this is called as post-stress transistor.

Here, for n-type FET normal gate and drain bias voltages are 1 V, whereas to evaluate CHC the stressed condition is 1.9 V for both terminals. On the other hand, to evaluate affect of PBTI in n-FET drain voltage is kept 1.9 V without any gate biasing. Conveniently, in p-type transistor all terminal potentials are kept negative [19]. Table 2 summarises the stress and measure conditions accurately. The simulation models had been validated and published in our previous published work [20] as shown in Fig. 1(b) that compares the drain current of both devices in normal working conditions and found that OFF current of DLFET is much smaller than conventional JLFET, which indicates better gate control and low leakage current in DLFET as compared to JLFET. Once, all device level simulations have been performed for pre and post-stress conditions, the drain current and terminal capacitance values have been imported in separate look-up tables, that later has been utilized for circuit simulation in spice.

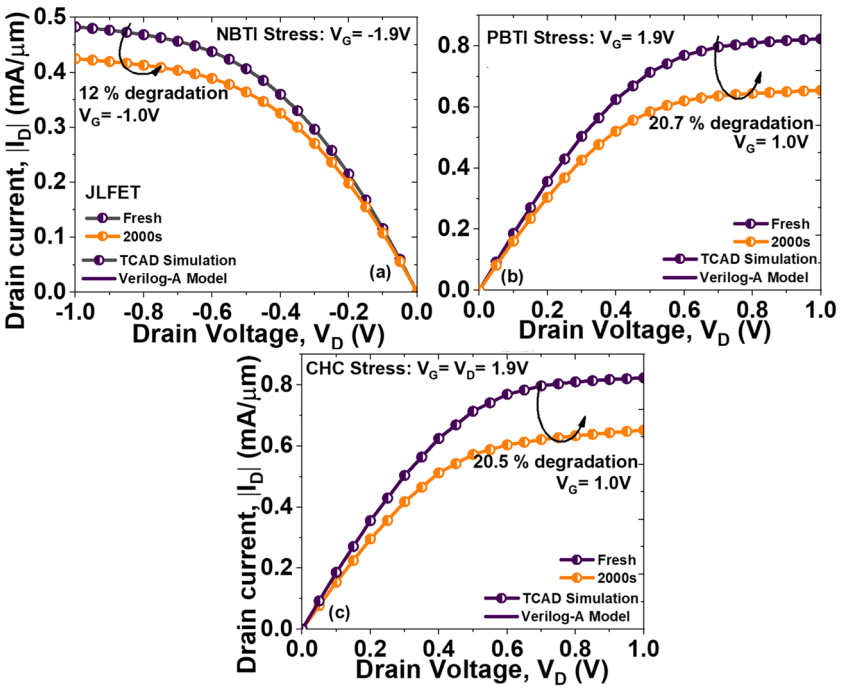

Fig. 2 Deviation of drain current in JLFET due to (a) NBTI, (b) PBTI, and (c) CHC stress conditions

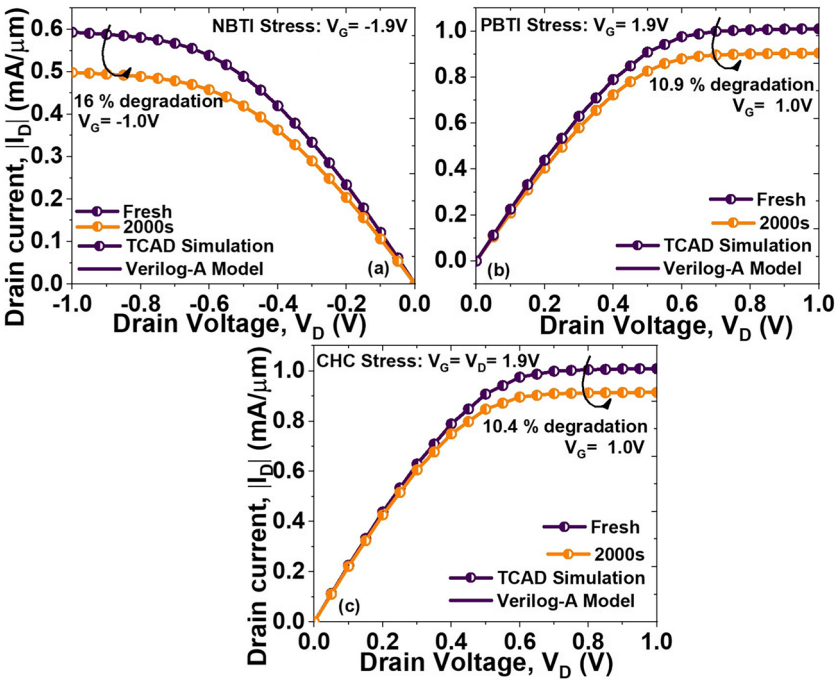

Fig. 3 Deviation of drain current in DLFET due to (a) NBTI, (b) PBTI, and (c) CHC stress conditions

2.1 Impact of Aging on JLFET and DLFET

This section discuses the impact of aging effect on conventional JLFET and CP based DLFET. Reliability analysis has been performed on both devices and percentage variation of drain currents have been calculated. The percentage variation of drain current on impact of NBTI is found to be 12 % (Fig. 2(a)) in p-JLFET, impact of PBTI is found to be 20.7 % (Fig. 2(b)), and impact of CHC is found to be 20.5 % (Fig. 2(c)) in n-JLFET. Similarly, the percentage variation of drain current on impact of NBTI is found to be 16 % (Fig. 3(a)) in p-DLFET, impact of PBTI is found to be 10.9 % (Fig. 3(b)), and impact of CHC is found to be 10.4 % (Fig. 3(c)) in n-DLFET. Table 3 compares the variation of subthreshold swing (SS), threshold voltage (V_t), I_{ON}, I_{OFF} and I_{ON}/I_{OFF} ratio of JLFET and DLFET for various doping concentrations. Therefore, it is proved that aging has more pronounced affect on conventional JLFET as compared to DLFET and hence, this indicates that DLFET has longer durability as compared to JLFET.

3 Circuit Implementation

Figure 4(a) explains the working of RO-PUF [4], where it is assumed an array of ROs have been developed and

Table 3 Device performance parameters

Device structure	Doping concentration (cm^{-3})	$V_t(mV)$	SS (mV /Decade)	I_{ON} (mA)	I_{OFF}	I_{ON}/I_{OFF}
n-DLFET	0.8 x 10^{15}	44.6	62.9	1.0	5.9 x 10^{-12}	0.2 X 10^9
	1 x 10^{15}	44.5	62.9	1.0	5.9 x 10^{-12}	0.2 X 10^9
	1.2 x 10^{15}	44.4	62.9	1.0	5.9 x 10^{-12}	0.2 X 10^9
p-DLFET	0.8 x 10^{15}	41.2	63.3	0.5	5.9 x 10^{-12}	0.1 X 10^9
	1 x 10^{15}	41.1	63.3	0.5	5.9 x 10^{-12}	0.1 X 10^9
	1.2 x 10^{15}	41.0	63.3	0.5	5.9 x 10^{-12}	0.1 X 10^9
n-JLFET	0.8 x 10^{19}	65	63.9	0.7	7.9 x 10^{-12}	0.1 X 10^9
	1 x 10^{19}	47.1	64.6	0.8	1 x 10^{-10}	0.1 X 10^9
	1.2 x 10^{19}	44.4	62.9	1.0	5.9 x 10^{-12}	0.2 X 10^9
p-JLFET	0.8 x 10^{19}	59.3	64.3	0.4	3.0 x 10^{-12}	0.1 X 10^9
	1 x 10^{19}	57	65	0.5	3.5 x 10^{-11}	0.1 X 10^8
	1.2 x 10^{19}	54.6	65.9	0.6	4.4 x 10^{-10}	0.1 X 10^7

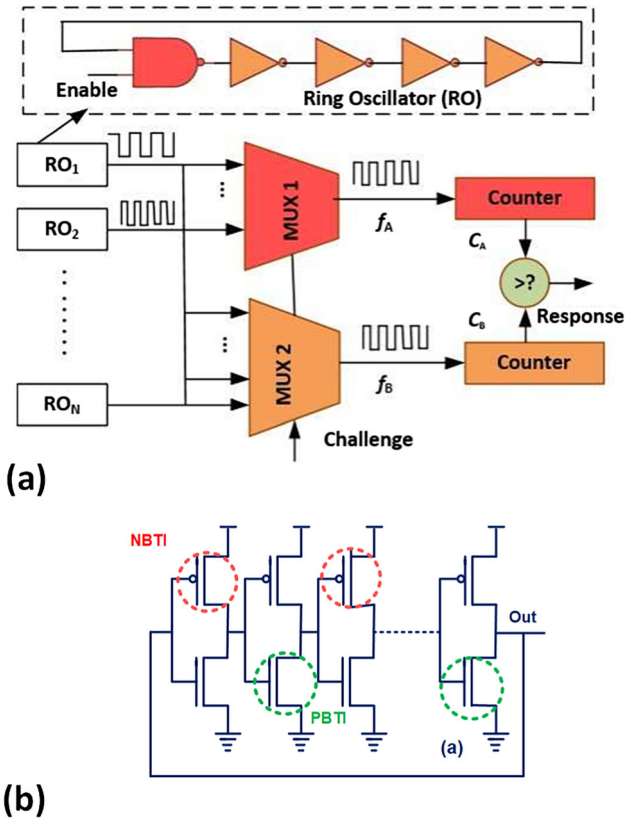

Fig. 4 (a) Circuit diagram of RO-PUF and (b) exact locations of BTI impact in a RO

fabricated using same process but uncontrollable and unpredictable manufacturing mismatches cause delay differences. Therefore, if any two RO has been selected and their frequencies have been counted and compared, the result will be 1 or 0 bit based on the positive or negative delay difference respectively. Here, MUX selector bits are known as challenges and final results are known as response. Hence, secure keys so generated are called as challenge response pairs (CRPs). We constructed the PUF architecture using an array of 256 ROs that generate 128 CRPs by comparing two ROs located far away from each other in layout as probability of being different is more in them as compared to ROs situated in neighborhood. These 128 CRPs are combinations of 7 challenge and 1 response bits. In order to include the static mismatches in device simulation, 100 MC simulations have been performed with 10% variation in device geometry on JLFET and DLFET for fresh, CHC and BTI conditions separately. Figure 4(b) represents exact locations of BTI influence in RO at transistor level.

Figure 5 compares the variations in delay of a JL-RO and a DL-RO for 100 different chips obtained through MC simulation under fresh condition, which indicates that later (Fig. 5(b)) is faster than former (Fig. 5(a)). Also, Fig. 6 shows shift in delay for JL-RO and DL-RO on account of NBTI, PBTI and CHC as compared to fresh state. It is clear that RO performance has been significantly delayed on account of PBTI and CHC as compared to NBTI for both cases. However, due to lack of random dopant fluctuations (RDFs) in DL-RO, the delay is least affected even by considering temperature and supply voltage variations as compared to JL-RO delay as shown in Fig. 7(a) and (b) respectively. Similarly, a comparison has been made for power-delay product (PDP) and found that DL-RO (Fig. 8(b)) has lower PDP that also has less fluctuations against temperature and supply voltage variations as compared to JL-RO (Fig. 8(a)). Therefore, DLFET provide better performance and sustainability for high-level electronic applications than JLFET.

3.1 Figure of Merits (FoM) of RO-PUF

This section compares figure-of-merits of JL-RO-PUF and DL-RO-PUF that decide which PUF provide more distinguish but sustainable security solution.

3.1.1 Uniqueness

To be secure enough it is required that sequential combination of 1 and 0 bits in CRPs should differ from one PUF to

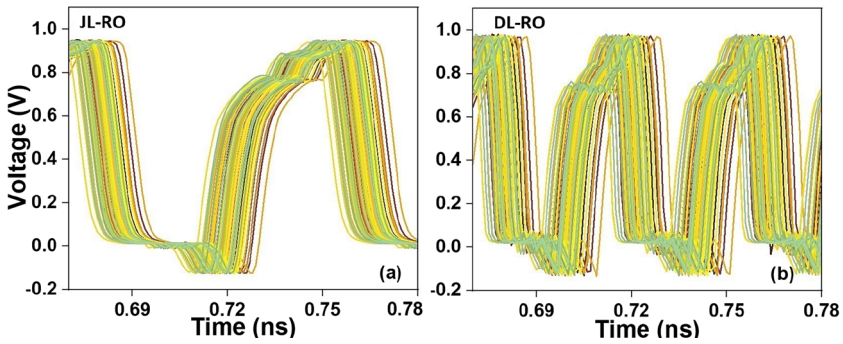

Fig. 5 100 Monte Carlo simulation results in fresh (a) JL-RO and (b) DL-RO

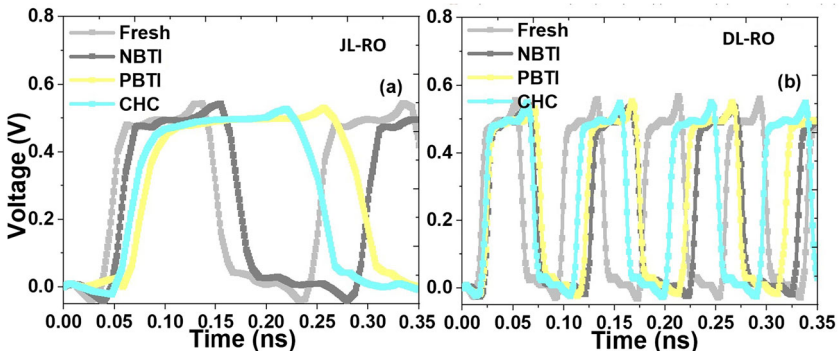

Fig. 6 Deviation in oscillation due to BTI and CHC in (a) JL-RO and (b) DL-RO

another, which decide uniqueness or inimitability of a PUF. Hence, uniqueness has been calculated using inter hamming distance (HD). In other words, inter-HD means EXORing CRPs such that unidentical locations can be identified. Ideally, there should be utmost 50 % unidentical bit positions among these different PUFs to ensure maximum uniqueness. Hence, in this work we evaluated the inter-HD of 100 RO-PUF made-up of JLFET and DLFET for fresh, NBTI, PBTI and CHC conditions. Figure 9 shows that the inter-HD of JL-RO-PUF is 44.6 % (Fig. 9(a)) and that of DL-RO-PUF is 47.9 % (Fig. 9(b)) in fresh condition, which indicates that DL-RO-PUF provides more unique security solution as compared to conventional JL-RO-PUF. Also, we evaluated inter-HD of these PUFs for different stressed conditions. It is found that under CHC stress the inter-HD of JL-RO-PUF is 40.98 % (Fig. 10(a)) and that of DL-RO-PUF is 46.4 % (Fig. 10(b)), this indicates that there is less deviation and more closeness to ideal inter-HD in DL-RO-PUF and hence, DLFET is capable to preserve uniqueness against CHC. Also, Fig. 11 shows that the inter-HD of JL-RO-PUF is 47.8 % (Fig. 11(a)) and that of DL-RO-PUF is 47.9 % (Fig. 11(b)) under NBTI stress, which also indicates that former is more immune to NBTI as compared to later one. Finally, Fig. 12 shows that inter-HD of JL-RO-PUF is 42.6 % (Fig. 12(a)) and that of DL-RO-PUF is 46.7 % (Fig. 12(b)) under PBTI stress, that again verifies that DL-RO-PUF would remain unmatchable even after years.

3.2 Reliability

Other than uniqueness, reliability is another major FoM for PUF designs. It is obvious from our previous discussions that DLFET based PUF designs must be more reliable as compared to JLFET-PUF. Reliability can be calculated using intra-HD. Here, CRPs obtained on normal working conditions are XOR with the CRPs obtained after applying stress. Lower the intra-HD better will be PUF reliability or there would be less possibility of 0 to 1 or 1 to 0 bits alteration in longer run. Hence, there will be high probability that for every run of challenge same response will be generated even after years. Figure 13 shows the average intra-HD of JL-RO-PUF is 3.29 % (Fig. 13(a)) while that of DL-RO-PUF is 2.87 % (Fig. 13(b)). Figure 14 shows the average intra-HD of JL-RO-PUF is 3.66 % (Fig. 14(a)) while that of DL-RO-PUF is 3.23 % (Fig. 14(b)). Figure 15 shows the average intra-HD of JL-RO-PUF is 3.33 % (Fig. 15(a)) while that of DL-RO-PUF is 2.86 % (Fig. 15(b)). All these observations indicate that DL-RO-PUF has better reliability against temperature variations as compared to JL-RO-PUF. Therefore, DLFET is

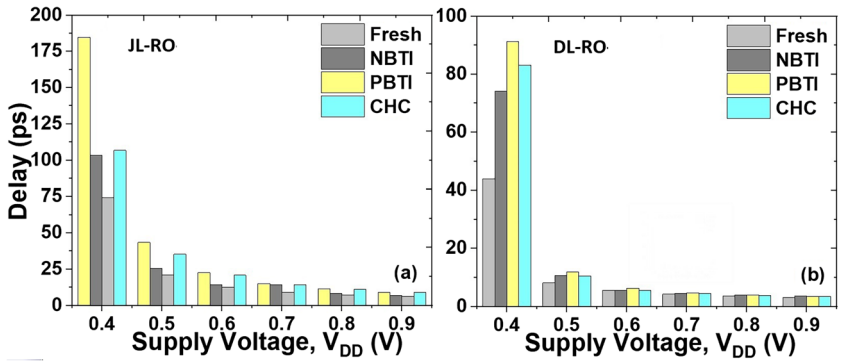

Fig. 7 Deviation of delay due to BTI and CHC in (a) JL-RO and (b) DL-RO for different supply voltages

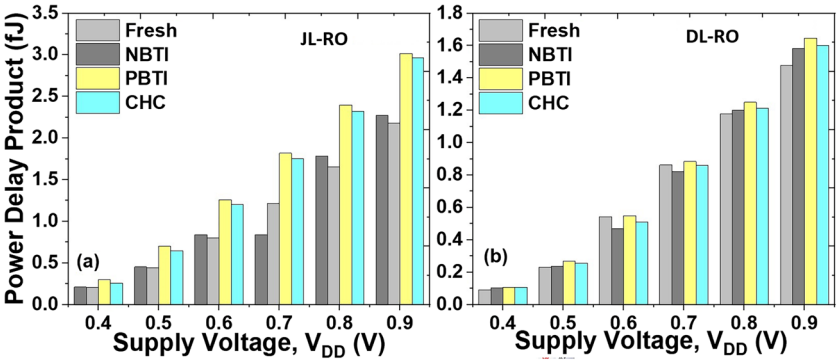

Fig. 8 Deviation of power delay product (PDP) due to BTI and CHC in (a) JL-RO and (b) DL-RO for different supply voltages

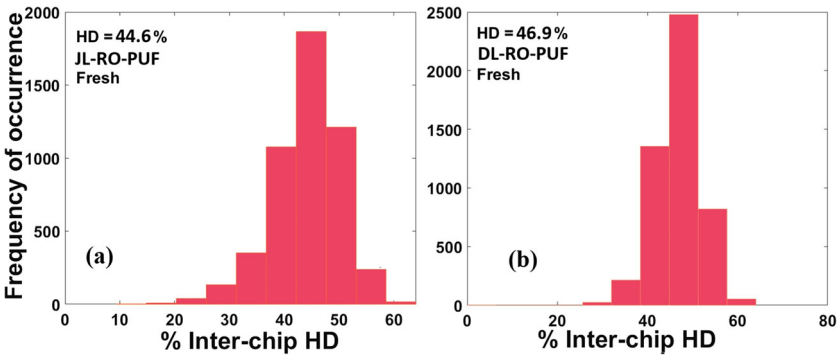

Fig. 9 Inter HD of (a) JL-RO-PUF and (b) DL-RO-PUF under fresh condition

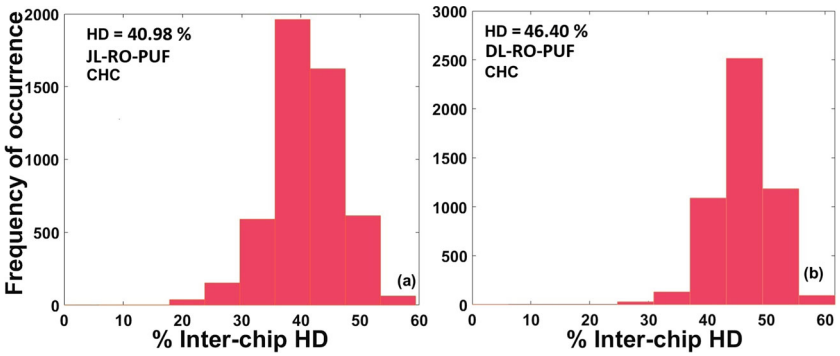

Fig. 10 Inter HD of (a) JL-RO-PUF and (b) DL-RO-PUF under CHC condition

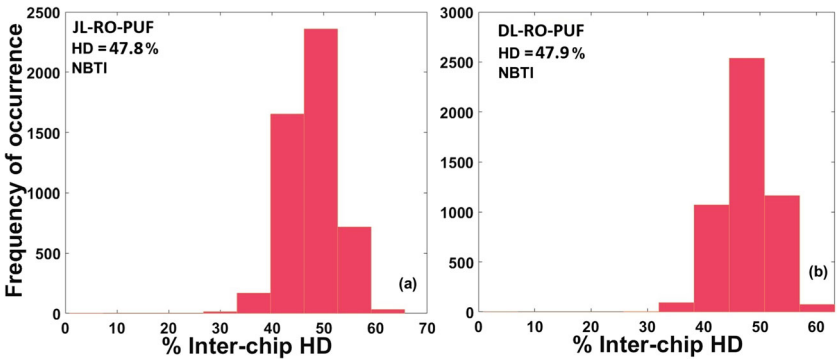

Fig. 11 Inter HD of (a) JL-RO-PUF and (b) DL-RO-PUF under NBTI condition

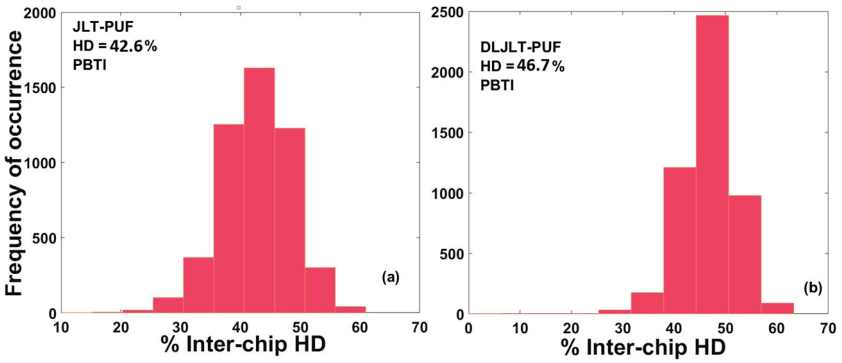

Fig. 12 Inter HD of (a) JL-RO-PUF and (b) DL-RO-PUF under PBTI condition

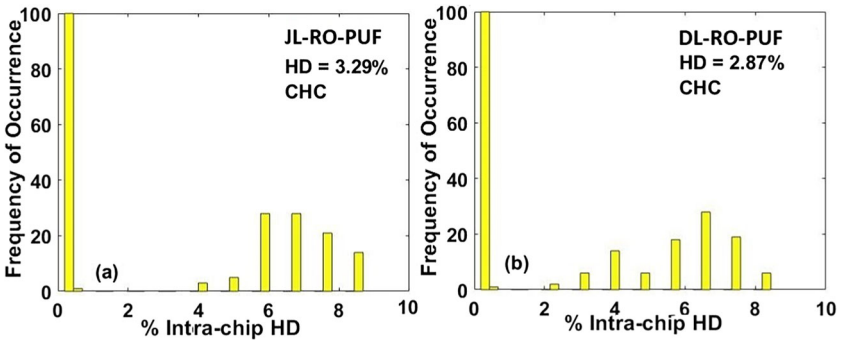

Fig. 13 Intra HD of (a) JL-RO-PUF and (b) DL-RO-PUF under CHC condition

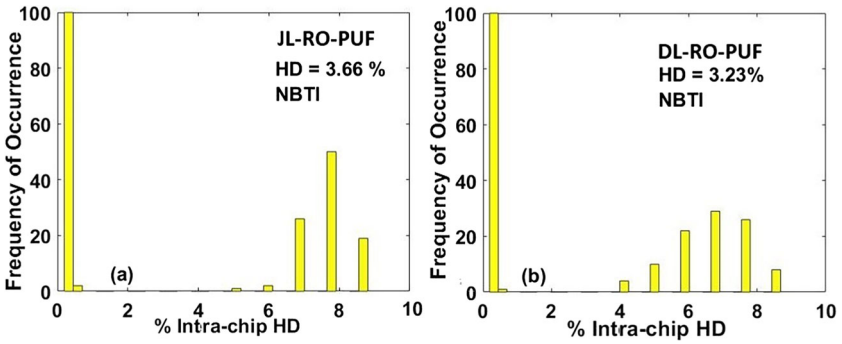

Fig. 14 Intra HD of (a) JL-RO-PUF and (b) DL-RO-PUF under NBTI condition

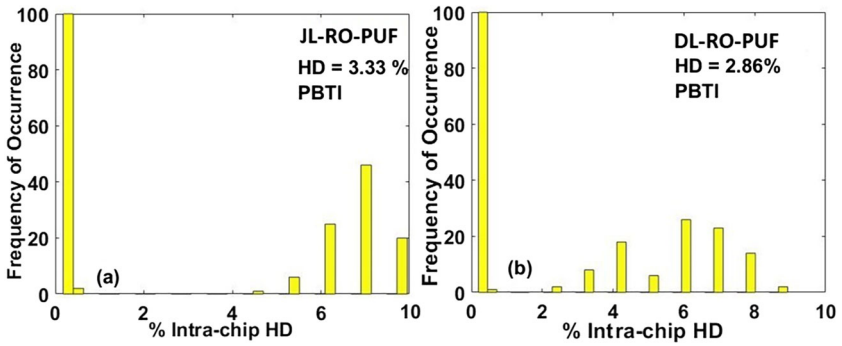

Fig. 15 Intra HD of (a) JL-RO-PUF and (b) DL-RO-PUF under PBTI condition

incredibly better option for circuit applications as compared to JLFET.

4 Conclusion

Sustainability of electronic systems means that systems should provide same performance for many years of operation as that it was designed to be. Indirectly, better sustainability can be achieved through better reliability. Hence, this paper presents a highly reliable but unique security chip using DLFET that avoids RDF, usually, main reason of performance inconsistency in conventional devices. Here, a 256 staged RO-PUF using DLFET and JLFET are constructed and their FoMs are compared for fresh, NBTI, PBTI and CHC stress conditions. We generated individual look-up tables for fresh and stressed states from device simulations, which are utilized in circuit level. Also, 100 MC simulations are executed to explore manufacturing variations for PUF. It is found that DL-RO-PUF produces inter-HD always closed to 50 % for all working conditions and hence, always unique as compared to JL-RO-PUF. Also, DL-RO-PUF keeps intra-HD in lower range for all working conditions and hence, more reliable as compared to JL-RO-PUF. Hence, this work is a proof that a high performing security solution can be reliable and hence, DLFET can be further used for better electronic sustainability.

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Availability of Data and Material All data and materials as well as software application or custom code support our published claims and comply with field standards.

Declarations

Conflicts of Interest The authors have no conflicts of interest to declare that are relevant to the content of this article.

Compliance with Ethical Standards Accepted principles of ethical and professional conduct have been followed. No human or animals' participation involved in the research.

Consent to Participate We agree to the terms and policies for the publication of the articles.

Consent for Publication We agree to the terms and policies for the publication of the articles.

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