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RESEARCH

Predicting Energy Dissipation in QCA-Based Layered-T Gates Under Cell Defects and Polarisation: A Study with Machine-Learning Models

Manali Dhar[1,2] · Chiradeep Mukherjee[3] · Ananya Banerjee[2,4] · Debasmita Manna[2,4] · Saradindu Panda[4] · Bansibadan Maji[2]

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Abstract

The semiconductor industry has encountered the physical constraints of current semiconductor materials and the impending end of Moore's forecast. The recent edition of the International Roadmap for Devices and Systems reveals that the semiconductor industry is now combining *More Moore, More than Moore* and *Beyond CMOS* to explore the possibilities towards emerging nanotechnologies like Quantum Cellular Automata (QCA). The fast-working speed, extremely low energy and high packing density make QCA incredibly appealing. In this work, machine learning-based models are developed to predict the energy dissipation of LT universal logic gates in advance with single-cell displacement defect (SCDD) and cell polarisation. Firstly, the cell-wise energy components of the universal logic gates realised by Layered T (LT) and Majority voter (MV) and logic reduction methodologies are estimated utilising the coherence vector (watt/energy) simulation engine of QCADesigner-E. Then, SCDD is introduced at the output LT universal gates in the horizontal and vertical directions, and consequent deviation in output cell polarisation and energy dissipation are examined. A dataset, namely *scdd_polarisation_energy (SPE)*, is created. In particular, K-Nearest Neighbour, Random Forest and Polynomial Regression-based machine learning (ML) models are found to be competent to anticipate the energy dissipation of LT universal logic gates. In ML models, the SCDD at the output cell and output polarisation are used as estimators, and energy dissipation (in electron Volt) is utilised as a response. These models offer less-complex and ease the energy estimation process in the QCA layout. The models are assessed based on r^2-score, mean absolute error (MAE), mean squared error (MSE), and root mean squared error (RMSE).

Keywords QCA · Layered T (LT) Gate · Single-cell displacement defect (SCDD) · Cell polarisation · Energy dissipation · Prediction · Machine Learning

1 Introduction

Moore's law, whose observation was first laid by Gordon Moore in the late 1960s, dominated the computing world for fifty years. The law states that the number of transistors on the integrated chip (IC) chip doubles every eighteen months [1]. However, instead of its uninterrupted incredible growth for five long decades, inconsistencies and limitations were observed in the performance of the chip. There are two significant limitations [2, 3]. Firstly, doubling the transistors in a small area generates unbounded heat within a chip. Secondly, continuous downscaling would cause an atomic-level feature size. In this trajectory, the quantum effects would be crucial in maintaining sustainability, forcing the traditional transistors to become unrealisable [4]. Nowadays, researchers urgently need to explore an alternative to

Responsible Editor: B. B. Bhattacharya

✉ Manali Dhar
manalidhar1985@gmail.com

[1] Centre for IOT, FET, ITER, Siksha 'O' Anusandhan Deemed to be University, Bhubaneswar, India

[2] Department of Electronics and Communication Engineering, National Institute of Technology, Durgapur, West Bengal, India

[3] Department of Computer Science Technology, University of Engineering & Management, Kolkata, West Bengal, India

[4] Department of Electronics and Communication Engineering, Dr Sudhir Chandra Sur Institute of Technology & Sports Complex, Kolkata, West Bengal, India

the Complementary Metal-Oxide-Semiconductor (CMOS) transistor, which embraces quantum effects and nano-scale physics [5].

The alternatives that can replace CMOS technology can be considered unique substitutes that broadly come with a specific technology with different features to store and convey binary information [6]. Under this type, diverse processor-based architectural designs are conceivable due to Boolean logic's implementation in another way. Radically emergent concepts like quantum physics, neuromorphic, and Deoxyribonucleic acid (DNA)-based computing are the most significant variants. The technologies which come under the manifold of this variant are as follows: - i) Carbon Nanotube (CNT) [7], ii) Spin-Wave Transistors (SWT) [8], iii) silicon nanowire [9], iv) Single Electron Transistor (SET) [10], iv) Tunnelling Phase Logic (TPL) [11], v) Molecular Electronics [12], vi) Superconducting electronics [13], vii) Resonant Tunnelling Devices (RTD) [14] and viii) Quantum-dot Cellular Automata (QCA) [15]. In one of its last meetings, the International Technology Roadmap for Semiconductor (ITRS) association focused on working on these technologies and emphasised some difficulties in implementing them [16].

In each of these technologies, it is worth mentioning that numerous devices per square centimetre reveal an excellent scope for further investigations. Some offer high throughput computation with below 40 nm (nm) cell size, while others provide ultra-low power dissipation and high operating speed. At this point, the research needs to be carried out so that a device can be propped with small size, ultra-low power dissipation, and high packing density to support ever-growing computation. QCA technology includes these three vital aspects in its feature, eliminating CMOS transistor scaling limitations.

The merits of the QCA technology manifest in the reduced demand for interconnects and the ability to realise structures that engage atoms or molecules. The QCA technology was first presented by Lent et al. in 1993 [17] that used the condition of a polarisation state to exhibit the information propagation from the input to the output of a layout. The QCA comprises quantum dots arranged inside a quantum cell, as shown in Fig. 1a. A quantum cell is a rudimentary square-shaped feature with oxide barrier material separating four quantum dots at four corners. The polarisation state of such a quantum cell is encoded as electric dipoles that consist of a cell of four quantum dots. Two electrons that occupy two of these quantum dots accommodate themselves in the furthest diagonal positions. Figure 1b demonstrates two possibilities associated with the primary and secondary diagonals representing the polarisation, P=-1 and +1. A group of cells interacts with each other through the electrostatic force of attraction and repulsion. The state of the nearest neighbouring cells determines the polarisation state of a specific cell. A single cell or a cluster of cells replicates to grow a complex system that takes information, processes a sub-task, and prepares intermediary outputs for the next level [18].

An external electric field regulates the information flow inside the QCA array, which is applied to the barriers between the quantum dots. This electric field, known as a clock, is employed to ensure the proper operation of these barriers. Logic gates are formed by exploiting the quantum-mechanical interactions and inherent properties of QCA cells. QCA logic gates utilise the collective behaviour of multiple cells to perform Boolean logic operations [19]. The important QCA logic gates are majority voter (MV) [20], and-or-invert (AOI) [21], universal logic gate (ULG) [22] and layered T (LT) gate [23].

A QCA cell with certain dimensions is fabricated using the self-assembly of nanostructures [24]. A molecular deposition is involved in this fabrication process, where a minor alteration may alter the characteristics of the QCA cell. Such a procedural deviation is termed a QCA defect. Several types of defects may occur; they are rotational cell defect (RCD), additional single cell deposition defect (ASCD) and, additional multiple cell deposition defect (AMCD), single cell displacement defect (SCDD) and multiple cell deposition defect (MCDD), single cell misalignment defect (SCMD) and multiple cell misalignment defect (MCMD). The output cell polarisation differs if any one (or the combination) of the defects as mentioned above occurs in a layout [25–28].

This work primarily carries out the cell-wise energy components of MV and LT universal gates. It is experimentally demonstrated in the subsequent sections that the

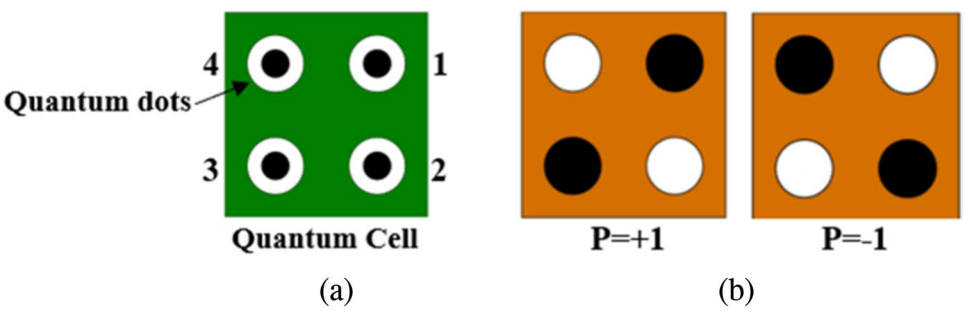

Fig. 1 **a** A quantum cell and its corresponding polarisations, **b** P = +1 and -1

energy dissipation of LT universal gates is lesser than corresponding MV counterparts. Therefore, the LT universal gates are chosen to assess the impacts of horizontal and vertical SCDD at the output cell on corresponding changes in target cell polarisations. Thereafter, SCDD, output cell polarisation and energy variations of a layout are collated to build the *scdd_polarisation_energy (SPE)* dataset. Finally, this work assesses and predicts the effects of SCDD and variation of target cell polarisation on the total and average energy dissipation using regression model of supervised machine learning (ML) algorithms [29, 30]. The detailed contributions are given as follows:

(i) Calculation and verification of cell-by-cell energy components of LT and MV universal logic gates. using computer-aided simulators, QCADesigner 2.0.3 [31] and QCADesignerE [32].
(ii) Detailed summary of total and average energy dissipation of LT and MV NAND & NOR in synchronisation with four clock signals.
(iii) Implementation of SCDD at the output cell of LT universal gates in horizontal and vertical directions, measuring its impact on the layout's output polarisation and energy dissipations.
(iv) Acquisition of *scdd_polarisation_energy (SPE)* dataset by capturing the SCDD at the output cell, variation of output polarisation and energy dissipations of LT universal gates, including data cleaning and data conditioning.
(v) Exploration of trends of the *SPE* dataset and correlation calculations amongst three critical parameters they are SCDD, output-cell polarisation (positive and negative), and total and average energy dissipation in electron Volt (eV) of LT universal gates.
(vi) Building and deployment of K-Nearest Neighbour (KNN), Random Forest (RF) and Polynomial Regression (PR) machine learning (ML) models to predict LT universal gates' energy dissipation depending on SCDD and output-cell polarisation.
(vii) Assessment of the performance of the proposed ML models depending on the metrics, mean absolute error (MAE), the mean squared error (MSE) and root mean squared error (RMSE).
(viii) To the best of the author's knowledge, this work is the first attempt which investigate the impact of defects and cell polarization on energy dissipations of nanotechnology-based QCA layouts. Additionally, the ML models are deployed on the newly proposed *SPE* dataset, and consequent performance metrics are reported.

The bistable approximation-based engine of QCADesigner 2.0.3 and the coherence vector (watt/energy) engine of QCADesigner-E are utilised to verify the QCA layouts and acquire the dataset. Additionally, the scikit-learn of the ML library is used for deploying the regression model [33].

The remaining work is organised as follows: Sect. 2 reviews the foundation of QCA, emphasising MV and LT logic reduction techniques. Additionally, the design metrics of MV and LT universal logic gates are calculated in this section. Afterwards, Sect. 3 provides the energy formulations of QCA layouts and analyses how energy is dissipated in logic gate layouts. Furthermore, this section specifies the ranges of parameters used in estimating the cellwise energy components. Section 4 defines QCA defects and discusses how energy dissipation varies concerning the output cell polarisations in the presence of SCDD. Section 5 discusses the fundamentals of machine learning models and deploys the ML models establishing proper SPE dataset predictors and responses. Section 6 analyses the outcomes with relevant discussions. The accuracies of the predictions are also visually illustrated in this section. Finally, the work is concluded in Sect. 7.

2 Foundation of QCA

2.1 Majority Voter and Layered T Gate

An isolated cell makes no sense in designing QCA layouts. However, a group of cells operate collectively to perform a specific task. In such a scenario, the polarisation of a particular cell impacts the polarisation of adjacent neighbour cells. For an example of an array of cells, or the binary wire, the first cell with logic state 1 drives the next cell to change its state to 1, and then the second cell performs the same to the third one and so on, only by Coulombic force of repulsion between the electrons of different cells [34]. The functionality remains similar for logic 0. Thus, an array of cells usefully operates as a connecting wire to carry digital logic from the input to the output cell, as revealed in Fig. 2a. Other preliminary logic primitives are a three-input Majority voter and a seven-cell conventional inverter, as demonstrated in Fig. 2b and c. A three-input MV consists of five QCA cells. Three of these four border cells take three inputs, i.e., A, B, and C; the remaining border cell is output, Z. The centre cell regulates the output polarisation, which favours the majority of the input logic states. Equation (1) provides the logical expression of three-input MV, as given below [35].

$$Z = \mathrm{Maj}(A, B, C) = AB + BC + AC \tag{1}$$

A conventional structure of an inverter comprises seven QCA cells that generate the output, Z as inverted input.

The realisation of numerous Boolean logic circuits becomes possible using the QCA primitives as mentioned

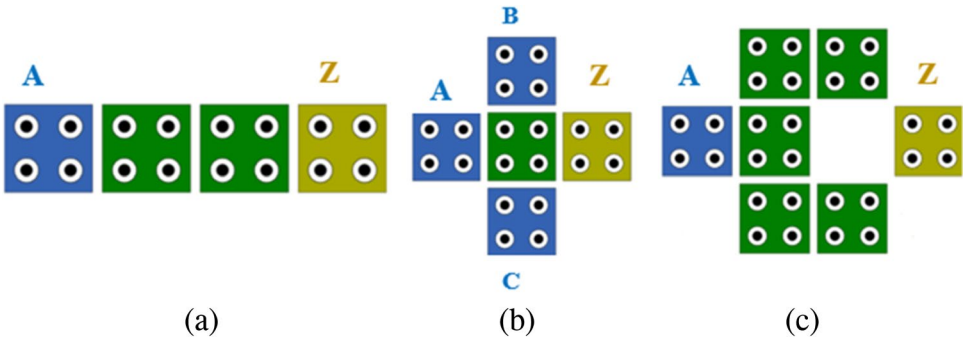

Fig. 2 **a** Binary wire, **b** 3-input Majority voter and **c** inverter

above. Layered T is another logic gate synthesising QCA layouts from a specific Boolean logic function.

An LT gate comprises five quantum cells. It has three inputs, one fixed polarisation (FP) cell and one output cell, as illustrated in Fig. 3a. Layer 1 occupies four quantum cells, whereas layer 2 keeps the FP cell with P = '+1' or '-1'. The placement of layer 2 vertically above layer 1 is significant. The optimum performance of the gate can be perceived when the variation of cell dimension (denoted as x) and dot diameter are maintained between 14 to 22 nm and 4 to 6 nm range, respectively, with 42 nm layer separation. Figure 3b and c demonstrate using two vertical layers in the layout and confirm the proposed gate as a multilayer gate in QCA [36, 37].

Z follows the NAND gate operation if the layer 2 cell is kept at logic 1. However, if it is kept at logic 0, then Z follows the NOR gate operation. Equation (2) provides the logical functionality of the LT gate:

$$\begin{cases} Z = \mathrm{L}_{\mathrm{T}}^{+}(\mathrm{A},\mathrm{B}) = \overline{\mathrm{AB}}, \ \textit{if layer 2 cell logic is 1} \\ Z = \mathrm{L}_{\mathrm{T}}^{-}(\mathrm{A},\mathrm{B}) = \overline{\mathrm{A}+\mathrm{B}}, \ \textit{if layer 2 cell logic is 0} \end{cases} \tag{2}$$

Here, the function, $\mathrm{L}_{\mathrm{T}}^{+/-}$ denotes the two-input LT function, and signs indicate the polarity of the fixed polarisation cell.

2.2 QCA Clock

In QCA, the clock synchronises the layout by providing driver power and controlling the signal flow direction. Individual cells need not be clocked separately. However, a group of QCA cells needs a clock to excite the entire QCA architecture to produce an output sequentially. In QCA, clocking is an essential process that synchronises the function of the system. The clocking scheme in QCA typically involves four phases. These phases are switch, hold, release, and relax. The switch phase occurs when the clock signal transitions from low to high. The switch phase prepares the QCA cells for the next cycle of computation. In this phase, the clock signal is high, holding the QCA cells in their current state and ensuring that the information stored in the cells remains stable and does not change during this period. During the release phase, the clock signal transitions from high to low, which causes the polarisation of the quantum dots in the QCA cells to relax. In the relax phase, the clock signal remains low, allowing the charges within the QCA cells to move freely and interact with neighbouring cells. The cells sense the polarisation and charge distribution of adjacent cells, which enables information propagation and the execution of logic operations. But the latched cell indicates the low clock signal [38, 39].

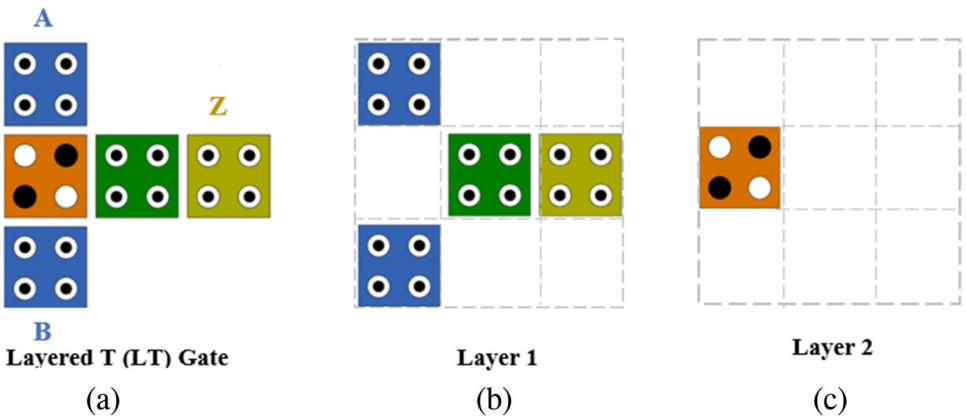

Fig. 3 **a** Layered T (LT) gate, **b** Main Cell Layer 3-input majority voter and **c** Upper Layer inverter

2.3 Crossovers

In complex multilevel QCA layouts, the data is transferred through the interconnecting binary wire without mixing with the other using crossovers. There are primarily three kinds of crossovers: i) coplanar [40], ii) multilayer [41], and iii) logical. The coplanar crossover occurs when a normal cell binary wire hops a rotated cell binary wire. The 45-degree cells are loosely coupled with regular (90-degree rotated) counterparts; hence, these cells do not affect each other's polarisation. When information is sent over the various vertical layers of a QCA design, a multilayer crossover occurs. Hence, cells with comparable orientations can cross each other. The multilayer crossovers excel over their coplanar counterparts for the reasons given below:

(i) The layout area of a multilayer crossover significantly goes lower than a coplanar crossover,
(ii) Multilayer nanostructures are reliable, robust, defect and fault-tolerant, and resilient to crosstalk,
(iii) The overall latency of the multilayer QCA layout becomes lower than the logical equivalent coplanar layout.

In the logical crossover, the information in one binary wire crosses the other using efficient clocking zone assignments inside a design. The inherent phase difference between four QCA clock signals helps to realise such crossovers in the layouts [42, 43].

2.4 Universal NAND and NOR using MV and LT Logic Gates

Since NAND and NOR are universal logic gates, any Boolean function can be realised using these gates in designing multilevel complex digital circuits. The QCA layouts of the universal logic gates are instantiated by MV and LT logic gates using QCADesigner 2.0.3 and simulated with the coherence vector-based simulation engine using the QCADesigner-E tool, as specified in Tables 1 and 2. The LT gate layout of Fig. 4a–d is simulated in QCA Designer 2.0.3 with the specific parameters mentioned in Table 1.

Table 2 Simulation parameters of QCADesigner-E

Sl. No.	Parameters	Value
1	Temperature	1 K
2	Relaxation Time	1.00e-015 s
3	Time Step	1.00e-016 s
4	Total Simulation Time	5.00e-011 s
5	Clock High	9.80e-022 J
6	Clock Low	3.80e-023 J
7	Clock Shift	NA
8	Radius of Effect	80 nm
9	Relative Permittivity	12.9
10	Layer Separation	11.5 nm
11	Time interval of each iteration step	1.00e-017 s
12	Input signals period	10.00e-012 s
13	Shape of clock signals	Ramp/gaussian/step

Unlike LT logic, the MV realisation does not support an in-built inverting function. However, an additional logic block required for the inversion may enhance the cost of the QCA circuits. The proposed LT method eliminates some disadvantages and complexities of the MV logic design. It also makes the mapping of the logic easier for the structural layouts. The corresponding QCA layouts of MV & LT NAND and NOR gates are demonstrated in Fig. 4a and c & in Fig. 4b and d respectively.

3 Energy Dissipation in QCA

3.1 Mathematical Expressions of Energy Dissipation in QCA

In QCA architecture, the clock phases regulate the energy dissipation of a layout. In the relax phase, the QCA cell remains depolarised. In switch and hold, the cell takes the energy from the clock and neighbouring cells to become polarised. In the release phase, the energy returns to the clock and neighbouring cells from where it was absorbed previously. However, some energy is lost in the environment during the release phase.

Table 1 Specifications of parameters of LT gate simulation in QCADesigner 2.0.3

Sl. No.	Parameters	Value or Range	Sl. No.	Parameters	Value or Range
1	Cell dimension	18 nmX18 nm	6	Relative permittivity	12.9
2	Layer separation	42 nm	7	Clock amplitude factor	2
3	RoE	65 nm – 80 nm	8	Convergence tolerance	0.001
4	Cell spacing	2 nm	9	Clock high	9.8e-22 J[a]
5	Dot diameter	4 nm	10	Clock low	3.8e-23 J[a]

[a]Implies Joule

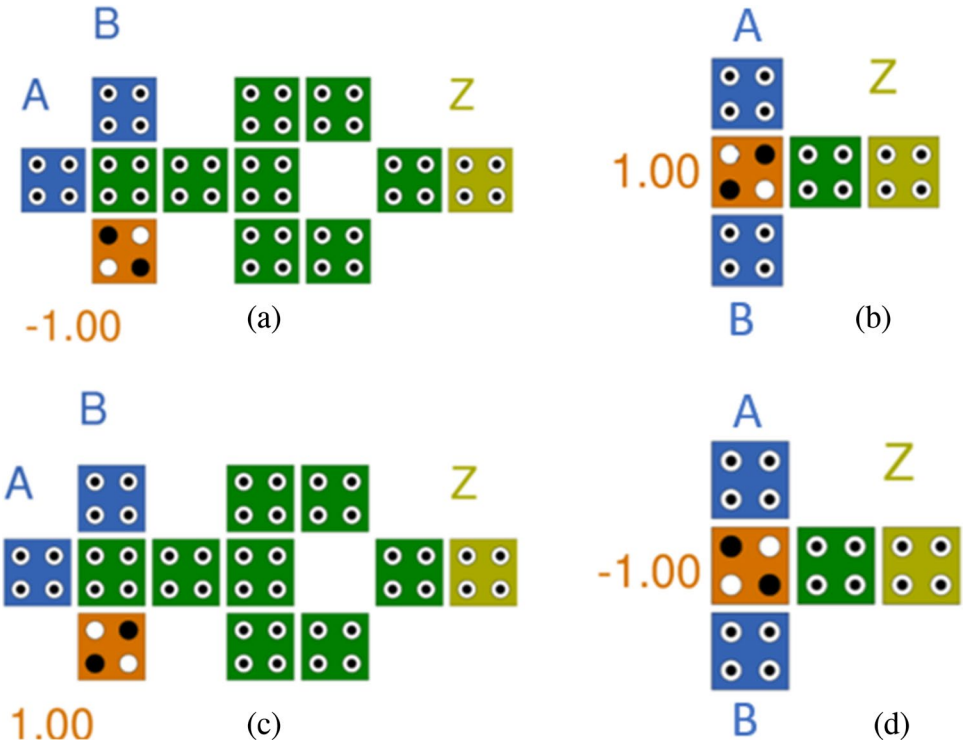

Fig. 4 QCA layouts **a** MV NAND, **b** LT NAND, **c** MV NOR and **d** LT NOR

The quantitative study of energy dissipation estimates the coherence vector (**Γ**) and the energy vector (**λ**). The instantaneous power of a QCA cell, P_{cell} is mathematically expressed in Eq. (3) [44].

$$P_{cell} = \frac{d}{dt}E_{cell}(t) = \frac{d}{dt}(\frac{\hbar}{2}\Gamma(t).\lambda(t)) \tag{3}$$

Here, $E_{cell}(t)$ is the scalar product of **Γ** and **λ** vectors and denotes the energy of the cell at any instance. Equation (4) represents the total energy, E_{tot} dissipated by a cell in four phases of clock cycles.

$$E_{tot} = \int_{Tc}^{t0+Tc} P_{cell}\, dt' = \frac{\hbar}{2}\int_{Tc}^{t0+Tc} (\frac{d}{dt}\Gamma(\mathbf{t}).\lambda(\mathbf{t}) + \frac{d}{dt}\lambda(\mathbf{t}).\Gamma(\mathbf{t}))\, \mathbf{dt'} \tag{4}$$

The first summand of Eq. (4) provides the sum of the energies taken (or given) from the clock, E_{clk} and the energy transfer from neighbouring cells, E_{io}. This notion is further elaborated in Eq. (5), as given below:

$$E_{clk} + E_{io} = \frac{\hbar}{2}\int_{Tc}^{t0+Tc} (\frac{d}{dt}\Gamma(\mathbf{t}).\lambda(\mathbf{t}))\, \mathbf{dt'} \tag{5}$$

The positive values in the terms, E_{clk} and E_{io} mean the flow of energies from the assembly of the cell (QCA cell and clock as a whole) to the environment, and negative means vice versa. The second summand of Eq. (4) denotes E_{bath}, the energy released during the release phase and lost to the environment [44–46]. E_{bath} is further elaborated with **Γ** and **λ** vectors in Eq. (6).

$$E_{bath} = \frac{\hbar}{2}\int_{Tc}^{t0+Tc} (\frac{d}{dt}\lambda(\mathbf{t}).\Gamma(\mathbf{t}))\, dt' \tag{6}$$

3.2 Simulators for Estimating Energy in QCA

In QCA, QCADesigner-E and QCAPro are the two simulators for calculating energy dissipation. Since the QCAPro simulator uses zero rise and fall time in the clock slope, it is not used to determine the exact values. It cannot calculate the energy dissipation of multilayer crossovers if present in the layout. QCADesigner-E, an open-source simulator, computes the precise values of E_{bath}, E_{clk} and E_{io} by interpolating the integrands mentioned in Eq. (3)–(6). Significantly, the gaussian and ramp-shaped clock signals in QCADesigner-E allow clock slope values to be altered. The time step, clock period, clock slope, radius of effect (RoE) and other specific parameters, as mentioned in [46, 47], aid in increasing the precision of the energy estimation. This simulator yields computation error, which is supposed to be as small as possible [48].

3.3 Values of E_{bath}, E_{clk} and E_{io} in LT and MV Universal Gates

This sub-section describes the cell-by-cell summary of energy components of universal gates realised by LT and MV logic reduction techniques. The main goal is to identify how energy components flow in a specific QCA layout since they are the ones that would help to sum up the total energy dissipation. This work excludes the cooling costs since it could yield misleading conclusions. Figure 5a shows the main cell layer of the LT NAND layout, where each cell is placed according to the x–y coordinate system. For example, cell A of Fig. 4b is indexed in a cartesian coordinate system. Consequently, the position

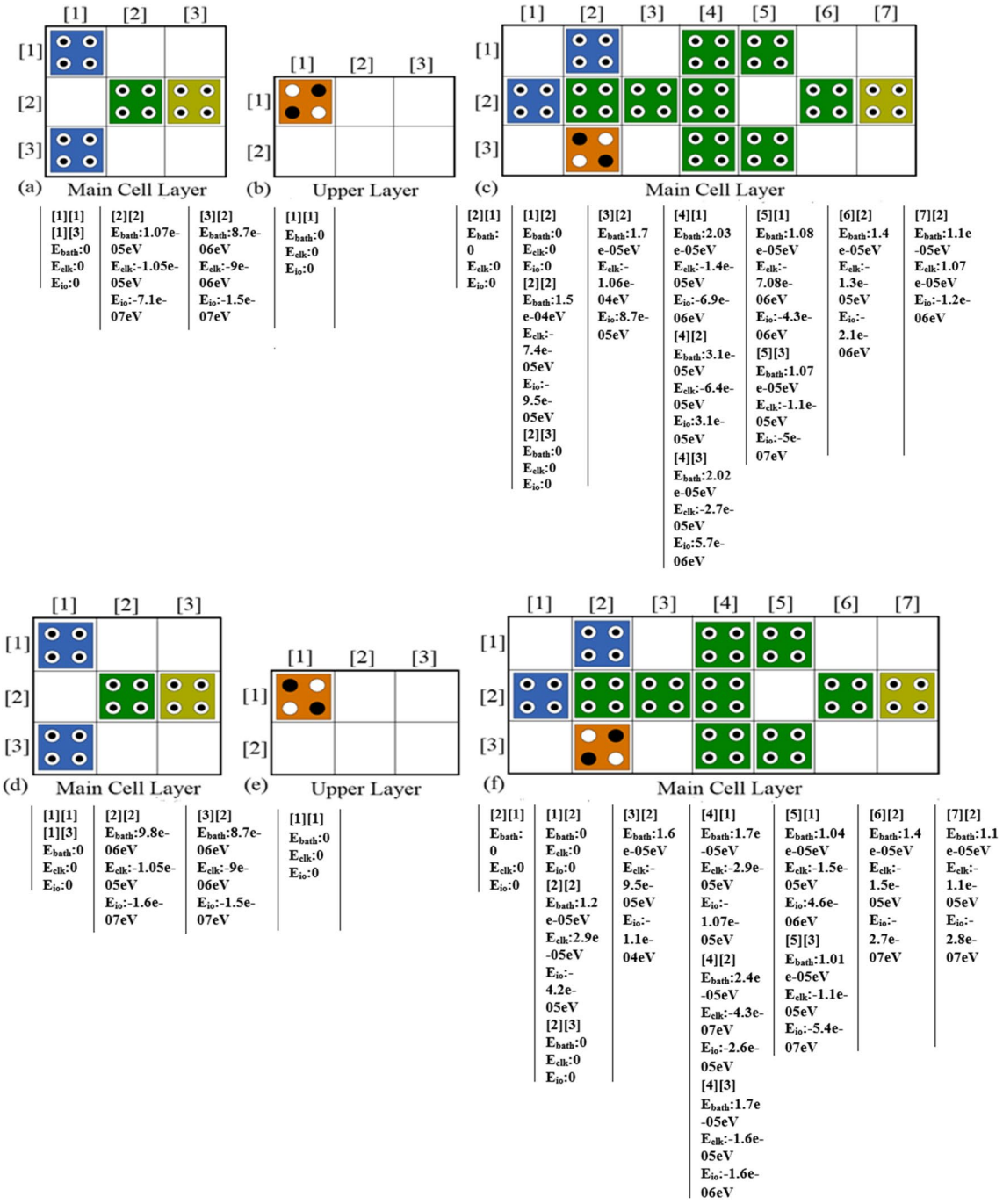

Fig. 5 Layer-wise cell-by-cell energy components of **a** LT NAND gate layer 1 (main cell layer), **b** LT NAND gate layer 2 (upper layer), **c** MV NAND gate (main cell layer), **d** LT NOR gate layer 1 (main cell layer), **e** LT NOR gate layer 2 (upper layer) and **f** MV NOR gate (main cell layer)

of cell A becomes [1] in layer 1. In this way, the cells of LT NAND in layer 1 and layer 2 are separately arranged in 3X3 and 2X3 matrices, as illustrated in Fig. 5a and b, respectively. Whereas the MV NAND layout cells are accommodated in a 3X7 matrix, as shown in Fig. 5c. The values of energy components, E_{bath}, E_{clk} and $E_{io,}$ for each cell in LT and MV NAND layouts are provided in Fig. 5a, b and c. E_{io} includes the energy entering and leaving a QCA cell. Any negative value of E_{bath}, E_{clk} and E_{io} means the energy transfer from the environment, the clock and the cell, while positive means the reverse. It is found that the energy dissipation of all input and fixed polarisation cells is 0 eV [47, 48].

The matrix representations of two layers of LT NOR and MV NOR gate with detailed cellwise energy components E_{bath}, E_{clk} and E_{io} are demonstrated in Fig. 5d, e and f.

3.4 Total and Average Energy Dissipation of LT and MV Logic Gate

Equations (3–6) are used to determine the average and total energy dissipations of LT and MV universal gates, using gauss, ramp, and cos clock signals. QCADesigner-E is then used to verify the results. Table 3 summarises the energy values of the specific layouts with corresponding errors, which are expected to be as small as possible. The simulation parameters can be adjusted per requirements in the output validation of a layout [49, 50]. It is significant to note that LT universal gates consume many-fold lower energy than MV gates.

As reported in Table 3, it is observed that the LT universal logic gates perform better than their MV counterparts regarding the total and average energy dissipations [29]. Consequently, the LT gates are chosen, and the impact of defects and polarisations on LT universal gates are investigated in the next section.

4 Defects of QCA

4.1 Types of Defects

The QCA cells are manufactured through synthesis and deposition phases. Additional dots, missing dots, additional electrons and missing electrons may occur in the primary layer during the first phase of the manufacturing process. However, the deposition phase is defect-prone, and any combinations of these four defects primarily occur in this stage. These are cell displacement defects (CDD), cell misalignment defects (CMD), rotational cell defects (RCD) and additional or missing cell defects (ACD or MCD), as shown in Fig. 6a–d. One type of such defect or a combination of all such defects may occur [51, 52]. Cell deposition defects occur once a cell (or more than one cell) is displaced from its original position, remaining aligned with the other cells. A single-cell displacement defect (SCDD) occurs if any cell differs from its intended position. However, multiple-cell displacement defect (MCDD) occurs when the positions of multiple cells differ from their actual positions [53].

SCDD and MCDD affect the functionality of QCA logic gates more than the other defects. The intermediary polarisation of an output cell is propagated to the successive neighbour cell or a group of cells in a multilevel QCA layout [53]. As a result, the output cell becomes essential in establishing a layout's ultimate polarization. As a result, the output cell is critical in deciding how polarised a layout would ultimately be. This section investigates how output cell polarisation and energy values change if SCDD happens at the LT gate's output cell.

4.2 SCDD on LT NAND and LT NOR Gates

The red dot represents the defect-free position of cell 4 as indicated by $\{x_0=0, y_0=0\}$ in Fig. 7b and d. The SCDD is inserted at cell 4 in the horizontal (east-west) and vertical (north-south) directions. Then, cell 4 is moved with a ± 0.1 nm step size in the north-south and east. However, the step size is kept at ± 0.01 nm since the cell spacing between two quantum

Table 3 Summary of total and average energy dissipation of LT and MV universal logic gates considering different types of clock signal

Logic Gates	Type of Clock Signals	Total Energy for LT (eV)		Total Energy for MV (eV)		Average Energy for LT (eV)		Average Energy for MV (eV)	
		Value	Error	Value	Error	Value	Error	Value	Error
NAND	Gauss	0.000739	-0.0000699	0.00409	-0.000386	0.0000672	-0.00000672	0.000372	-0.0000351
NOR		0.000953	-0.000094	0.00385	-0.00036	0.0000867	-0.0000854	0.00035	-0.0000327
NAND	Ramp	0.0237	0.0118	0.154	0.0415	0.000483	0.00024	0.00314	0.000846
NOR		0.0243	0.0114	0.155	0.0406	0.000497	0.000233	0.00316	0.000828
NAND	Cos	0.0006	-0.000427	0.0049	-0.000416	0.0000563	-0.00000388	0.000445	-0.0000378
NOR		0.000715	-0.0000536	0.0057	-0.000506	0.0000165	-0.000165	0.000518	-0.000046

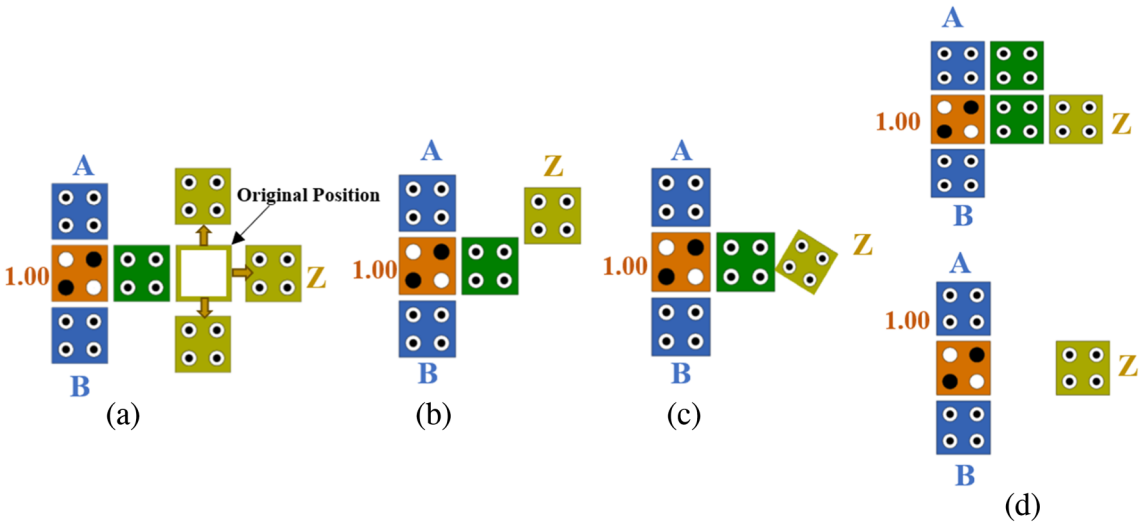

Fig. 6 Four types of defects **a** CDD, **b** CMD, **c** RCD and **d** ACD (upper), MCD (lower)

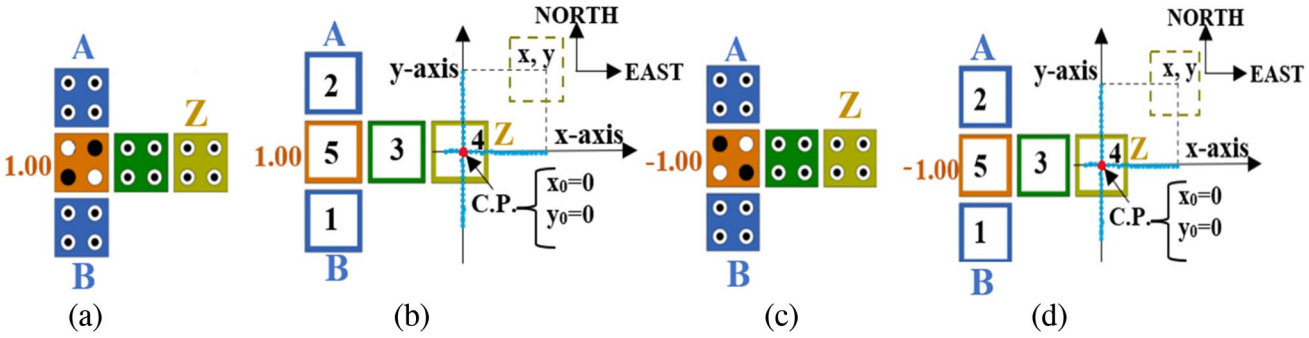

Fig. 7 **a** LT NAND layout and its, **b** Associated cell numbering, **c** LT NOR layout and its, **d** Associated cell numbering

cells remains at 2 nm west directions. The negative values of SCDD indicate west and north direction displacements from their original position. In contrast, the positive values of SCDD reveal east and south direction displacements. The location of cell 4 in the east–west and north–south directions, {x, y}, where the SCDD is introduced, is provided by the blue dots of CP. The maximum and minimum SCDD values of LT NAND and LT NOR in nm are provided in Eq. (7a) and (7b).

$$\begin{aligned} &\text{East SCDD} = 0.1 \le x \le 7.4,\\ &\text{West SCDD} = -0.01 \le x \le -1.54,\\ &\text{North SCDD} = -0.1 \le y \le -4.1,\\ &\text{South SCDD} = 0.1 \le y \le 4.1 \end{aligned} \tag{7a}$$

$$\begin{aligned} &\text{East SCDD} = 0.1 \le x \le 3.4,\\ &\text{West SCDD} = -0.01 \le x \le -1.53,\\ &\text{North SCDD} = -0.1 \le y \le -4.1,\\ &\text{South SCDD} = 0.1 \le y \le 4.1 \end{aligned} \tag{7b}$$

4.3 Variation of Output Polarisation with Respect to SCDD

The simulation output of the faulty architecture is compared with the defect-free layout, whose logical reliability has already been established in [23, 36, 37, 42, 54]. Thresholds of +0.6 and -0.6 polarisations have been selected rather than directly comparing the patterns of output waveforms. If these threshold values constrain the polarisation of cell 4, the layout is considered to be determinate. Otherwise, the polarisations in the presence of SCDD are considered indeterminate. The scatter plots in Fig. 8a–d illustrate the variations of output polarisations with respect to the north-south and east-west SCDD.

4.4 Impact of Output Polarisation on Total and Average Energy Dissipation

The energy dissipation of a cell and its associated polarisation are interrelated by the Hamiltonian Equation [55].

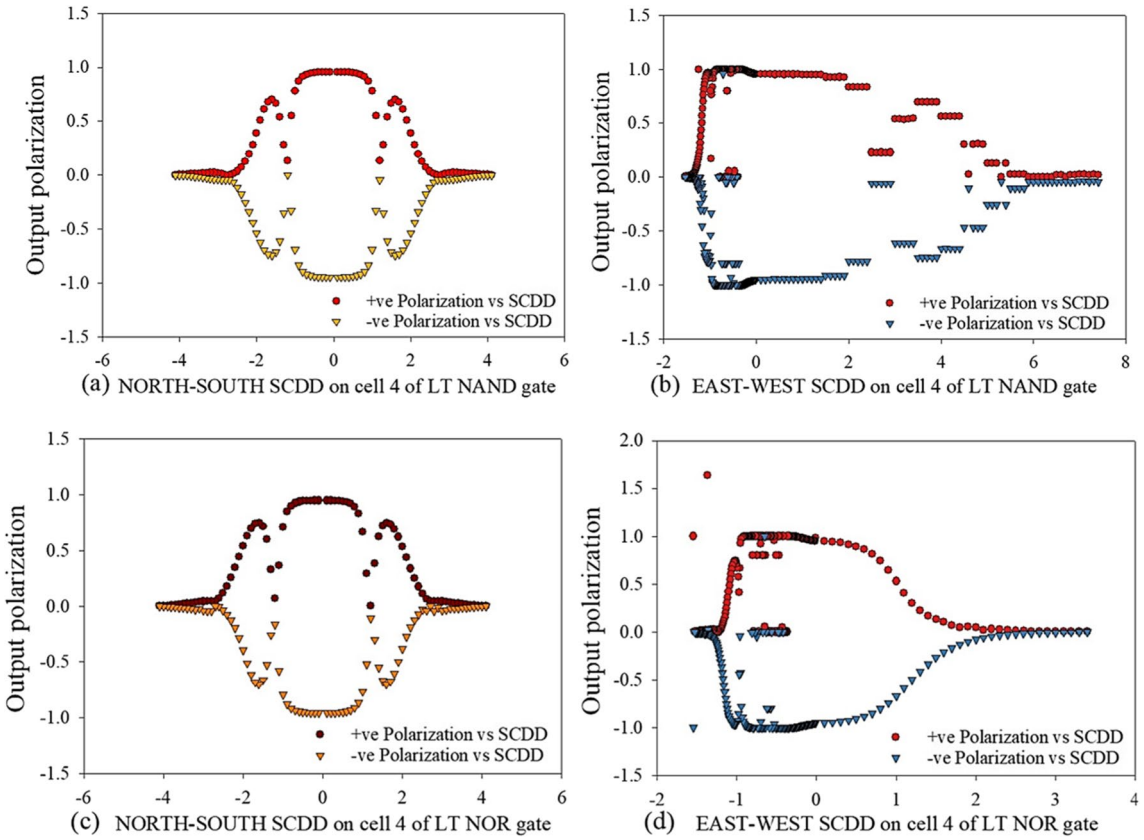

Fig. 8 Scatter plots of output polarisation w.r.t. **a** north-south SCDD on cell 4 of LT NAND gate, **b** east-west SCDD on cell 4 of LT NAND gate, **c** north-south SCDD on cell 4 of LT NOR gate and **d** east-west SCDD on cell 4 of LT NOR gate

However, the relation between output polarisation, energy dissipation and the impact of SCDD is not deterministic. This sub-section explores the effect of variation of output cell polarisation in the energy dissipation in the presence of SCDD. The scatterplots of variation in positive and negative output polarisation with total and average energy dissipation of LT NAND layout are shown in Fig. 9a and b, respectively. Similarly, the scatterplots of the LT NOR layout depicting similar variations are revealed in Fig. 9c and d.

4.5 Impact of SCDD on Total and Average Energy Dissipation

In sub-Sect. 4.2, the total and average energy of the LT NAND and NOR architectures are measured in a specified differential of north-south and east-west SCDD step size at cell 4. Figure 10a and c show scatter plots of energy dissipation for LT NAND and LT NOR layouts according to north-south SCDD and scatter plots of energy dissipation with east-west SCDD for LT NAND and LT NOR layouts are demonstrated in Fig. 10b and d, respectively illustrating the spline plots for the LT NAND layout. The *scdd_polarisation_energy* (SPE) dataset is built by collating the scatterplot [57], which is further utilised in the next section to predict the universal gate's energy dissipations.

5 Machine Learning Models

Machine learning models are algorithms or computational models that learn patterns and make predictions or decisions based on data. Supervised learning is a type of machine learning where the algorithm is trained on a labelled dataset consisting of both the features as inputs and the desired output as targets. The trained model then makes a prediction for the unknown input data or test dataset [58–60]. In this learning approach, regression techniques and classification algorithms have been used to build predictive models. Three algorithms have been yielded in this study of energy dissipation predictions where they performed well: K-Nearest Neighbour (KNN), Random Forest (RF) and Polynomial Regression (PR).

(i) K-Nearest Neighbour (KNN)

KNN algorithm is a versatile and frequently used machine learning algorithm known for its simplicity

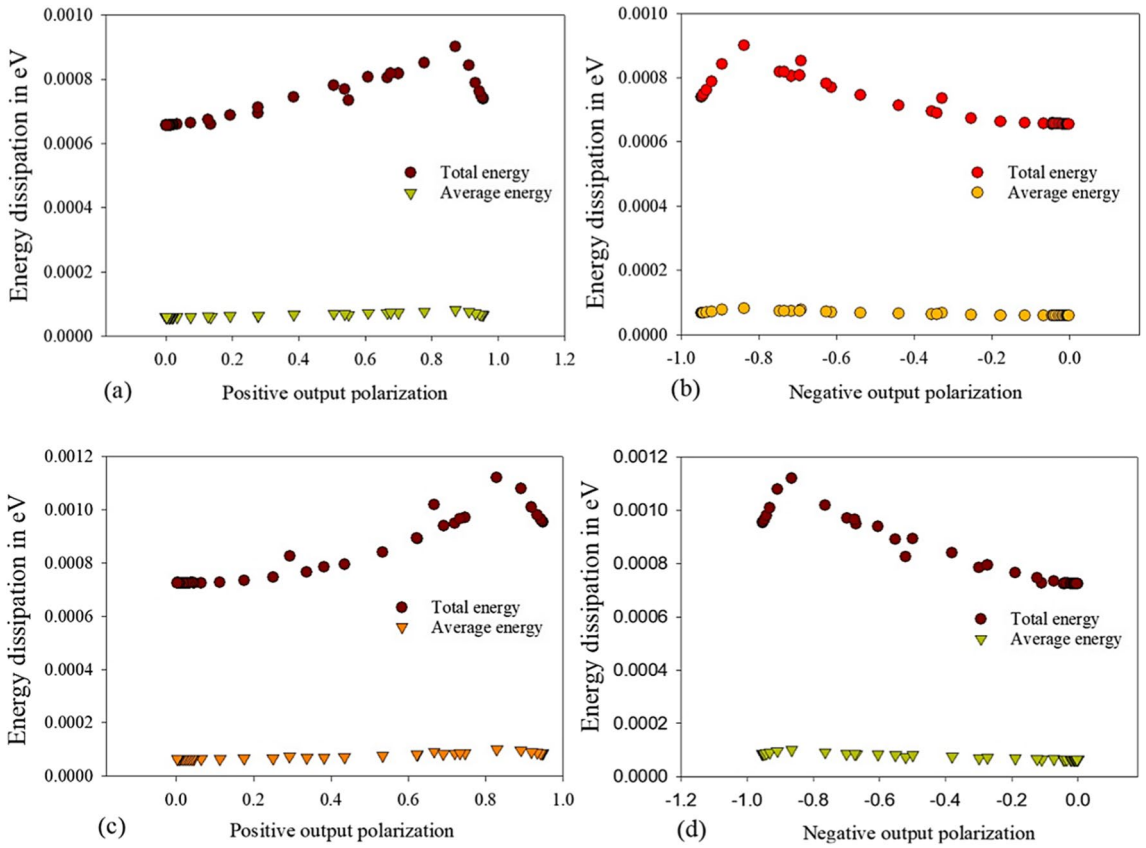

Fig. 9 Scatterplots of total and average energy dissipation of LT NAND gate w.r.t. **a** positive polarisation, **b** negative polarisation and same for LT NOR gate with respect to **c** positive polarisation **d** negative polarisation

and ease of implementation. It makes no assumptions about the underlying data distribution. It can also handle numerical and categorical data, giving it a versatile solution for a wide range of datasets in classification and regression problems. It is a non-parametric algorithm that predicts data points in a given dataset based on their similarity. When compared to other algorithms, K-NN is less sensitive to outliers. The KNN technique finds the K closest neighbours to a given data point using a distance measure such as Euclidean distance. The majority vote is then used to determine the data point's class or value [56, 59, 60].

(ii) Random Forest (RF)

Random Forest is a powerful ensemble learning method used for both classification and regression tasks. It operates by constructing multiple decision trees during training and outputting the class, that is, the mode of the classes (classification) or mean prediction (regression) of the individual trees. Random forest techniques have three major hyperparameters that must be set prior to training. These variables include node size, number of trees, and number of characteristics sampled. The random forest classifier can then be used to address regression or classification problems. The prediction will differ depending on the type of difficulty. Individual decision trees will be averaged for a regression task, and a majority vote, that implies the most common categorical variable will produce the predicted class for a classification problem. Random Forest works in two phases. The first is to create the random forest by combining the N decision tree, and the second is to make predictions for each tree created in the first phase. It conquers the high variance problem, improves accuracy, provides flexibility and reduces the risk of overfitting [56, 60].

(iii) Polynomial Regression (PR)

Polynomial regression is a machine-learning algorithm that modulates the probabilistic relationship between the independent and dependent variables using an n^{th}-degree polynomial. Historically, the independent and dependent variables are known as predictor and response [61]. Polynomial regression

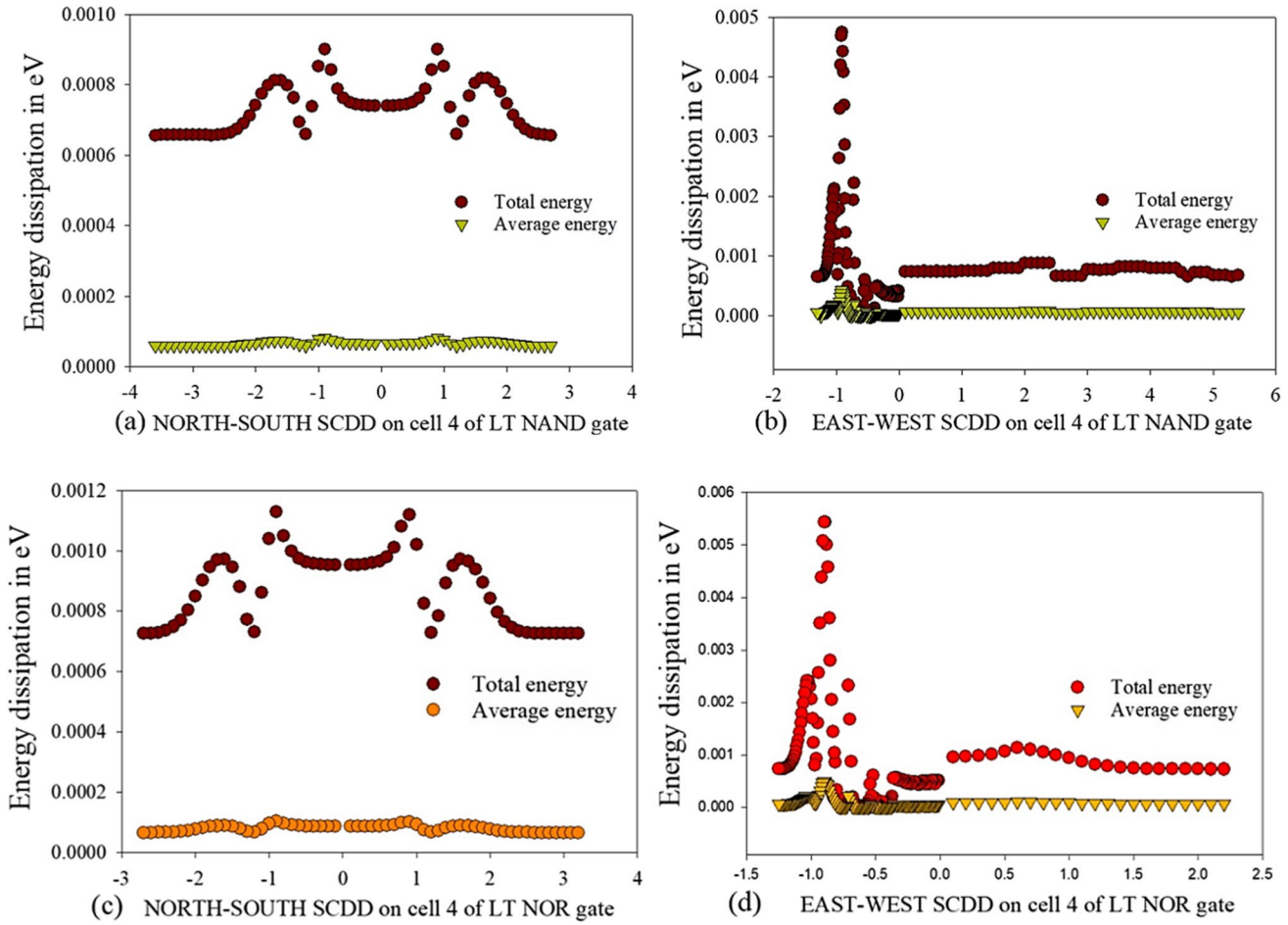

Fig. 10 Scatterplots of total and average energy dissipation of **a** north-south SCDD on cell 4 of LT NAND gate, **b** east-west SCDD on cell 4 of LT NAND gate, **c** north-south SCDD on cell 4 of LT NOR gate and **d** east-west SCDD on cell 4 of LT NOR gate

has two types, and they are univariate and multivariate. If one predictor is used in the n^{th}-degree polynomial, it is termed a univariate polynomial regression model, as given in Eq. (8). Here, θ_i, with $i \in n$ denoting regression coefficients, x and y represent predictor and response.

$$y = \theta_0 + \theta_1 x + \theta_2 x^2 + \cdots + \theta_n x^n = \theta_0 + \theta_i x^i + \epsilon_i \tag{8}$$

If multiple predictors are used in the polynomial regression, the algorithm becomes multivariate polynomial regression, as follows in Eq. (9). Here, x_i and y_i, with $i \in n$, denote predictors and responses and ϵ_i presents the error terms.

$$y_i = \theta_0 + \theta_1 x_i + \theta_2 x_i^2 + \theta_3 x_i^3 \cdots + \theta_n x_i^n + \epsilon_i \tag{9}$$

Let, $\hat{y_i} = \hat{\theta}_0 + \hat{\theta}_1 x_i + \hat{\theta}_2 x_i^2 + \hat{\theta}_3 x_i^3 \cdots + \hat{\theta}_n x_i^n$ be the predicted value of the response, y on the i^{th} value of the predictor, x with the estimated coefficients, $\hat{\theta}_0, \hat{\theta}_1, \hat{\theta}_2, \ldots, \hat{\theta}_i$. Then the error, $\epsilon_i = y_i - \hat{y_i}$, is the difference between i^{th} original response and the predicted response.

5.1 Deploying Machine Learning Model

Eight models are developed for energy estimations whose predictors and associated responses have been demonstrated in Table 4. These models can estimate the total and average energy dissipations based on the *scdd_polarisation_energy (SPE)* dataset [57] deploying the predicting models. The *SPE* dataset contains six parameters and 2160 data points for LT NAND and NOR gates. The parameters are given as follows:

Table 4 The predictors and responses of the ML models deployed on the SPE dataset to predict energy dissipation

SCDD Category	Estimators	Responses	Model Parameters
Estimation of Total Energy Dissipation			
SCDD-1	i) North-South SCDD ii) Positive Polarisation	Total Energy in eV	random_state[a] = 23 for sample selection
SCDD-2	i) North-South SCDD ii) Negative Polarisation	Total Energy in eV	
SCDD-3	i) East-West SCDD ii) Positive Polarisation	Total Energy in eV	
SCDD-4	i) East-West SCDD ii) Negative Polarisation	Total Energy in eV	
Estimation of Average Energy Dissipation			
SCDD-5	i) North-South SCDD ii) Positive Polarisation	Average Energy in eV	random_state[a] = 23 for sample selection
SCDD-6	i) North-South SCDD ii) Negative Polarisation	Average Energy in eV	
SCDD-7	i) East-West SCDD ii) Positive Polarisation	Average Energy in eV	
SCDD-8	i) East-West SCDD ii) Negative Polarisation	Average Energy in eV	

[a]Random_state sets seed to the random generator so that database-splitting remains deterministic

(i) Direction of SCDD
(ii) Displacement from base position in nm
(iii) Positive Output Polarisation
(iv) Negative Output Polarisation
(v) Total energy dissipation in eV
(vi) Average energy dissipation in eV

The correlation coefficients provide the direction and strength of associations between estimators and responses of a regression model. Its value ranges from -1 to +1. The parameter, shifting distance from CP in nm, represents SCDD. According to Eq. (10), Pearson's correlation coefficient examines the relationship between SCDD, positive and negative output polarisation, and total and average energy dissipations [58–61]. Figure 11a and b show the correlation matrices of LT NAND and LT NOR gates, respectively. Due to the non-zero correlation coefficient values observed from correlation matrices, it is derived that there exist non-linear dependencies between SCDD, positive and negative output polarisation with energy dissipations. Therefore, SCDD, positive and negative output polarisations are chosen as good estimators to predict the responses, total and average energy dissipations.

$$r = \frac{\sum(x_i - \overline{x})(y_i - \overline{y})}{\sqrt{\sum(x_i - \overline{x})^2 \sum(y_i - \overline{y})^2}} \quad (10)$$

Here, $\overline{x}$ and $\overline{y}$ denote the arithmetic mean of estimators and responses.

Due to the non-linear dependencies between the parameters mentioned above, the aforesaid predictive models effectively estimate the total and average energy dissipation of LT NAND and NOR gates when SCDD is present at the output cell. The dataset is split into two parts: train and test data. The train data is used to train models 1–8 with different machine learning models, and the results obtained from the training of the models are utilised to yield prediction according to the test data. The proportion of the dataset needed in test data varies from 20 to 30%. The effectiveness of those models is analysed by taking the performance metrics, r^2-score, the Mean Absolute Error (MAE), the Mean Squared Error (MSE) and Root Mean Squared Error (RMSE) [62, 63], which are described in the following sub-section. The task of machine learning is performed by utilising python based scikit-learn package.

5.2 Evaluation Parameters

In this study, we evaluate the performance of each of the considered learning models in terms of r^2- score, the Mean Absolute Error (MAE), the Mean Squared Error (MSE) and Root Mean Squared Error (RMSE) [62, 63].

1. r-SQUARED SCORE (r^2)

Fig. 11 Correlation matrices to represent the dependencies of predictors and responses in case of **a** LT NAND and **b** LT NOR gates

The mathematical expression of the r^2-score that specifies the variation between predictors and responses is given in Eq. (10). The higher value indicates the better performance of the model. It always has a score between 0 and 100%. A score of 0% indicates that the model explains no variability around the mean of the response variable, while a score of 100% indicates that the model explains all variability around the mean of the response variable.

$$r^2 = 1 - \frac{\frac{1}{n}\sum (y_i - \hat{y}_i)^2}{\frac{1}{n}\sum (y_i - \overline{y})^2} \tag{10}$$

2. MEAN ABSOLUTE ERROR (MAE)

Mean absolute error or MAE measures the absolute value of the arithmetic mean of the errors on model estimations. It is a significant performance metric since it evaluates the effect of outliers in the dataset. The lower value of MAE means the estimated values are closer to the original values. Equation (11) provides the mathematical expression of MAE.

$$\text{MAE} = \frac{1}{n}\sum \left|(y_i - \hat{y}_i)\right| \tag{11}$$

3. MEAN SQUARED ERROR (MSE)

The mean-squared error or MSE measures the mean squared residues between the original and predicted values. As the MSE value approaches 0, a better model is

obtained. The mathematical expression of MSE is given in Eq. (12).

$$\mathrm{MSE} = \frac{1}{n}\sum (\mathrm{y_i} - \hat{\mathrm{y}}_\mathrm{i})^2 \tag{12}$$

4. ROOT MEAN SQUARE ERROR (RMSE)
   The standard deviation of the prediction errors can be defined as the root mean square error. The difference between the best fit line and the actual data points is defined as prediction errors, also known as residuals. Thus, RMSE measures how concentrated the real data points are around the best fit line. It is the error rate produced by the square root of MSE, which is presented below in Eq. (13).

$$\mathrm{RMSE} = \sqrt{\frac{1}{n}\sum (\mathrm{y_i} - \hat{\mathrm{y}}_\mathrm{i})^2} \tag{13}$$

6 Results and Discussion

6.1 Comparison of Design Metrics of Universal Logic Gates

The existence of crossovers has a significant influence on the QCA design parameter. It is difficult and expensive to fabricate multilayer QCA layouts. Specific QCA design factors such as effective area, O-Cost, and latency are explained to guide the performance of the logic circuit design.

(i) Effective area: The area of activity where QCA cells are placed upon the foundation material is termed a functional area, namely an effective area. In this area, the computation starts at the leading edge of the QCA clocking wires.
(ii) O-Cost: The total number of QCA cells, including the logic gate, interconnecting wires, and input-output excitation port, is accounted as operational costs, namely the O-Cost of a layout.
(iii) Delay: The total count of the clock cycles assigned to a specific QCA layout during the zone partitioning in the direction of signal propagation is called latency or delay, T [64].

The LT realisations of NAND and NOR gates consume 57.15% less effective area and need 58.33% less O-Cost than the MV counterparts from the aforementioned table. However, the delay requirements are the same for both cases (Table 5).

6.2 Comparison of Energy Dissipation Values of Universal Logic Gates

The calculations of complex energy components mentioned in Sect. 3 paved the way towards the total and average energy dissipation summary of LT and MV NAND and NOR gate, as reported in Table 3. LT NAND and NOR gate yield ~ 82% and ~ 75.25% lesser total energy than MV counterparts in the presence of a gauss clock signal. Additionally, LT NAND and NOR gate produce ~ 84.6% and ~ 84.33% less energy than MV counterparts in the presence of a ramp clock signal. Moreover, LT NAND and NOR gate dissipate ~ 87.76% and ~ 87.46% lesser total energy than MV counterparts in the cos clock signal. Also, the LT Universal logic gate remains energy efficient in the average energy calculations. LT NAND and NOR gate generate ~ 81.94% and ~ 75.23% less average energy than MV counterparts in the Gauss clock signal. Additionally, LT NAND and NOR gate yield ~ 84.62% and ~ 84.28% less average energy than MV counterparts in the ramp clock signal. Moreover, LT NAND and NOR gate dissipate ~ 87.35% and ~ 96.82% less average energy than MV counterparts in the cos clock signal.

6.3 Observations of SCDD in Universal Logic Gates

The comparative analysis of energy dissipation motivates predicting the impact of SCDD and polarisation on energy dissipation of LT Logic gate by deploying machine learning models. In north-south SCDD, it is observed that beyond 13.67% displacement of the cell in either direction, the total and average energy values of LT NAND and NOR gate layouts remain unaffected and become fixed at ~ 0.0006 eV total and ~ 0.00006 eV, respectively. In east-west SCDD, 24.67% and 85.55% displacement of the cell in either direction mainly affects the energy dissipation for both gates.

Table 5 Summary of effective area, O-Cost and delay requirements for Logic gates implemented using MV and LT logic gate

Sl. No	Logic gates	Effective area in MV realisation (nm^2)	Effective area in LT realisation (nm^2)	O-Cost in MV realisation	O-Cost in LT realisation	Delay in MV realisation	Delay in LT realisation
1	NAND	8400	3600	12	5	0.25	0.25
2	NOR	8400	3600	12	5	0.25	0.25

6.4 Performance Evaluation of Proposed ML Models

This study exhibits the outcome of the parameters (mentioned in Sect. 5.1) with the SPE dataset to predict the total and average energy dissipation of LT NAND and LT NOR gates based on specified SCDD categories. We used the programming language Python for our research. We exploited the Scikit-learn [59–62] package for the implementation of our machine-learning models. The best performing ML models i.e. RF, KNN and PR on the SPE dataset with different hyperparameters, and the corresponding r^2 scores (in percentage) are shown in Tables 6 and 7. The effective ML models are presented here in the following Tables 6 and 7. The first step when employing our models was to determine the value of the hyper-parameter *n_estimator*, *n_neighbour* and *degree of polynomial* for respective models. It is observed from Table 6 that individual ML models have achieved different r^2 scores based on various SCDD categories.

The RF model performed better than the KNN model in predicting the total energy dissipation for the LT NAND observed in Table 6 with an r^2 score of 99.11 for SCDD-1 and an RMSE value of 0.0994 at $n\_estimator = 4$. For SCDD-2, the RF model performs better than KNN with an r^2 score of 98.53 with an RMSE value of 0.0842 at $n\_estimator = 3$. In the context of SCDD-3 and 4, the RF model produces the perfectly fit r^2 scores of 83.09 and 83.11 with respective RMSE values of 0.1656 and 7.21e-07 at $n\_estimator = 4$ and 200. In SCDD-5, the RF model performs better than 99.48 r^2 score with RMSE of 0.0694 at $n\_estimator = 19$. In SCDD-6, the KNN yields a higher accuracy of 99.58 than the RF counterpart, with an RMSE value of 0.0639 at $n\_neighbour = 6$. The RF models have performed well in SCDD-7 and 8

Table 6 Model and SCDD category-wise performance evaluations w.r.t. r^2-score, MSE, MAE and RMSE for LT NAND gate

SCDD Category	ML Model	TRAIN r^2 Score	TEST r^2 Score	MSE	MAE	RMSE
SCDD-1	i)RF	98.81	99.11	0.0098	0.0223	0.0994
	ii)KNN	97.88	99.01	0.0171	0.0797	0.0063
SCDD-2	i)RF	98.46	98.53	0.0071	0.0209	0.0842
	ii)KNN	87.73	94.95	0.0561	0.2161	0.0467
SCDD-3	i)RF	79.09	83.09	0.0274	0.0169	0.1656
SCDD-4	i)RF	79.45	83.11	5.20E-13	1.55E-07	7.21E-07
SCDD-5	i)RF	99.08	99.48	0.0048	0.0139	0.0694
	ii)KNN	96.77	97.33	0.0302	0.1574	0.0247
SCDD-6	i)KNN	99.43	99.58	0.004	0.0151	0.0639
	ii)RF	87.79	95.03	0.0569	0.2149	0.0462
SCDD-7	i)RF	84.08	94.12	2.43E-13	1.68E-07	4.93E-07
SCDD-8	i)RF	79.45	83.17	5.18E-13	1.56E-07	7.20E-07

Table 7 Model and SCDD category-wise performance evaluations w.r.t. r^2-score, MSE, MAE and RMSE for LT NOR gate

SCDD Category	ML Models	TRAIN r^2 Score	TEST r^2 Score	MSE	MAE	RMSE
SCDD-1	i)RF	99.41	99.56	0.0092	0.0215	0.0961
	ii)KNN	91.37	98.15	0.0209	0.0365	0.1445
SCDD-2	i)KNN	97.73	98.38	0.0183	0.0227	0.1354
	ii)RF	98.83	99.8	0.0369	0.0398	0.1922
SCDD-3	i) RF	85.93	96.14	0.2004	0.0456	0.4476
SCDD-4	i) RF	89.83	98.02	2.54E-13	1.54E-07	5.04E-07
SCDD-5	i) KNN	91.3	98.08	0.0373	0.1472	0.0216
	ii) RF	98.85	99.77	0.0168	0.0259	0.1299
SCDD-6	i) RF	99.6	99.79	0.0069	0.0166	0.0834
	ii) KNN	97.71	98.36	0.023	0.1358	0.0184
SCDD-7	i) PR	99.61	99.68	0.003	0.0212	0.0549
SCDD-8	i) PR	92.05	92.52	0.0017	0.0174	0.045
	ii) RF	82.84	97.82	1.49E-13	1.02E-07	3.85E-07

categories, scoring 94.12 and 83.17 r^2 scores, respectively, with RMSE values of 4.93e-07 and 7.2e-07 at corresponding *n_estimator* 4 and 200.

It is important to note from Table 7 that the RF model worked well for both SCDD-1 and 2 in terms of total energy dissipation prediction of LT NOR gate, obtaining 99.56 and 99.8 r^2 scores, 0.0961 and 0.1922 RMSE values for respective *n_estimator* values of 18 and 2. The RF is the only model effective for SCDD-3 and 4. The RF model achieved 96.14 and 98.02 r^2 scores with corresponding RMSE values of 0.4476 and 5.04e-07 for *n_estimator* = 30 and 5, respectively. The RF models yield the better r^2 scores of 99.77 and 99.79 at *n_estimator* = 5 and 6, respectively, where achieved RMSEs are reported as 0.1299 and 0.0834, respectively. The PR model remain perfectly fit for SCDD-7 with test r^2-score 99.68, RMSE 0.0549 at *degree of polynomial* 5. For SCDD-8, the RF model achieves 97.82 r^2-score with RMSE 3.85e-07 at *n_estimator* 30.

6.5 Graphical Illustration of Comparative r^2 Score and Loss Metrices Value

To further illustrate the accuracy analysis for the various proposed models, we have exhibited histogram analysis to illustrate the loss metrices performances and a comparative approach to visualize the r^2 score performance. Figures 12 and 13 provides the accuracy analysis of different SCDD models w.r.t. r^2-score for LT NAND gate and LT NOR gates, respectively.

Moreover, Figs. 12 and 13 depict a visual representation of different r^2 score for individual SCDD with associated train and test r^2 scores, which provides a notion for choosing an appropriate machine learning model for evaluating energy dissipation based on single cell displacement effect and cell polarization LT NAND and LT NOR gates.

We have evaluated the MSE, MAE and RMSE metrices as machine learning parameters to summarize the accuracies of predictive models. We have attempted to demonstrate a histogram analysis and illustrate the range of loss metrices for best suited ML models as shown in Fig. 14. Observing these

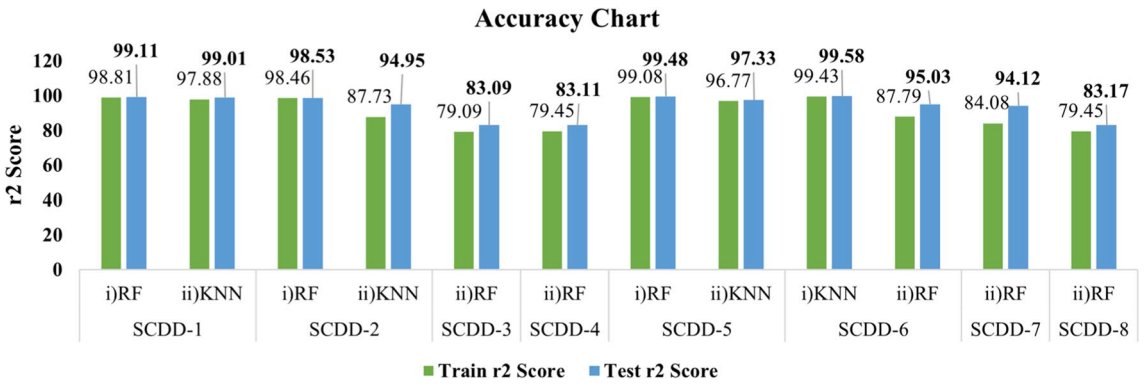

Fig. 12 Accuracy analysis of different SCDD models w.r.t. r^2-score for LT NAND gate

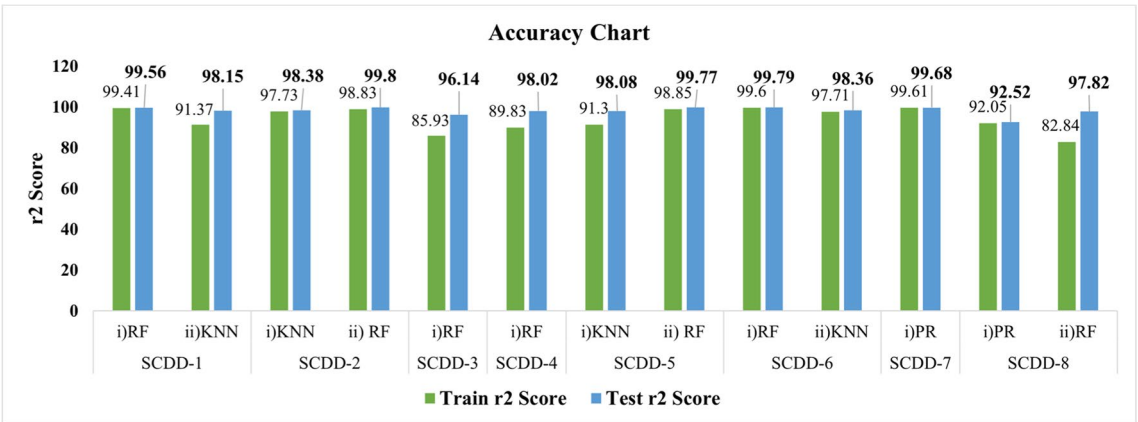

Fig. 13 Accuracy analysis of different SCDD models w.r.t. r^2-score for LT NOR gate

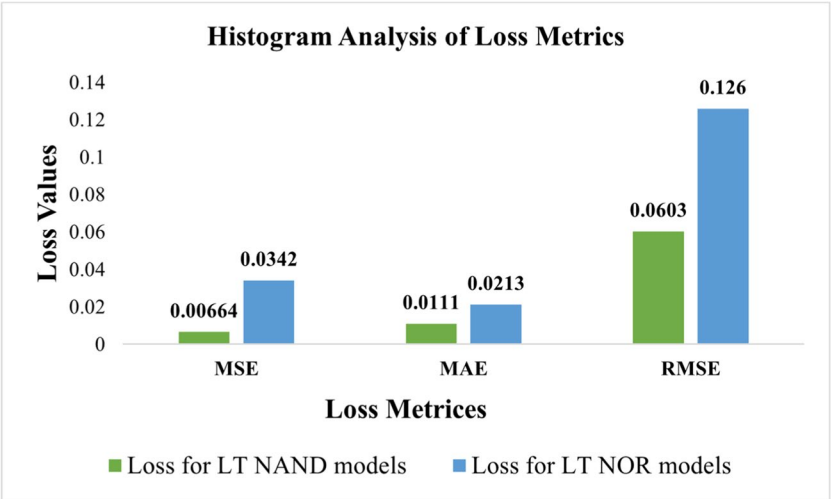

Fig. 14 Histogram analysis of SCDD models deployed for loss metrices for LT NAND and LT NOR SCDD

values, a few things stand out that there's a range of values of MSE, starting from as low as 0.00664 and going up to 0.0342, the range of MAE lies within 0.0111 to 0.0213 while RMSE lies in-between 0.0603 to 0.126. Lower values (closer to zero) generally indicate better performance in terms of predictive accuracy. The spread between the lowest and highest loss metrices values is notable. It is noted that the models yield lesser MSE, MAE and RMSE values for LT NAND gate compared to the respective values for LT NOR gate.

7 Conclusion

This work explores a pivotal point in identifying how SCDD at the output cell in a QCA circuit may impact energy dissipation. In the CMOS model, the impact of defects causes increased or decreased static and dynamic power dissipation. However, in QCA, the polarisation of a cell is also more likely to influence the energy dissipation of a layout along with the amount and direction of SCDD. It is reported that the LT universal logic gates outperform the conventional MV universal gates concerning energy and other QCA design metrics. The defects introduced in the LT gates include four possible directions, which cause the polarisation and energy to vary nonlinearly. Accordingly, distinct machine learning models are chosen to predict the energy of layouts. Such an ML-based predictive analysis contrasts the existing relevant works, which have focused on observing the effects of defects on the reliability and yield rates of nanoelectronics circuits, not on the impact of defects on predicting energy. For LT universal gates, the layout designer can predict the energy more precisely once the defect occurs within a specific direction and range. Predictive models with intricate circuitry can be tested in accordance with this research. Considering the encouraging results obtained after deploying the predictive models, the researchers and manufacturers may be encouraged to use LT universal gates in constructing QCA counterparts of different blocks of a nano processor [45, 65–70] where energy dissipation is bounded within the SNR limit.

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Data Availability Statement The collated dataset is available in the supplementary dataset.

Declarations

Competing Interest The authors have no significant competing interests.

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Manali Dhar is a Research Scholar in the Department of Electronics and Communication Engineering at the National Institute of Technology, Durgapur, India. She is presently serving as an Assistant Professor in ITER, Siksha 'O' Anusandhan Deemed to be University, Bhubaneswar, India. She has 11.5 years of experience as an Assistant Professor. She received her MTech in Microelectronics and VLSI from MAKAUT(In-House). Her current research interests include the VLSI Designs, Machine learning, and Quantum-dot Cellular Automata (QCA). She has published conference papers, journals in prestigious international publications. She reviews articles for reputed conferences.

Chiradeep Mukherjee received PhD from the National Institute of Technology, Durgapur, India. He is a member of ISLE (MISLE), member of IEEE (MIEEE) and associate member of IETE (AMIETE). His fields in research include Quantum Cellular Automata, Machine Learning, Deep Learning. He has published more than twenty reputed national and international conference and journal papers. He is also serving as a reviewer in reputed SCI/SCOPUS indexed journals in Taylor and Francis, Springer and Wiley publications.

Ananya Banerjee is a Research Scholar in the Department of Electronics and Communication Engineering at the National Institute of Technology, Durgapur, India. She has 15 years of experience as an

Assistant Professor. She received her MTech in Radio Physics and Electronics from Calcutta University. Her current research interests include Microwave and Quantum-dot Cellular Automata (QCA). She has published conference papers, journals in prestigious international publications. She reviews articles for reputed conferences.

Debasmita Manna is a Research Scholar in the Department of Electronics and Communication Engineering at the National Institute of Technology, Durgapur, India. She has 15 years of experience in academics. She received her Master in Technology in Mobile Communication and Network. Her current research interests include the Antenna Design, Biomedical Controller Devices, and Quantum-dot Cellular Automata (QCA). She has published several numbers of conference papers, journals in prestigious international publications. She is attached with different Professional Society's and reviews articles for reputed conferences.

Saradindu Panda has been working as a professor and the Principal at Dr. Sudhir Chandra Sur Institute of Technology& Sports Complex (SurTech). He worked in the designations of Head of Department, and Dean, at Narula Institute of Technology. He achieved PhD degree from the National Institute of Technology (NIT), Durgapur, West Bengal in 2007. He has a total 18 teaching experience of 18 years. He is the Chair of the IEEE CASS Kolkata Section. He is also the IQAC Member of Swami Vivekananda College, Rahara, Ramakrishna Mission, West Bengal. He has 53 SCI, Scopus and Web of Science publications. He has 68 International and National conference publications. He has published two books and 8 book chapters. He is the editor of two books. He published 9 patents.

Bansibadan Maji holds a PhD and is a senior professor of Electronics and Communication Engineering Department in National Institute of Technology, Durgapur, West Bengal, India. His main research areas are on microwave, antenna, VLSI design and low power device, and circuits. He has more than 56 publications in different international and national journals and conference proceedings. He has published more than 50 research articles in peer-reviewed international journals, national and international conferences.