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Comparison of Single Event Effect and Space Electrostatic Discharge Effect on FPGA Signal Transmission

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Abstract
As the central control component in aerospace products, SRAM-based FPGA finds extensive application in space. In its operational context, the space radiation environment introduces single event effect (SEE) and space electrostatic discharge effect (SESD) in FPGAs. This paper investigates SEE and SESD in SRAM-based FPGA using an integrated simulation method that combines device-level and circuit-level analyses. The findings reveal that the distinction in signal transmission primarily lies in the number of upsets and their correlation with the initial state. SEE can lead to single-bit or multi-bit upsets in SRAM, while SESD typically induces multi-bit upsets (MBU) in SRAM. Furthermore, the logic upset caused by SEE exhibits almost no correlation with the initial state of SRAM. Conversely, the upset caused by SESD is linked to the initial state, and the threshold voltage of Single Event Upsets (SEU) in different initial states is not uniform.

Keywords Single event effect · Space electrostatic discharge effect · Circuit simulation · FPGA

1 Introduction

Given its attributes of high density, compact size, and low power consumption, static random-access memory-based field-programmable gate arrays (SRAM-based FPGAs) find extensive use in aerospace electronic products [1–3]. Nonetheless, the space radiation environment poses a risk of inducing anomalies in spacecraft FPGA systems. Notably, anomalies stemming from the single event effect (SEE) and space electrostatic discharge effect (SESD) constitute a significant portion of these occurrences, posing a threat to the safety and reliability of spacecraft [4, 5].

Anomalies resulting from SEE and SESD exhibit similar soft errors, posing challenges in distinguishing between these two effects [6, 7]. A considerable portion of failures labeled as "soft errors" is often erroneously attributed solely to SEE, hindering effective radiation hardening [8–10]. Addressing these challenges, the Han group conducted experimental comparisons of SEE and SESD effects in a representative SRAM memory circuit [11] and an operational amplifier linear circuit [12]. They revealed through experiments the characteristic patterns of "soft errors" in circuits caused by two types of radiation effects: SEE and SESD. It was found that both SEE and SESD in SRAM could cause changes in the electric potentials of the n-well and p-well within the memory cell. Additionally, they observed that the electric potential collapse of well caused by SESD is significantly larger in both time and area compared to SEE. In the study of operational amplifier linear circuits, it was discovered that SEE and SESD can generate different transient signals at the device's output. This disparity arises from the varying sensitivity of transistors to SEE and SESD. Transistors in the amplification stage are more sensitive to SEE, while those in the output stage are more susceptible to SESD.

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Overall, current research on single event effect (SEE) in FPGAs across various institutions primarily relies on experimental studies, with a particular emphasis on single event upset (SEU), while there is limited investigation into the impact of SEEs on signal transmission within FPGAs. In contrast to the well-established research on the effects of SEEs on devices and circuits, research on the effects of space electrostatic discharge effect (SESD) on devices and circuits is relatively lacking, further restricting comparative studies on the characteristics, laws, and mechanisms of both phenomena. Regarding SESD, most studies focus on the macroscopic correlation between spacecraft anomalies and induced charging and discharging disturbances in the space environment, with a focus on spacecraft reliability [13–15]. Only a small amount of work involves the study of discharge phenomena itself, where significant interference of discharge pulses on timing circuits can be observed through satellite deep SESD simulation devices [16]. Currently, there is no literature exploring the impact of SESD on FPGA devices and circuits. Evaluating the macroscopic correlations and distinctions between SEE and SESD-induced FPGA failures is crucial for further enhancing the on-orbit reliability of FPGA application in spacecraft. Considering the constraints of irradiation resources, high costs, and limited irradiation conditions, employing comprehensive simulation methods using Technology Computer-Aided Design (TCAD) combined with Simulation Program with Integrated Circuit Emphasis (SPICE) provides a flexible approach to analyze the effects of SEE and SESD on FPGA signal transmission. This approach allows for a comprehensive analysis of SEE at different scales, providing a better understanding of their propagation and impact throughout the entire circuit. Therefore, this study investigates the similarities and differences in the effects of SEE and SESD on FPGA signal transmission using device-level and circuit-level comprehensive simulation methods, and the laws and mechanisms are analyzed.

2 Radiation Effect Modeling

2.1 TCAD and SPICE Simulation

We modeled the MOS device structure of the FPGA core unit using the TCAD simulation platform and simulated to obtain its basic electrical characteristic curves. The establishment of the device simulation model referred to experimental data of the same size process [17]. The cell structure used in electrical simulation is shown in Fig. 1, with a lateral width of 0.1 μm, a longitudinal height of 0.2 μm, a thickness of 0.1 μm, a junction depth of 0.012 μm, a gate oxide layer thickness of 0.002 μm, a channel width of 0.028 μm, and other dimensions and doping concentration ranges are shown in the figure.

After obtaining the transfer and output characteristic curves from the simulation, we extracted the SPICE parameters of the TCAD device and built the SPICE model of the device. Figure 2 shows the transfer characteristic curve of the MOS device. The agreement between TCAD and SPICE indicate that a reasonably accurate SPICE model of the device has been established, which can be used for further FPGA circuit-level simulations.

Based on the device electrical model, we utilized the device simulator in TCAD to define the spatial and temporal distribution of electron-hole pairs generated by collision ionization when heavy ions hit the device. This parameter was used to construct a SEE model of the device. SEE simulations were conducted on the device for different LET values. Figure 3 shows the transient drain current values corresponding to different typical LET values. It can be observed that the transient drain current increases with the increase in LET values.

2.2 Modeling of FPGA Basic Unit

Based on the MOS device electrical model of the FPGA established using TCAD, we utilized the circuit-level

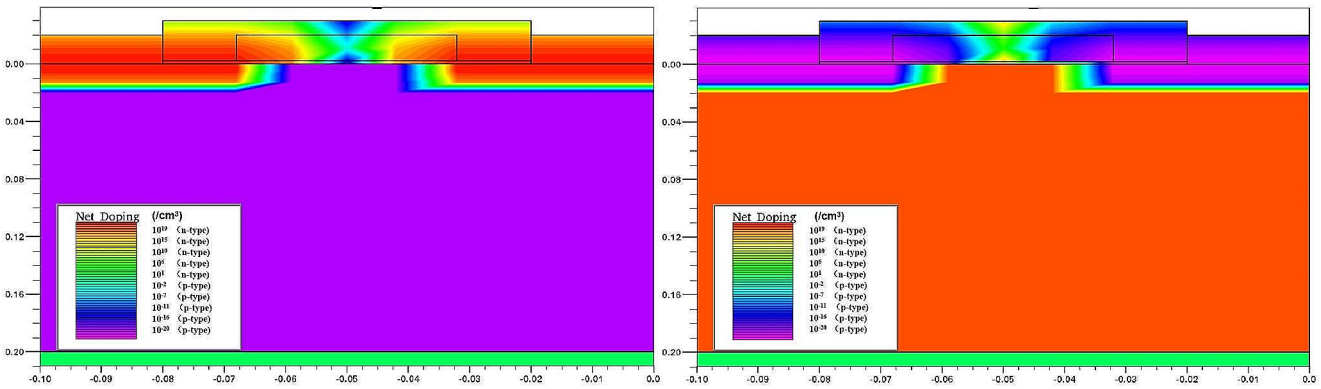

Fig. 1 Structure of the cell. (**a**) NMOS, (**b**) PMOS

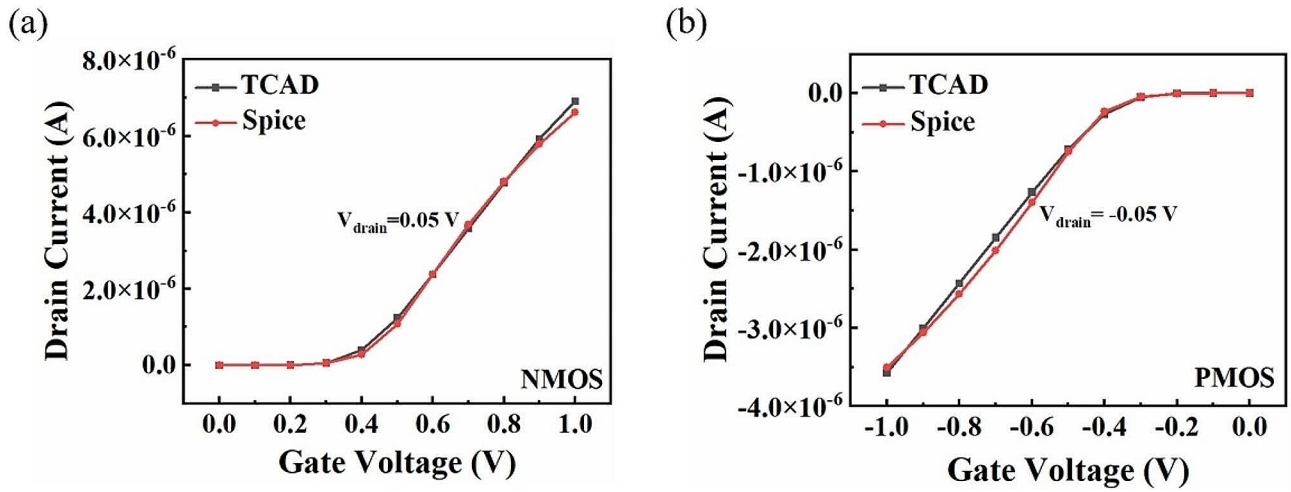

Fig. 2 Transfer characteristic curve of the devices. (**a**) NMOS, (**b**) PMOS

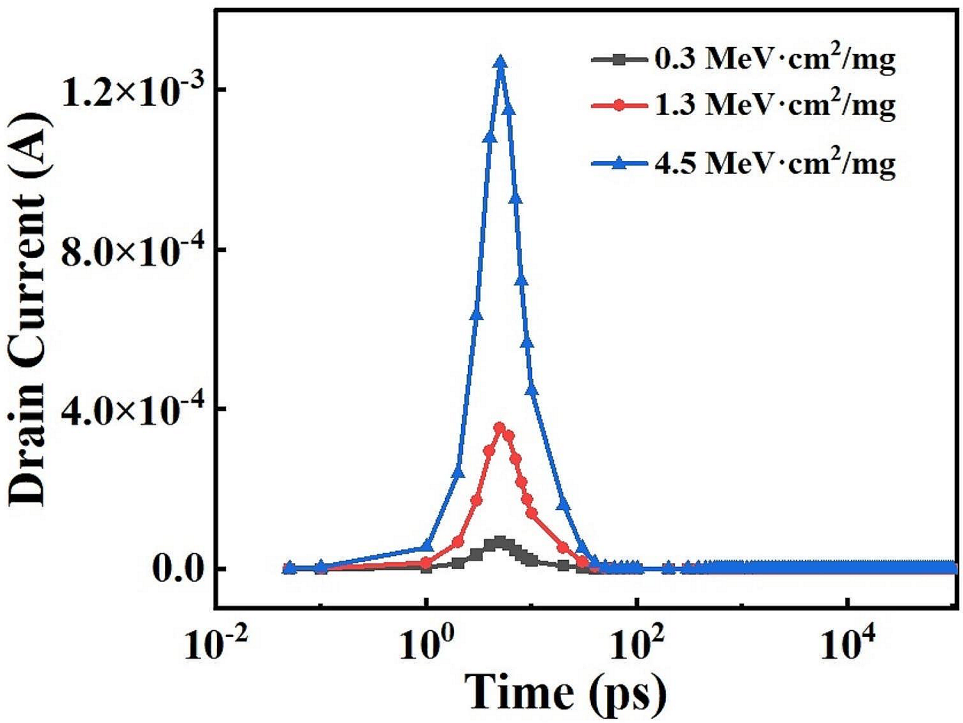

Fig. 3 Curve of the transient drain current

simulation tool HSPICE to construct the equivalent circuit of the FPGA modules. The device under investigation in this study is the Virtex-7 series SRAM-based FPGA, manufactured by Xilinx Company, utilizing 28 nm technology. The Configurable Logic Block (CLB), serving as the fundamental logic unit in SRAM-based FPGA, can be dynamically configured to implement various logic circuits. Each configurable logic block (CLB) element contains a pair of Slices (Slice 0 and Slice 1), as shown in Fig. 4a [18]. Each Slice consists of a 6-input look-up table (LUT), a data selector, a carry chain, and a storage unit. The simplified circuit structure is shown in Fig. 1b. From the diagram, it can be seen that the Slice has two carry chains, each carry chain contains six-input look-up table (LUT), carry look-ahead adder (ADD) and rising-edge D Flip-Flop (FF). Various functions of combinational logic circuits can be accomplished through the combination logic presented by the LUT structure.

Each six-input Look-Up Table (LUT) comprises 64 SRAM storage units and 63 binary data selectors, illustrated in Fig. 5 [19]. Six control bits (Input A-F) are employed to output information from the corresponding SRAM. The outcome of the six-input LUT is then conveyed and utilized as the carry input for the adder, as depicted in Fig. 4. The adder's result is employed as the input signal for the

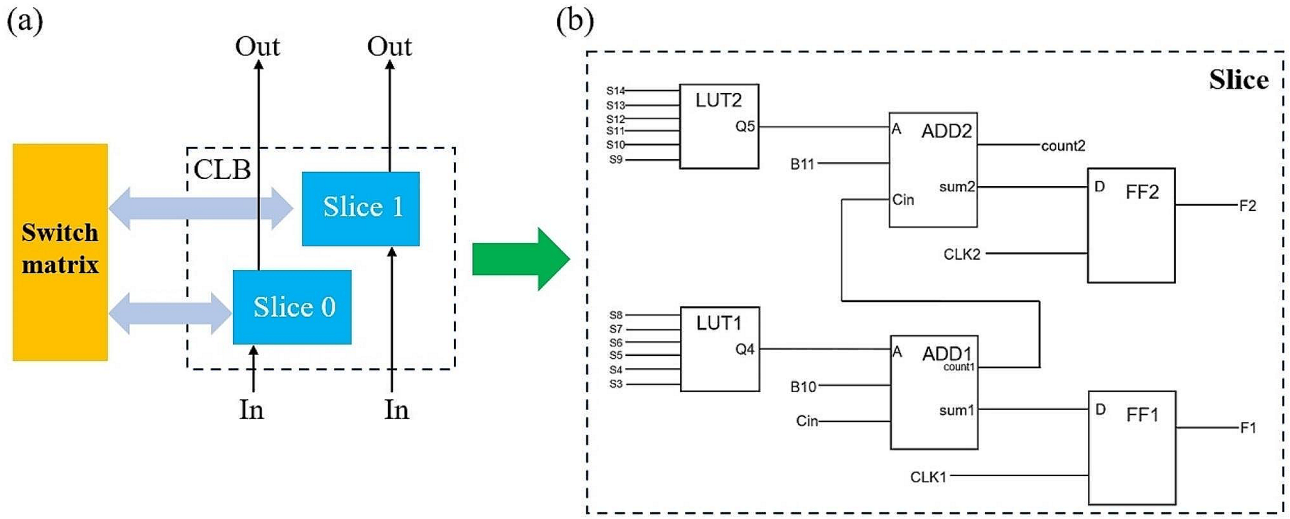

Fig. 4 Diagram structure of the circuit. (**a**) CLB,(**b**) Slice

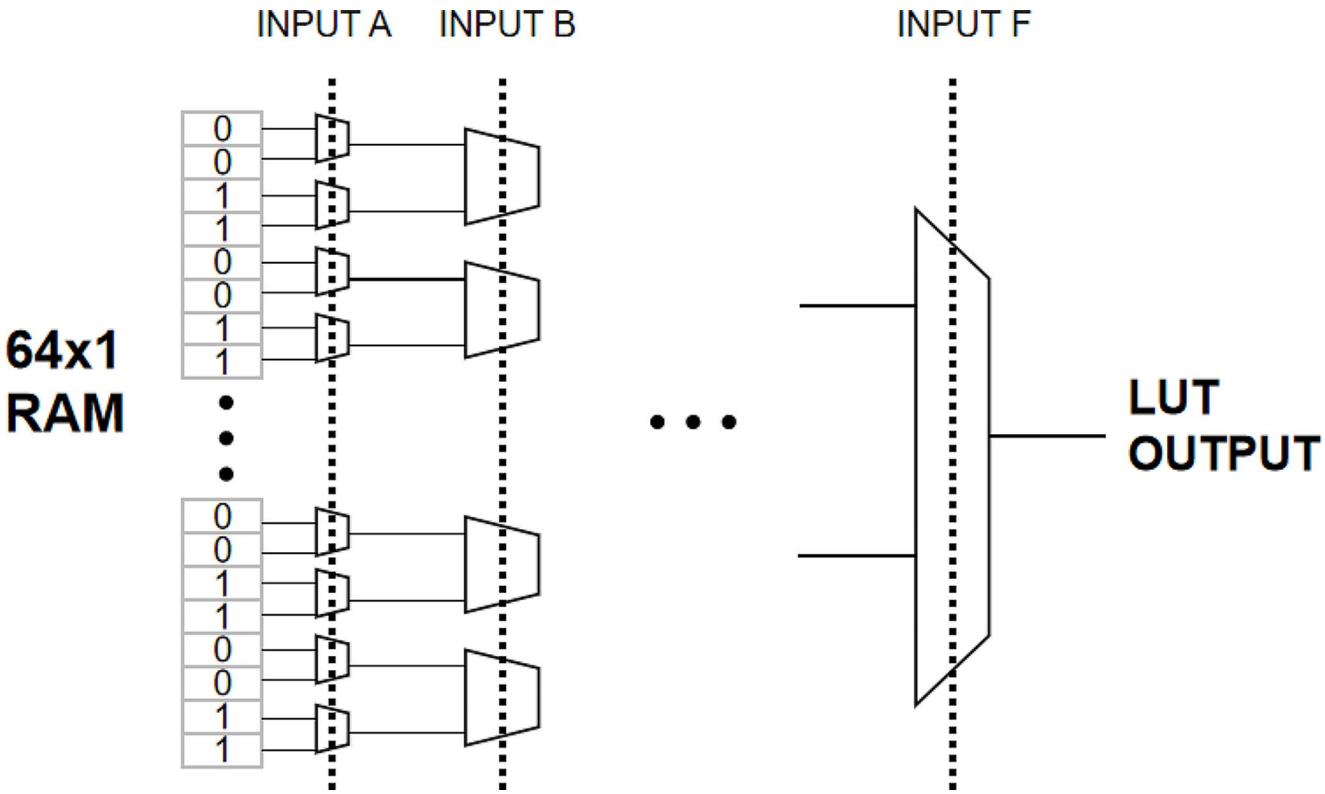

Fig. 5 Structure diagram of six-input LUT

rising-edge D trigger. The clock (CLK) pulse and the output result of the two D triggers operate independently of each other. The electrical model of the core device's Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) in the FPGA was established using TCAD.

2.3 Modeling of Fault Injection

Figure 3 depicts the schematic diagram of fault injection for a 6-cell SRAM structure [20]. For SEE simulation, the sensitive node of the SRAM unit is located in the drain area of the off-state NMOS [21]. Referring to literature [22], we establish a dual-double exponential current source. The

Table 1 Fitting parameters extracted for a single transistor

Item	LET (MeV.cm^2/mg)		
	0.3	1.3	4.5
I_{ps}/mA	0.0676	0.354	1.27
t_{rs}/ps	2.46	2.49	1.77
τ_{1s}/ps	0.72	0.78	1.34
t_{fs}/ps	5.56	5.66	5.73
τ_{2s}/ps	3.74	4.99	4.29

Table 2 Fitting parameters extracted for PMOS restoring current in an inverter

Item	LET (MeV·cm^2/mg)		
	0.3	1.3	4.5
I_{ph}/mA	0.025	0.12	0.34
t_{rh}/ps	2.46	2.49	1.77
τ_{1h}/ps	0.66	0.52	0.36
t_{fh}/hps	5.82	12.63	35.26
τ_{2h}/ps	4.43	9.12	13.45

source can be expressed as $I(t)=I_s(t)+I_h(t)$, where $I_s(t)$ and $I_h(t)$ both have double exponential forms, as shown in Eqs. (1) and (2). In the equations, $I_{p(s\backslash h)}$ represents the peak current; $t_{r(s\backslash h)}$ represents the rising time of the current, and $t_{f(s\backslash h)}$ represents the falling time of the current; $\tau_{1(s\backslash h)}$ and $\tau_{2(s\backslash h)}$ are the rise time constant and fall time constant of the current, respectively.

$$I_s(t)=\begin{cases}0 & 0<t<t_{rs}\\ I_{ps}(1-e^{-\frac{t-t_{rs}}{\tau_{1s}}}) & t_{rs}<t<t_{fs}\\ I_{ps}(e^{-\frac{t-t_{fs}}{\tau_{2s}}}-e^{-\frac{t-t_{rs}}{\tau_{1s}}}) & t>t_{fs}\end{cases} \quad (1)$$

$$I_s(t)=\begin{cases}0 & 0<t<t_{rs}\\ I_{ps}(1-e^{-\frac{t-t_{rs}}{\tau_{1s}}}) & t_{rs}<t<t_{fs}\\ I_{ps}(e^{-\frac{t-t_{fs}}{\tau_{2s}}}-e^{-\frac{t-t_{rs}}{\tau_{1s}}}) & t>t_{fs}\end{cases} \quad (2)$$

$I_s(t)$ mainly characterizes the current collected by the struck transistor during the initial transient non-equilibrium process. That is, based on the established TCAD model of the NMOS transistor, the initial conditions for simulation are set as follows: the particle's impact position is at the center of the drain, and the radius of the particle's trajectory is 0.02 μm. The transient current collected by the drain is recorded, as depicted in Fig. 3 in Sect. 2.1. The main parameters are obtained by fitting the current curve, as shown in Table 1.

$I_h(t)$ mainly characterizes the feedback current from the surrounding circuit due to changes in node voltage. That is, a CMOS inverter is established, where the NMOS adopts the TCAD device model of a single transistor under heavy ion irradiation, and the PMOS adopts a SPICE model, for mixed simulation of devices/circuits. The initial condition is set as Vin = 0 V, and the feedback current of the PMOS is recorded. The main parameters are obtained by fitting, as shown in Table 2.

Considering the presence of power supply and ground in actual circuits, the response of node voltage after particle injection is constrained between V_{DD} and 0 V. Using this constraint, we optimize the peak current values of $I_s(t)$ and $I_h(t)$, continuously iterating and adjusting the peak current I until the voltage drops to 0 V. The values in Tables 1 and 2 are the final optimized parameters obtained through this process.

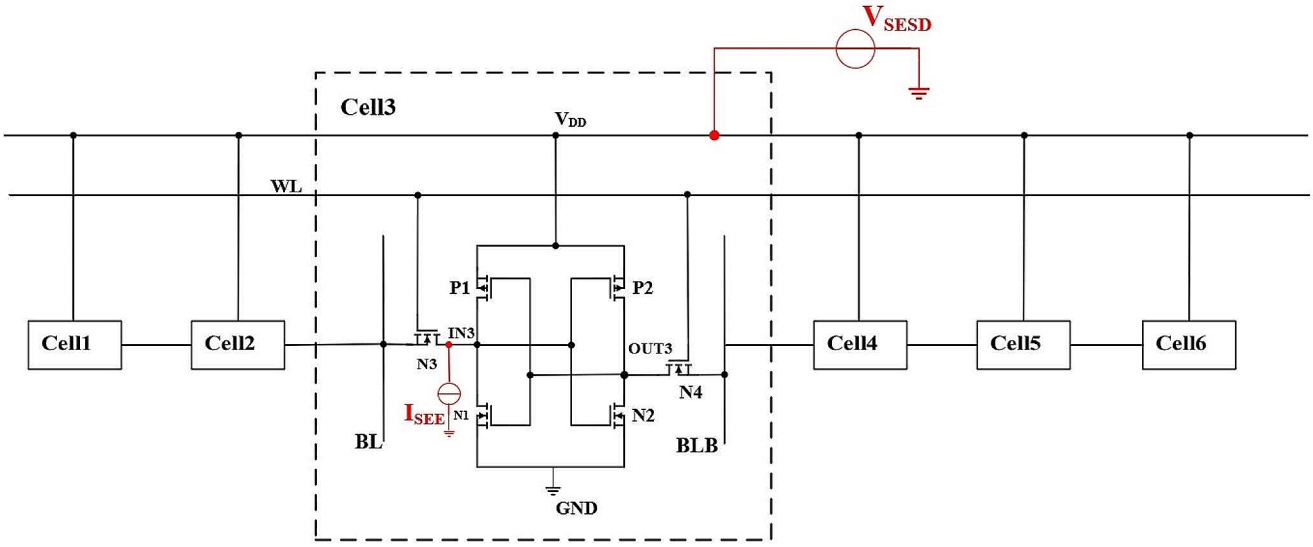

Fig. 6 Fault injection schematic diagram

Upon acquiring all the parameters, the equivalent circuit-level model for SEE simulation is constructed. The results for different linear energy transfer (LET) values are illustrated in Fig. 7(a). It can be observed that at lower LET, the transient current waveform for SEE approximates a double-exponential current source shape. However, as LET increases, the transient waveform exhibits a plateau, followed by a gradual decline.

In previous SESD investigations, researchers identified that this phenomenon predominantly affects the power terminal of the device [23], resulting in transient pulse output similar to SEE [24]. Therefore, we employ the widely used double-exponential function model as the injection form for the voltage source and select typical values [23] as the parameters for this function. The waveforms of injected voltage with varying amplitudes V1 are illustrated in Fig. 7(b).

3 Results and Discussion

3.1 SEE on FPGA Signal Transmission

Building upon the fault injection model described above, we proceed to investigate the impact of SEE and SESD on FPGA signal transmission. We designate SRAM (1,0) as the initial state 1, where node IN = 1 and node OUT = 0; SRAM (0,1) is denoted as the initial state 2, with node IN = 0 and node OUT = 1 (See Fig. 8).

In the event of SEE occurring at the off-state NMOS drain (IN3) of SRAM cell 3, the simulation results are depicted in Fig. 9. If $0 \le \text{LET} \le 1.5$ MeV•cm^2/mg, SRAM cell 3 experiences a single event upset (SEU), while the logic state of other SRAM storage units remains unaffected. The upset in SRAM cell 3 then propagates downward. Notably, the data read by LUT1 and the output signal of LUT1 undergo changes during the reading of the faulty SRAM. This is illustrated in Fig. 9(c), (d), where the output values of triggers D1 and D2 change due to the SEU in SRAM cell 3.

If $1.5 \le \text{LET} \le 5$ MeV•cm^2/mg, SRAM cells 1, 2, and 3 exhibit simultaneous upsets. Moreover, when LET is > 5 MeV·cm^2/mg, SRAM cells 1 to 5 undergo upsetting, as depicted in Fig. 9(b). The number of bits upset varies with different LET values. Lower LET induces single-bit upsets in the SRAM device, whereas higher LET results in the occurrence of Multiple Bit Upsets (MBU), ranging from 3 to 5 bits. The relationship between the number of upsets and LET is shown in Table 3.

In the second device configuration, SEE manifests at the off-state NMOS drain (OUT3) of SRAM cell 3. The simulation outcomes align with the first configuration. For LET values below 1.5 MeV·cm^2/mg, SEU doesn't occur in the SRAM. However, when LET exceeds 5 MeV·cm^2/mg, MBUs emerge, and the number of upset bits correlates with the LET value. In essence, at lower LET, the SRAM encounters exclusively single-bit upsets. Conversely, at higher LET, the SRAM undergoes MBUs, and this behavior remains irrespective of the initial state of the SRAM.

3.2 SESD on FPGA Signal Transmission

When the amplitude (V1) of the SESD-induced voltage pulse follows a double exponential transient pattern with a value of 5 V [23], the simulation outcomes are depicted in Fig. 10. SRAM (1,0) remains unaffected but experiences only a transient pulse. In contrast, a state upset is observed in SRAM (0,1), and all SRAMs with the same initial state in the FPGA, i.e., (0,1), undergo upset. Additionally, the fault of a logic upset in SRAM propagates further downward. Figure 6(c), (d) illustrates the comparison of the output waveform of D triggers D1 and D2.

Furthermore, we observed that the state upset in different initial states is linked to the magnitude of the voltage

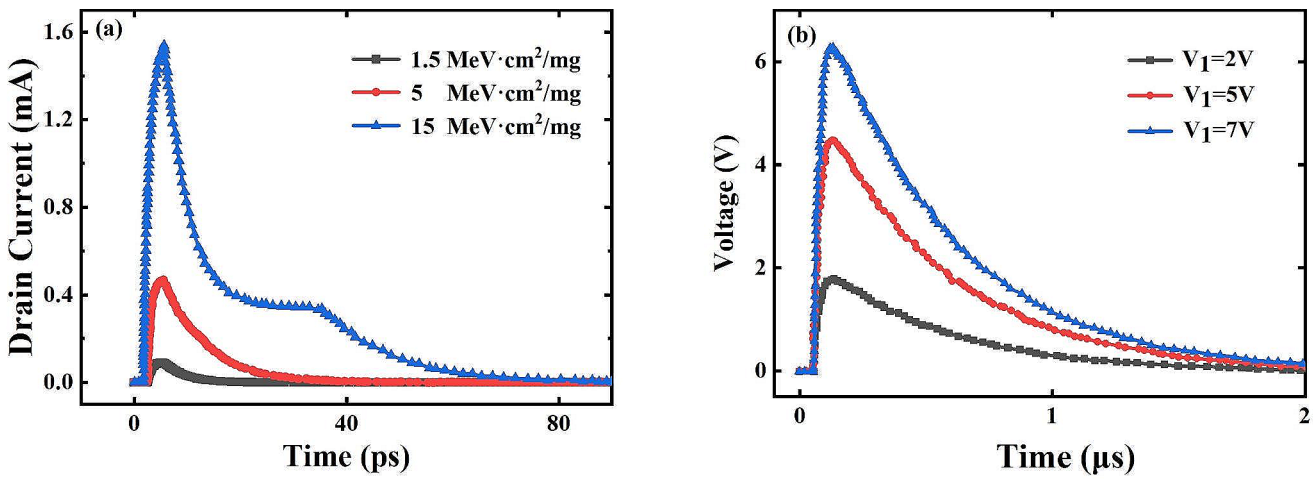

Fig. 7 The waveforms for fault injection. (**a**) transient current used in SEE simulation, (**b**) pulse voltage used in SESD simulation

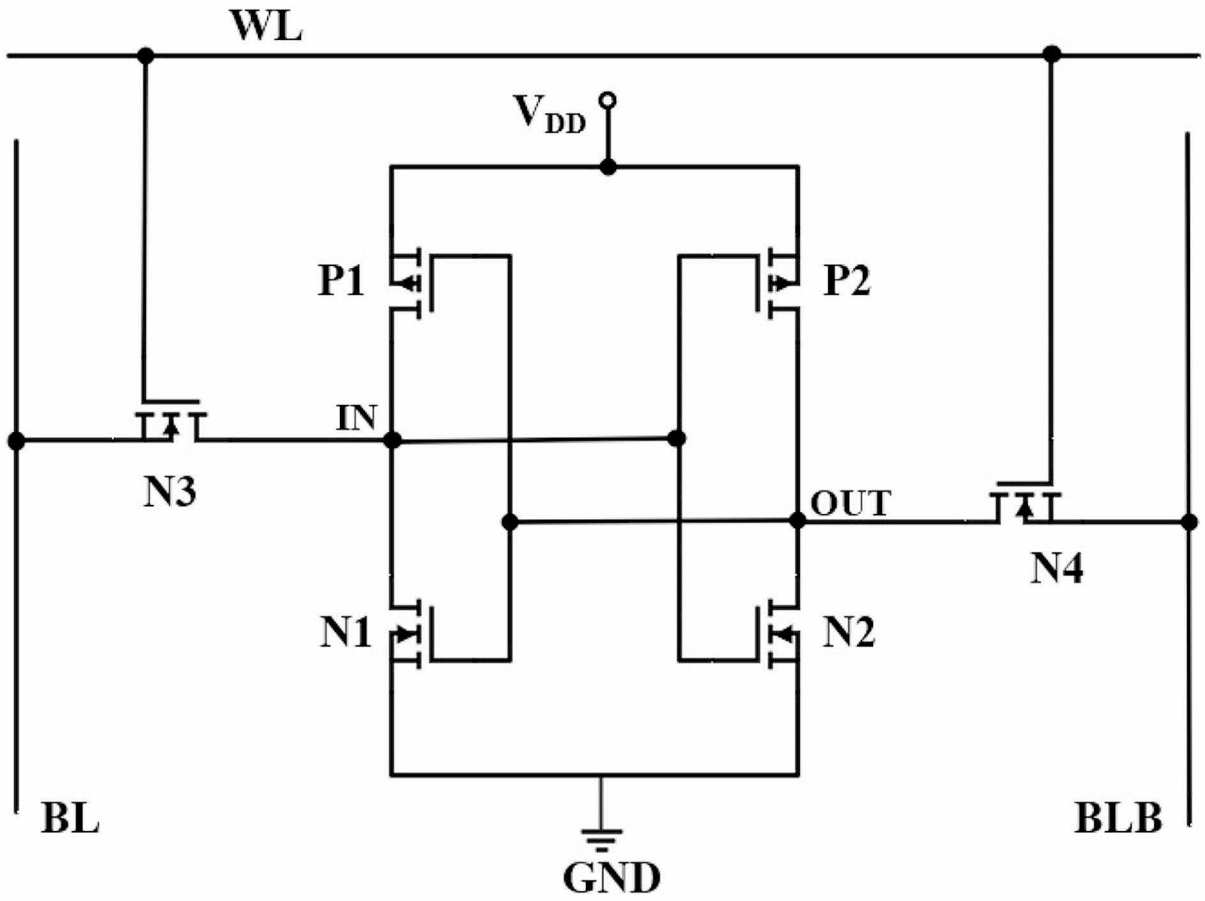

Fig. 8 SRAM storage unit structure

amplitude V1. Subsequent simulations reveal that when the amplitude V1 of the injected SESD transient pulse is ≤ 3 V, SRAMs in both initial states remain unaffected, as depicted in Fig. 11, and only a voltage transient pulse occurs. When the amplitude is between 3 and 7 V, all SRAMs with the initial state of (0,1) remain unaffected; however, SRAMs (1,0) experience a state upset. When the amplitude V1 is ≥ 7 V, all the SRAMs exhibit an upset.

3.3 Comparison of SEE and SESD

Moreover, we investigated the distinctions between state upsets induced by SEE and SESD. Two aspects were considered: the number of upsets and the correlation to the initial state. Initially, SEE can induce single-bit or multi-bit upsets in SRAM, whereas SESD typically causes the upset of multiple bits that share the same storage state.

When SEE is applied to the sensitive position of a single SRAM, the non-equilibrium carrier-electron hole pair collected by the electrode forms a transient current. This current alters the node potential, leading to a reversal of the logic state of the device [25]. At low LET, the generated electron-hole pairs are not collected by the electrodes of different storage cells. In this case, only the SRAM cells directly affected by the fault injection exhibit upsets. However, at high LET, due to charge-sharing effects, the transient currents generated by heavy ion impact are collected by multiple nodes, causing multiple SRAM cells to upset.

While SESD acts on the power supply of SRAM, the induced transient pulse increases the leakage current from the power supply to the ground through the SRAM unit. The significant leakage leads to a substantial decline in the performance of SRAM [24], resulting in a widespread "rail collapse" within a short period. Meanwhile, the bit information of the storage unit with the same initial state becomes unstable. As many bits share the same power supply, the SESD-induced state upset occurs in bits with the same initial state.

Secondly, the logic upset caused by SEE has little correlation with the initial state of SRAM, while the upset induced

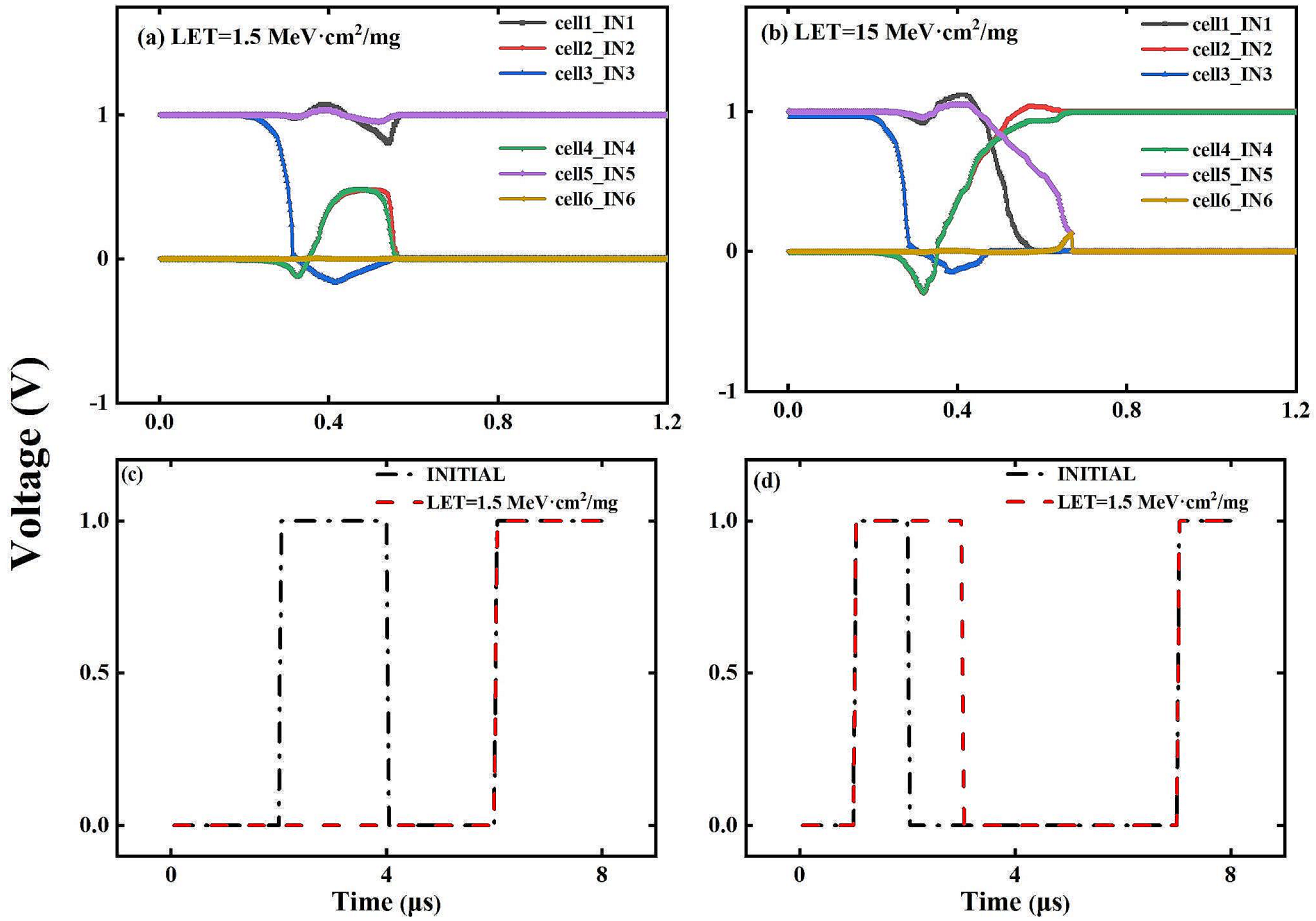

Fig. 9 Comparison of SEE induced waveforms. (**a**) SRAM (1,0) voltage when LET = 1.5 MeV·cm^2/mg, (**b**) SRAM (1,0) voltage when LET = 15 MeV·cm^2/mg, (**c**) Output F1 of D trigger D1 and (**d**) Output F2 of D trigger D2 when SEU occurs

Table 3 SEU situations of a 6-Cell SRAM Structure (impact at the drain of cell 3)

LET (MeV.cm^2/mg)	0-1.5	1.5-5	>5
Upset cells	cell 3	cells 1 to 3	cells 1 to 5

by SESD is related to the initial state. The LET thresholds of SEU in different initial states are both 1.5 MeV·cm^2/mg in the simulated device, indicating the same sensitivity in the initial state. On the contrary, the simulation results of SESD are related to the initial state, as shown in Fig. 11. We further simulated the voltage amplitude thresholds of SESD-induced upset in different initial states and found that they are not equal. For SRAM (1,0), the voltage threshold of SESD-induced logic reversal is about 7 V. For SRAM (0,1), the voltage threshold is about 4.5 V.

To further compare the soft errors induced by SEE and SESD, we conducted an analysis of static noise margin (SNM). Based on the aforementioned findings, we selected specific SRAM back-end circuits for analysis. SNM is a measure commonly used to assess the anti-interference capability of a storage unit. It refers to the amplitude of the maximum DC noise signal that a storage unit can withstand. This value is determined from the "butterfly curve" of voltage transmission characteristics. The side length of the largest square accommodated in the butterfly diagram represents SNM [26]. When SEE affects the sensitive position of a single SRAM, the "butterfly diagram" of SRAM under two initial states is shown in Fig. 12(a). Since the threshold voltage, power supply voltage, and other parameters do not change, the SEU sensitivity of SRAM under two states is the same. Figure 12(b) displays the "butterfly diagram" of SRAM under different injected voltages caused by SESD. It can be observed that a higher power supply voltage will alter the SNM value of SRAM, indicating a slight decrease in its anti-upset ability followed by an increase.

Additionally, we investigated the mechanism of SRAM reversal under the two effects. When SEE impacts the N1 drain (IN) of SRAM (1,0), the resulting transient current lowers the drain potential. For SRAM cells, when the drain potential decreases from a high level to a low level and P1 remains on, the state of the storage unit becomes unstable. Two competing processes occur in the circuit: the recovery

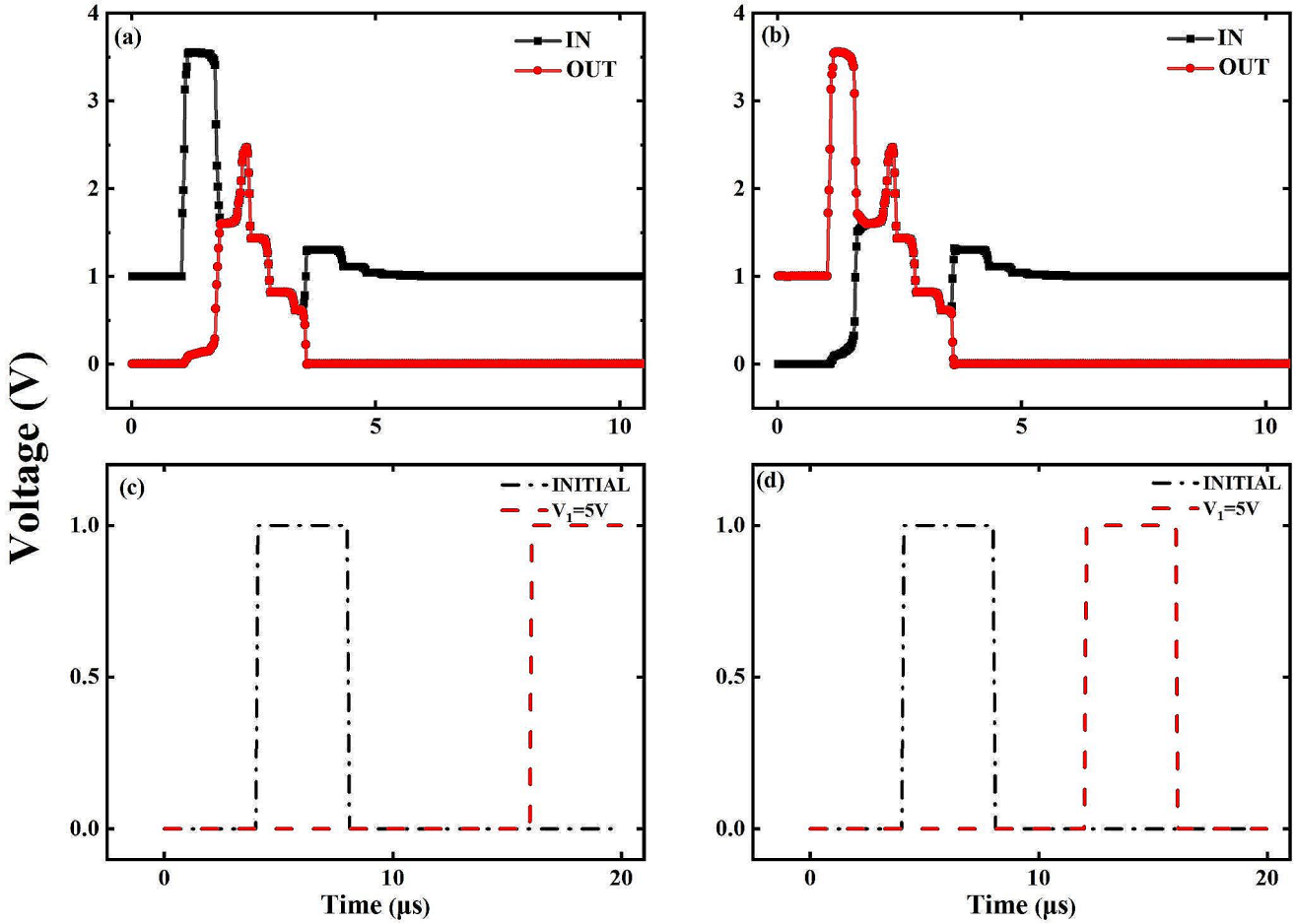

Fig. 10 Comparison of SESD induced waveforms ($V_1 = 5$ V). (**a**) SRAM (1,0) voltage, (**b**) SRAM (0,1) voltage, (**c**) Output F1 of D trigger D1, (**d**) Output F2 of D trigger D2

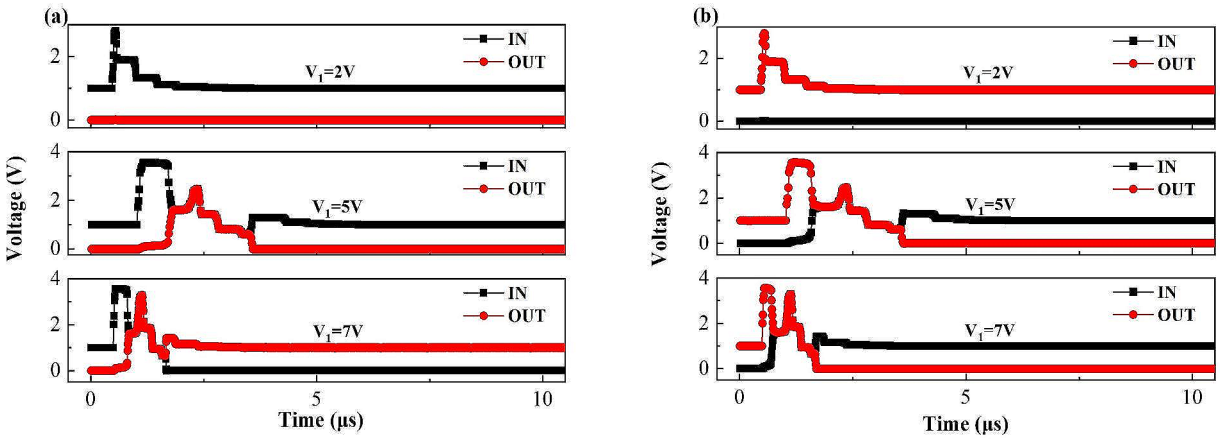

Fig. 11 Comparison of SRAM voltage waveform. (**a**) SRAM (1,0) voltage, (**b**) SRAM (0,1) voltage

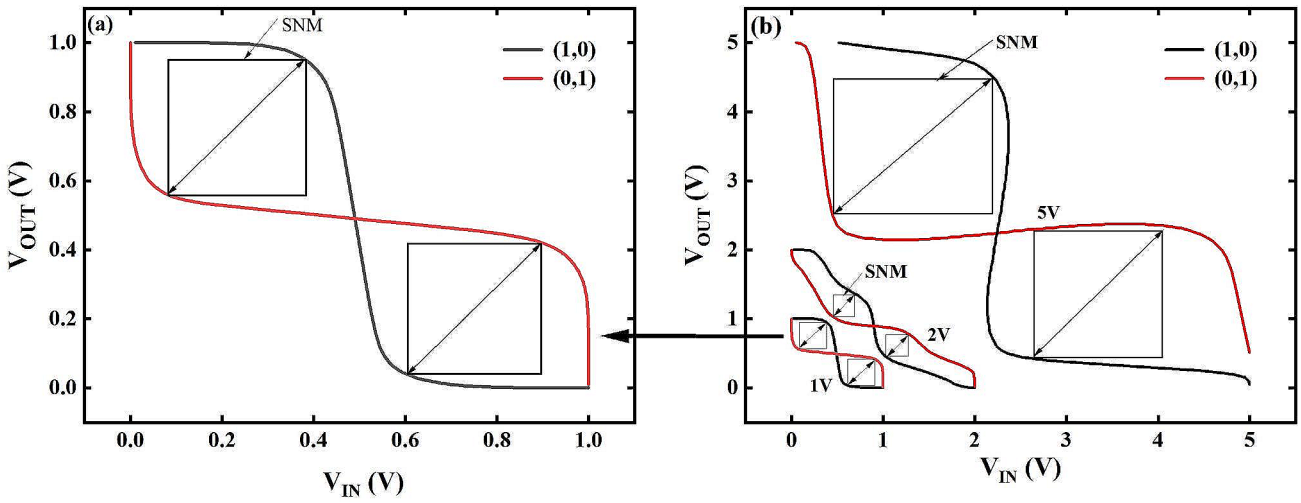

Fig. 12 Butterfly diagram of SRAM. (**a**) Butterfly diagram under SEE, (**b**) butterfly diagram under SESD

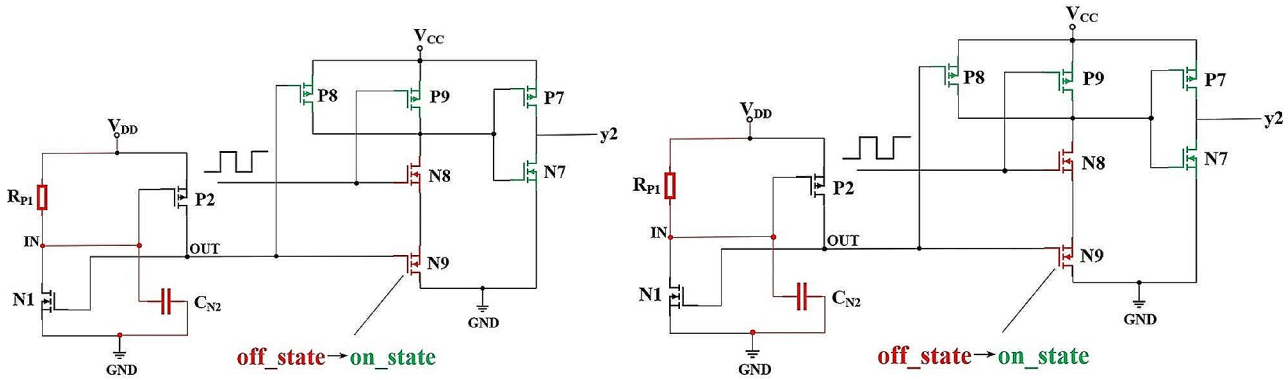

Fig. 13 Equivalent circuit diagram under SEE. (**a**) SRAM (1,0), (**b**) SRAM (0,1)

process and the feedback process. The recovery process involves the power supply V_{DD} charging the capacitor of N2 gate through P1. Subsequently, the drain potential of N1 rises, and the circuit restores to the initial state. This recovery time is denoted as t_r. The feedback process involves the decrease in drain potential of N1, coupled to the gate of N2 and P2, causing N2 to cut off and P2 to turn on. The drain potential of N2 increases and feeds back to the gate of N1 and P1, turning N1 on and P1 off. The larger the difference between feedback time and recovery time (t_f-t_r), the less likely the SRAM will upset [27].

Figure 13(a) illustrates the equivalent circuit diagram for a data selector, serving as a simplified model of the Look-up Table (LUT). The red route represents the equivalent circuit of the recovery process after fault injection in the N1 drain. Concerning the back-end circuit, the N1 drain potential decreases and is coupled to the gate of N2 and P2, resulting in the off-state of N2 and on-state of P2. The drain (OUT) potential of N2 increases, making N9 meet $V_{gs}>0$ and turning the SRAM into the on-state, while P8 still meets $V_{gs}<0$. As depicted in Fig. 13(a), both the back-end circuit N9 and P8 are in the on-state.

When SEE affects the N2 drain (OUT) in SRAM(0,1), the equivalent circuit diagram for SRAM units is shown in Fig. 13(b). At this point, the recovery process involves the power supply V_{DD} charging the gate capacitance of the N1 via the P2, causing the drain potential of the N2 to decrease, thereby restoring the circuit to its initial state. The red route indicates the equivalent circuit of the recovery process after current injection caused by SEE on the N3 drain. Due to the symmetry of the circuit and the same process parameters of the MOS, the difference between the feedback time and the recovery time (tf-tr) is the same in the two states. For the back-end circuit, the generated transient current reduces the drain potential of N2. At this time, P8 meets $Vgs<0$ and changes from off- to on-state, while N9 still meets $Vgs>0$, indicating that both the back-end circuit N9 and P8 are in the on-state.

In conclusion, the equivalent process of the circuit is the same under the two initial states, meaning that the SEU

sensitivity of the SRAM has little correlation with the initial state.

Unlike SEE, SESD induces a transient change in the supply voltage, leading to leakage current through the output node OUT to the back-end circuit. The shunting and absorption in the back-end circuit are related to the initial state of the SRAM unit. For SRAM (1,0), P1 consistently satisfies $V_{gs}<0$. When P1 and N2 are on, P2 and N1 are off. As depicted in Fig. 14(a), the leakage current I_{leak1} is given by $I_{leak1}=I_{gs(P1)}+I_{g(N1)}+I_{d(P2)}+I_{ds(N2)}$. $I_{g(P1)}$ is the pulse transient current flowing through the gate-source capacitor $C_{gs(P1)}$, $I_{g(N1)}$ is the current generated by the circuit charging the N1 gate capacitor, $I_{d(P2)}$ is the current generated by the pulse current flowing through the P2 drain, and $I_{ds(N2)}$ is the N2 source leakage current flowing through the on-resistance $R_{on(P1)}$.

After the superposition of current, the leakage current I_{leak} is depicted in the purple curve in Fig. 14(c). The current flowing into the back-end circuit increases the potential of the output node (OUT). At this point, for the back-end circuit, N9 meets $V_{gs}>0$ and changes from off to on-state, while P8 still meets $V_{gs}<0$. As illustrated in the figure, both N9 and P8 are in the on-state.

For SRAM (0,1), P2 consistently satisfies $V_{gs}<0$. When P2 and N1 are on, and P1 and N2 are off. As illustrated in Fig. 10(b), the leakage current I_{leak2} is defined as follows: $I_{leak2}=I_{g(P1)}+I_{gs(N1)}+I_{ds(P2)}+I_{d(N2)}$. Here, $I_{g(P1)}$ is the current generated by the pulse current flowing through the gate of P1, $I_{gs(N1)}$ is the pulse transient current flowing through the gate-source capacitor $C_{gs(N1)}$, $I_{ds(P2)}$ is the P2 source leakage current flowing through the on-resistance $R_{on(P2)}$, and $I_{d(N2)}$ is the current generated by the pulse current flowing through the drain of N2. After vector superposition of the current, the leakage current I_{leak2} is represented by the purple line in Fig. 14(d). Since I_{leak2} is small and negligible, the potential of the output node (OUT) remains unchanged, and P8 does not satisfy $V_{gs}<0$. Therefore, N9 is in the on-state, and P8 is off.

As evident from the figure, in comparison with SRAM (0,1), SRAM(1,0) generates a larger leakage current. Consequently, the leakage current flowing to the ground through the SRAM unit is smaller for SRAM(1,0). At this juncture, the circuit is less prone to experiencing "rail collapse." In other words, when the SESD voltage amplitude is larger, the logic state of SRAM will reverse. Simultaneously, the operational state of the MOS of the back-end circuit differs in the two initial states. In summary, the simulation results of the SESD are correlated with the initial state.

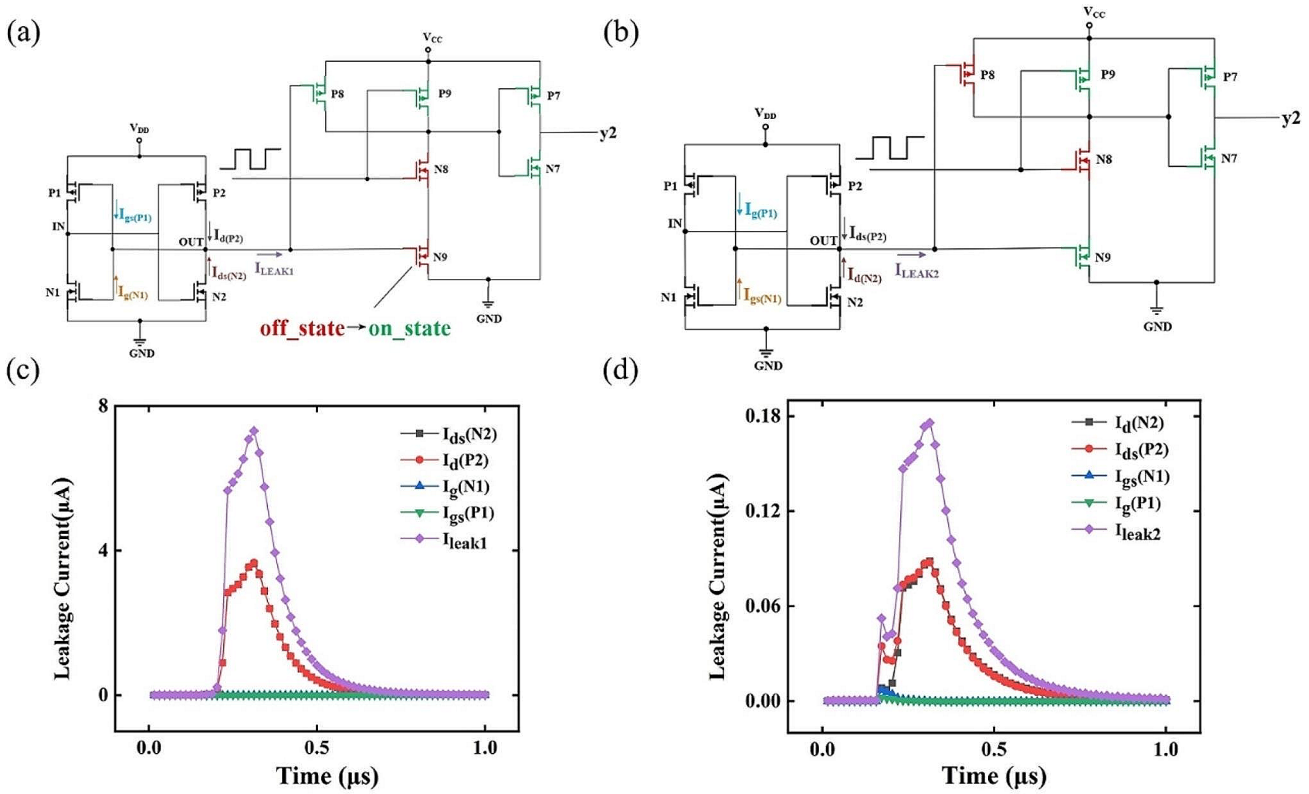

Fig. 14 Equivalent circuit diagram under SESD. (**a**) SRAM(1,0), (**b**) SRAM(0,1), (**c**) Leakage current in SRAM(1,0), (**d**) Leakage current in SRAM(0,1)

4 Conclusion and Further Work

In this study, we delved into the distinctions between SEE and SESD concerning signal transmission in typical FPGA devices. This integrated approach allows for a comprehensive analysis of SEE and SESD at different scales, thereby enhancing our understanding of their propagation and impact throughout the entire circuit. Additionally, it provides a deeper insight and guidance for device design and circuit optimization. Notably, we identified differences in the number of upset bits and their correlation to the initial state. Firstly, SEE can induce Single-Bit Upset (SBU) or Multi-Bit Upset (MBU) in devices, while SESD predominantly leads to MBU. Secondly, the logic upset triggered by SEE exhibits almost no correlation with the initial state of SRAM, whereas SESD-induced upset is intimately connected to the initial state. The threshold voltage amplitude for Single Event Upset (SEU) in SRAM (1,0) surpasses that in SRAM (0,1). This discrepancy is explained by the distinct sensitive regions in SRAM during different effects. SEE introduces two competing processes, namely recovery and feedback, into the circuit, with the time difference between them determining the SEU sensitivity. In contrast, SESD induces leakage current from the power supply to the ground through the SRAM unit, influencing whether the SRAM experiences upset or not. Furthermore, the leakage current resulting from SESD is contingent on the initial state of SRAM, leading to unequal upset thresholds for different initial states.

Additionally, we also have a vision for our future work. We aim to conduct ground experiments involving beam irradiation and an Electrostatic Discharge (ESD) generator to validate our simulation results. It's noteworthy that there is presently no standardized model for the voltage source in the context of SESD. Therefore, we plan to undertake experiments in the future to delve deeper into fault injection and address this gap in understanding.

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Data Availability The datasets used and analyzed during the current study are available from the corresponding author upon reasonable request.

Declarations

Competing Interests The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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