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Radiation Hardened by Design-based Voltage Controlled Oscillator for Low Power Phase Locked Loop Application

Rachana Ahirwar[1] · **Manisha Pattanaik**[1] · **Pankaj Srivastava**[1]

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Abstract
A radiation-hardened-by-design (RHBD) current-starved-ring voltage-controlled oscillator (CSR-VCO) design is proposed based on the separation of gate input technique to mitigate single event effects (SEEs) for phase-locked loop (PLL) implementation. A double-exponential (DE) current model is used to analyze the effect of single event transient (SET) at the output of the proposed RHBD CSR-VCO. The proposed RHBD CSR-VCO is implemented in United Microelectronics Corporation (UMC) 65 nm CMOS technology and a 71.6% improvement is achieved in phase displacement as compared to conventional VCO. The oscillation frequency of 1.75 GHz is obtained for the proposed RHBD CSR-VCO with a tuning range from 0.40 GHz to 2.23 GHz and power dissipation of 1.368 mW. The proposed RHBD CSR-VCO is protected against radiation with deposited charges up to 1050 fC and achieved a higher figure-of-merit (FOM) when compared to the recently reported VCOs and PLLs. This shows that even in a radiation-prone environment, the RHBD PLL can achieve excellent performance and be employed successfully in low-power, high-speed communication applications.

Keywords Radiation hardened by design (RHBD) · Single event transient (SET) · Voltage controlled oscillator (VCO) · Phase displacement · Phase locked loop (PLL)

1 Introduction

Space research delivers us valuable information related to the broadcast, communication, weather forecast, etc. Different types of radioactive processes may occur in the environment. Due to this, the lifetime of a spacecraft (electronic equipment) can reduce and even cause space-mission failure. The phase-locked loop (PLL) is a control system essentially used for frequency synthesis; it is also used in radio, telecommunication, and satellite communications. With continuous scaling of devices, lowered power supply, and higher frequencies, circuits are vulnerable to radiation, such as soft errors or single events effects (SEE) [9]. SEE occurs when radiation particles such as neutrons, protons, or heavy ions strike sensitive nodes of a circuit [7]. This radiation particle passes and interacts with the particular semiconductor device and generates electron–hole pairs (EHPs). The electrons are highly mobile and flow through the device. These electrons generate a current pulse shortly which is in the form of a double exponential function after the interaction of radiation particles. The deep penetration of the charged particles occurs in the device due to voltage glitches generated on the sensitive node. Due to the radiation exposure, charge particles may strike any nodes in a circuit which may cause inaccurate data on the storage node [34, 36, 37]. When a SEE occurs in a storage or memory element and it changes its logic value, this type of effect is known as a single event upset (SEU). The single-event transient (SET) occurs in a combinational circuit while the SEU occurs in a sequential circuit. The main cause of SEE is a current pulse, which has various impacts and outcomes on the circuits. It is a soft error i.e., it disturbs the functional working of a circuit and does not damage the circuit. So, we aim to reduce this soft error rate. There are two basic radiation resistance techniques. The first one is radiation hardened by process

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✉ Rachana Ahirwar
rachana@iiitm.ac.in

Manisha Pattanaik
manishapattnaik@iiitm.ac.in

Pankaj Srivastava
pankajs@iiitm.ac.in

[1] ABV-Indian Institute of Information Technology and Management, Gwalior, Madhya Pradesh 474015, India

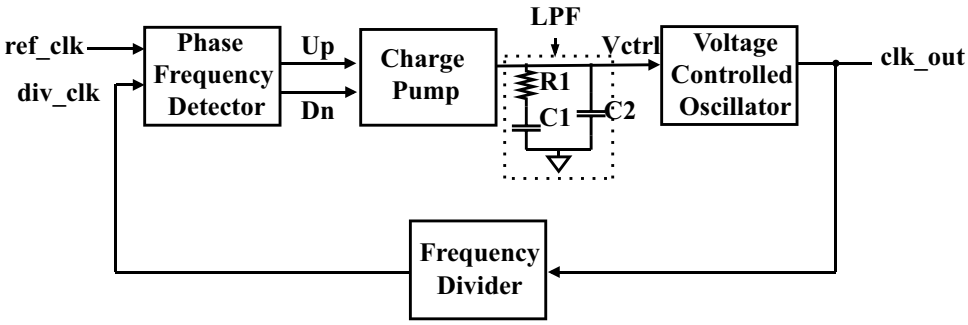


Fig. 1 Block diagram of the conventional PLL

(RHBP) i.e. it is modified the fabrication process so it is very costly and not much preferable due to this property and the second one is radiation hardened by design (RHBD) i.e., it is implemented by different design techniques due to this property it is more attractive than the RHBP technique [10, 13, 21, 26, 33]. So, in this research paper, we have used RHBD based techniques to mitigate SETs. There are different types of RHBD techniques used for device-level, circuit-level, and system-level designs. The Circuit-level techniques such as electrical masking, logical masking, and temporal masking are not very helpful in mitigating SET from the circuits, their effects are decreased with scaling down or increasing the clock frequencies [32].

There are various research works have been reported on radiation hardened by design (RHBD) approaches for PLL. Chen et al. [7] proposed the RHBD-based PLL at 130 nm CMOS technology to improve the performance in the presence of soft error by using voltage-based charge pump instead of the currently based charge pump, this requires additional radiation hardened circuit to achieve high radiation tolerance on voltage-controlled oscillator (VCO) and phase frequency detector (PFD). Chen et al. [6] proposed the radiation-hardened PLL based on a differential cascode voltage switch logic (DCVSL) circuit which consumes more power and area overhead, and it shows high phase noise as compared to the other research. Prinzie et al. [29] and Loveless et al. [23] investigated triple modular redundancy (TMR) based PLL which consists of a triplicate VCO with a major voter circuit for the selection of unaffected data. A large chip area is required to fabricate it. Spatial redundancy techniques consume larger area and high power dissipation while temporal redundancy techniques reduce the performance of the circuit.

Chen et al. [8] proposed the TMR based VCO with a TMR divider (DIV) circuit to achieve high radiation tolerance PLL. When compared to Prinzie et al. [29], the TMR-based approach required a larger area. This approach is used in the digital circuits of a PLL. The design technique is for the radiation-hardened digital circuit. This methodology can only protect the digital area of the PLL from radiation exposure, however, the analog part does not stay protected.

To achieve high radiation tolerance with low area and power dissipation, a circuit-level-based radiation-hardened VCO is proposed to implement radiation-hardened PLL by using the separation of gate input technique. Due to the separation of input for NMOS and PMOS transistors, the circuit area is increased and hence, achieves soft error tolerance.

1.1 The Conventional and the RHBD PLL

The block diagrams of the conventional and the proposed RHBD PLL are shown in Figs. 1 and 2, respectively. It consists of a sequential radiation-hardened phase frequency detector (PFD), a charge pump (CP), a low pass filter (LPF), a frequency divider (FD), and a voltage-controlled oscillator (VCO). When comparing the phase difference (phase error) between the feedback signal (*div_clk*) and the input reference signal (*ref_clk*), the PFD generates a difference signal.

A conventional inverter can experience both positive or negative glitches since the PMOS and the NMOS transistors are both connected to the output node. Hence, this inverter is modified to protect from these types of glitches. The flip-flops and the logic gates of the proposed PLL are implemented in a radiation-hardened manner to protect from radiation particle strikes. A radiation particle strikes a sensitive diffusion region of a MOSFET, which induces glitches in the form of a current that always passes through a p-n junction from the n-type diffusion region to the p-type diffusion region [35]. This states that if a gate is made up of only PMOS (NMOS) transistors then a radiation particle strikes cannot flip the node voltage from $1 \rightarrow 0$ ($0 \rightarrow 1$). It implies that if a particle strikes the diffusion region of an NMOS transistor of an inverter whose

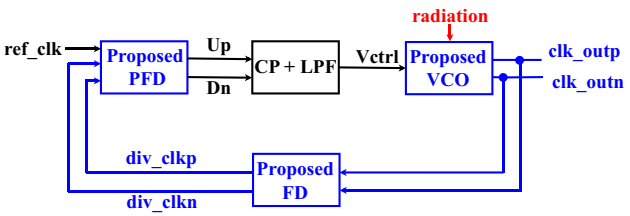


Fig. 2 Block diagram of the proposed RHBD PLL

output is at logic 0, then this particle strike will not cause the output node voltage to flip. Similarly, a particle strikes at the diffusion region of a PMOS transistor of the inverter (with an output node at logic 1) will not result in a SET. This is a key idea to suggest that if a logic circuit is made up of only NMOS (PMOS) transistors, then that logic circuit will be tolerant to node flips from $0 \rightarrow 1$ ($1 \rightarrow 0$). In [22, 35], this method was used to design radiation-hardened SRAM and flip-flop cells, while in [11], it was used to design highly SEU-tolerant standard cell gates. The logic inverter and the flip-flop are used in the proposed PLL design (as shown in Figs. 6 and 10, respectively, are designed using the approach of [11, 20, 22, 35]).

In the proposed RHBD PLL design the inputs of PFD are split in *div_clkp*, *div_clkn*, and (*ref_clk*). The Up and the Dn are the output signals of the PFD which are given as inputs of CP circuits. The outputs of CP are given to the VCO after passing through an LPF. A CP circuit is used to convert the logic states of the PFD which is the phase error (digital signal) into charges (analog signals) required for controlling the VCO. The LPF is used to reject the high-frequency noise (ripples) from the output signal of the CP. The VCO is used to generate oscillating output signals *Clk_outp* and *Clk_outn* are the outputs of the VCO circuit at a frequency determined by the V_{ctrl}. Frequency dividers are commonly used in PLL for generating a frequency that is compared with a reference frequency.

1.2 The Conventional VCO

The VCOs can be based on a ring oscillator or inductor-capacitor (LC) oscillator. The ring oscillator is most popular among LC oscillators due to its wide tuning range and low complexity. The ring oscillator has its limitations such as high phase noise, low operating frequency, and low-quality factor value as compared to the LC oscillator [31]. However, the modern world demands are low power consumption, less complexity, and wide tuning range-based PLL. Moreover, LC-oscillator based PLL is more sensitive to total ionizing dose (TID) and SEU as compared to ring oscillator based PLL [16]. Hence, the ring oscillator based VCO is the best choice for radiation-hardened PLL design. The schematic representation of the conventional current starved ring (CSR) VCO as shown in Fig. 3, consists of an inverter with additional PMOS and NMOS transistors which is connected as bias i.e., the node voltage Vp is connected to input of PMOS bias transistors (MPbias) and the node voltage Vn is connected to input of NMOS bias transistors (MNbias). These excess PMOS and NMOS transistors can reject the excessive drain leakage current from the circuit [25].

The oscillation frequency [2] is calculated as:

$$f_{osc} = \frac{I_d}{N.V_{dd}.C_{total}} \tag{1}$$

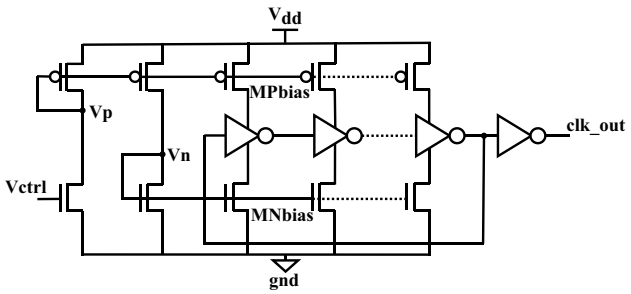


Fig. 3 Schematic view of the conventional CSR-VCO

where f_{osc} is the oscillation frequency of PLL, N is the number of VCO inverter stages, I_d is the drain current when VCO input voltage (V_{ctrl}) is $V_{dd}/2$, V_{dd} is the supply voltage and C_{total} is the total capacitance of single stage of VCO. The following equation is used to calculate the total capacitance

$$C_{total} = \frac{5C_{ox}(W_pL_p + W_nL_n)}{2} \tag{2}$$

where C_{ox} is the capacitance of CMOS, W_p (W_n) and L_p (L_n) are the width and length of PMOS (NMOS), respectively. The oxide capacitance C_{ox} is calculated as

$$C_{ox} = \frac{\epsilon_0\epsilon_r}{t_{ox}} \tag{3}$$

where, ϵ_0 and ϵ_r are the absolute permittivity and the relative permittivity of the SiO_2, respectively, t_{ox} is the oxide thickness of NMOS and PMOS defined by technology library. This oscillator has a high tuning range with low power consumption due to the low leakage current. However, the VCO cannot provide the desired output frequency for a long period defined as a phase displacement in the presence of radiation. A modified VCO circuit is proposed in the subsequent section to improve the radiation tolerance of current-starved VCO in the radiation-harsh environment.

The organization of this paper has been done as follows. Section 2 includes the architecture and working operation of the proposed RHBD-VCO for PLL. Section 3 consists of different experimental analysis of the proposed RHBD VCO and the conclusion is summarized in Section 4.

2 The Radiation Hardened by Design (RHBD) Based Phase Locked Loop (PLL)

2.1 The Proposed Radiation-Hardened VCO

The VCO is the most sensitive block in PLL. The schematic representation of the radiation-hardened CSR-VCO is shown in Fig. 4. It includes an input-biased stage and

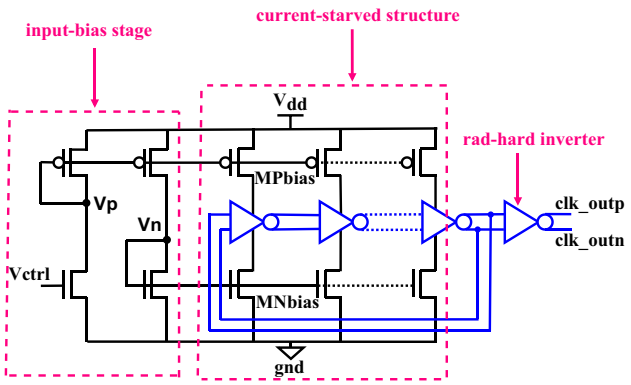


Fig. 4 The proposed radiation-hardened CSR-VCO

a current-starved structure which offers a good balance between area, power, and phase noise with a wide tuning range. This CSR-VCO design is based on the separating gate input RHBD technique. This RHBD technique ensures that the gate inputs are isolated from each other, thereby reducing the impact of radiation on the VCO's performance. This separation helps in achieving a stable and reliable output frequency even in the presence of radiation.

Additionally, the current-starved structure further enhances the VCO's resilience to radiation by providing a consistent and controlled current flow throughout its operation. The RHBD CSR-VCO layout is shown in Fig. 5. The RHBD CSR-VCO has an area of $322.123\mu m^2$ (11.65 μm X 27.65 μm) which is smaller as compared with the recently reported radiation-hardened VCO [14], which has an area of $8400\mu m^2$.

2.1.1 The Proposed Radiation-Hardened Ring Inverter

The schematic and the symbolic representation of the proposed radiation-hardened ring inverter are shown in Fig. 6. The proposed radiation-hardened ring inverter used additional PMOS and NMOS transistors as compared to the conventional inverter design. If the input or the output node voltage of a conventional inverter is flipped due to radiation particles the ring-VCO circuit output (*clk_out*) is altered. Hence, there is a requirement for additional input and output nodes to protect against radiation particles hit. Both inputs (inp and inn) are at the same node voltage and both outputs (outp and outn) are also at the same node voltage of the proposed ring-inverter (in Fig. 6). This inverter refers to a ring inverter because it is connected by two inverters i.e. both inverter is made up of four transistors. The first inverter has three PMOS (M1, M2, M3) and one NMOS (M5) transistor. Similarly, another inverter has three NMOS (M6, M7, M8) and one PMOS (M4) transistor. The M3 and M6 transistors are selected to be low-threshold voltage transistors. Due to this, the voltage swing is increased at output nodes (outp and outn) and these nodes are becoming closer to the rail voltages. When the voltage swings at nodes outp and outn are reduced, the leakage currents are not increased in a similar inverter in its fanout. This is because, when the node outp is at $|V_{M3T}|$ ($|V_{M3T}|$ is the threshold voltage of M3 transistor) then the node outn is at gnd due to this the NMOS transistor of the fanout inverter is completely turned OFF while its PMOS transistor is turned ON. A similar argument holds for the case when the node outp is at V_{dd} and the node outn is at $V_{dd} - V_{M6T}$ ($|V_{M6T}|$ is the threshold voltage of M6 transistor). Therefore, the leakage currents in a fanout inverter do not increase due to non-rail voltage swings at its inputs.

The current-starved inverters are used in the proposed RHBD VCO to reduce leakage current. A radiation-hardened ring-inverter is designed by separating the inputs for both NMOS and PMOS (in = inp for PMOS, in = inn for NMOS) transistors. The NMOS transistors will avoid the data flipping from logic 0 to logic 1 and the PMOS transistors will avoid the data flipping from logic 1 to logic 0. In the proposed radiation-hardened inverter (Fig. 6), outp and outn nodes are the most sensitive nodes

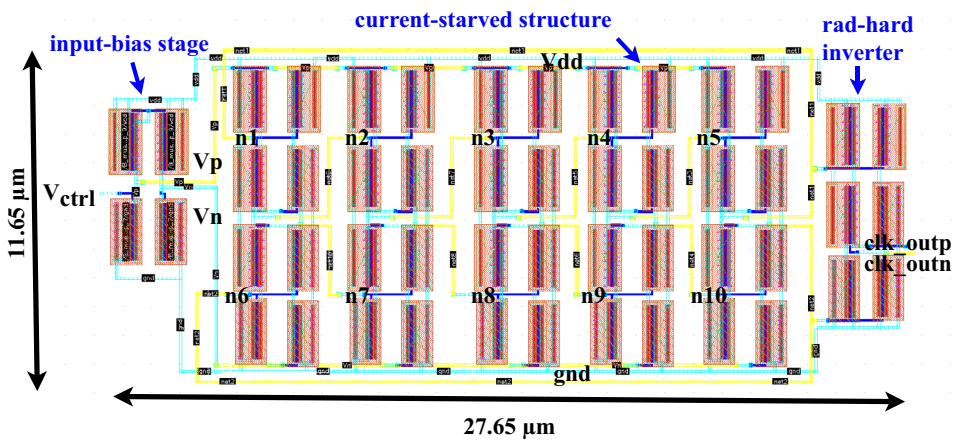


Fig. 5 Layout of the proposed radiation-hardened five-stage CSR-VCO

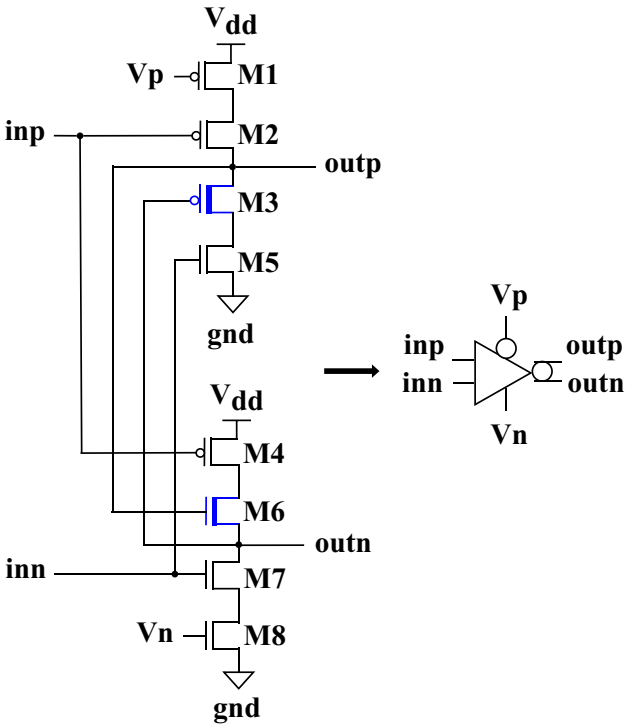


Fig. 6 The proposed radiation-hardened ring inverter

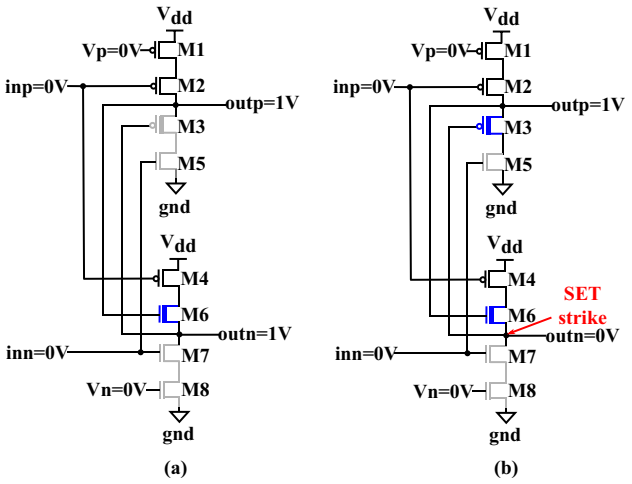


Fig. 7 Radiation-hardened ring inverter **a** before the SET strike, and **b** after the SET strike

in a radiation-based environment. Consider a case for the radiation-hardened proposed ring inverter if input values (inp and inn) of both PMOS (M2 and M4) and NMOS (M5 and M7) transistors are at logic value 0 and the inputs (Vp and Vn) of biasing transistors (M1 and M8) is at a logic value of 0, the output nodes outp and outn will have at a logic value of 1 as shown in Fig. 7(a). If there is a flip of the logic value of 1 to a logic value of 0 due to SET at the sensitive output node outn, this output node outn will change the input node voltage of the M3 PMOS transistor but it will not affect the output node outp as shown in Fig. 7(b). However, the node outp will remain at its original true logic value of 1, and with the help of M5 and M6 NMOS transistors, the node outn again gets its true logic value of 1.

Similarly, for the given case if there is a 1 to 0 logic value flipping at the node outp, the node outn will help the node outp to recover the true logic value.

2.2 RHBD Based Frequency Divider

The VCO generates high frequency. Therefore, the frequency divider (FD) circuit as shown in Fig. 8, is used to reduce the frequency of clock signals (*Clk_outp* and *Clk_outn*) generated from the VCO. Here a frequency divide-by-32 circuit is used to match the outputs of FD *div_clkp* and *div_clkn* with (*ref_clk*) signal. The circuit consists of radiation radiation-hardened D flip-flop (FF_1 - FF_n) with a combination of radiation-hardened based XOR and AND gates. The schematic of the RHBD based NAND gate is shown in Fig. 9. The schematic of the RHBD D flip-flop as shown in Fig. 10 is based on splitting the gate inputs approach for PMOS and NMOS transistors to protect from radiation particle strike. The separate *Clk_outp* and *Clk_outn* are the outputs of the VCO. The Dp and Dn

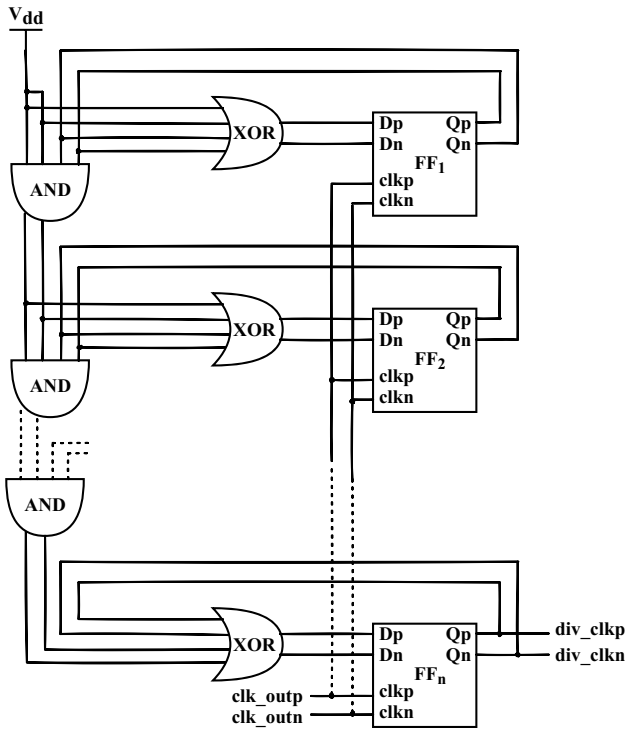


Fig. 8 RHBD based frequency divider

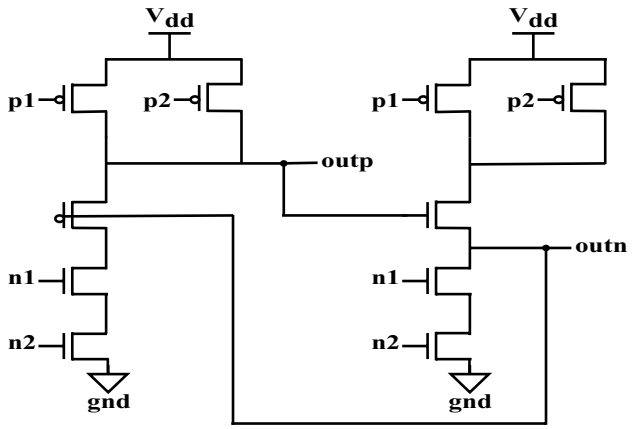


Fig. 9 RHBD based NAND gate

are used as input of PMOS and NMOS transistors, respectively. The Qp and the Qn are outputs of the D flip-flop.

2.3 The RHBD Based Phase Frequency Detector

The phase frequency detector (PFD) is used to compare the difference between *div_clkp*, *div_clkn*, and the reference clock (*ref_clk*). The three states of a NAND PFD circuit are the Up, the Down, and the reset [20]. The working of the NAND PFD must be appropriate when the reference signal is delayed or the feedback signal is delayed [1]. The block diagram of the RHBD PFD is shown in Fig. 11.

2.4 The RHBD Based Charge Pump

The charge pump (CP) design is based on a radiation-hardened technique. It is the second most sensitive area than VCO in PLL. The input UP (DN) signal of CP is at high logic when the reference clock signal (*ref_clk*) leads (lags) with divider clock outputs (*div_clkp* or *div_clkn*). Hence the CP generates a positive (negative) polarity current at its output and this current passes through the filter as shown in Fig. 12. Here the filter is based on a low-pass filter which filters high-frequency noise and converts current into voltage. The LPF has a resistor R1 and two capacitors (C1 and C2). These values are obtained at 994 ohm, 721 pF, and 56 pF, respectively [20]. This voltage is an input of VCO (V_{ctrl}). Due to the prior of UP signal as compared to the DN signal, the V_{ctrl} voltage value is increased. Conversely, when the DN signal is at the prior state, the V_{ctrl} voltage value is reduced.

3 Experimental Analysis of PLL

This section includes the DC as well as the RF analysis of PLL. The proposed RHBD PLL is bench-marked with respect to conventional and reported PLL. The simulation results are conducted on the United Microelectronics Corporation (UMC) 65 nm CMOS commercial standard process in the CADENCE Virtuoso tool.

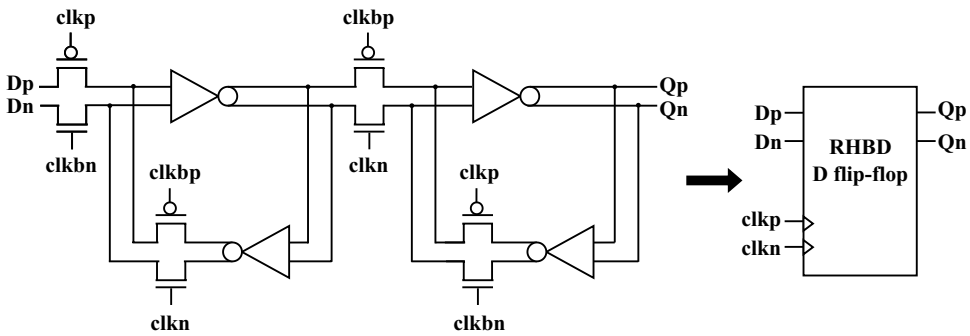
3.1 Transient Current Modeling

Due to the strike of radiation at sensitive nodes (or at the drain side of PMOS and NMOS), a large amount of current flow in the circuit affects the circuit output value. Due to it, a transient current pulse is generated which is in the form of a double exponential (DE) function. This transient current has a rapid rise and gradual fall time. The equation for DE current pulse [3], I(t), in SPICE is defined as

$$I(t) = \begin{cases} 0 & ;t < t_{d_r} \\ I_{peak}(1 - e^{\frac{-(t-t_{d_r})}{\tau_r}}) & ;t_{d_r} < t < t_{d_f} \\ I_{peak}(e^{\frac{-(t-t_{d_f})}{\tau_f}} - e^{\frac{-(t-t_{d_r})}{\tau_r}}) & ;t > t_{d_f} \end{cases} \quad (4)$$

where, τ_r is the rise time constant, τ_f is the fall time constant, t_{d_r} is the rise delay time, t_{d_f} is the fall delay time and I_{peak} is the peak current value. The total charge, Q_t delivered by the current pulse which is integral over time of the double exponential current pulse, I(t) [17, 18].

Fig. 10 RHBD based D flip-flop



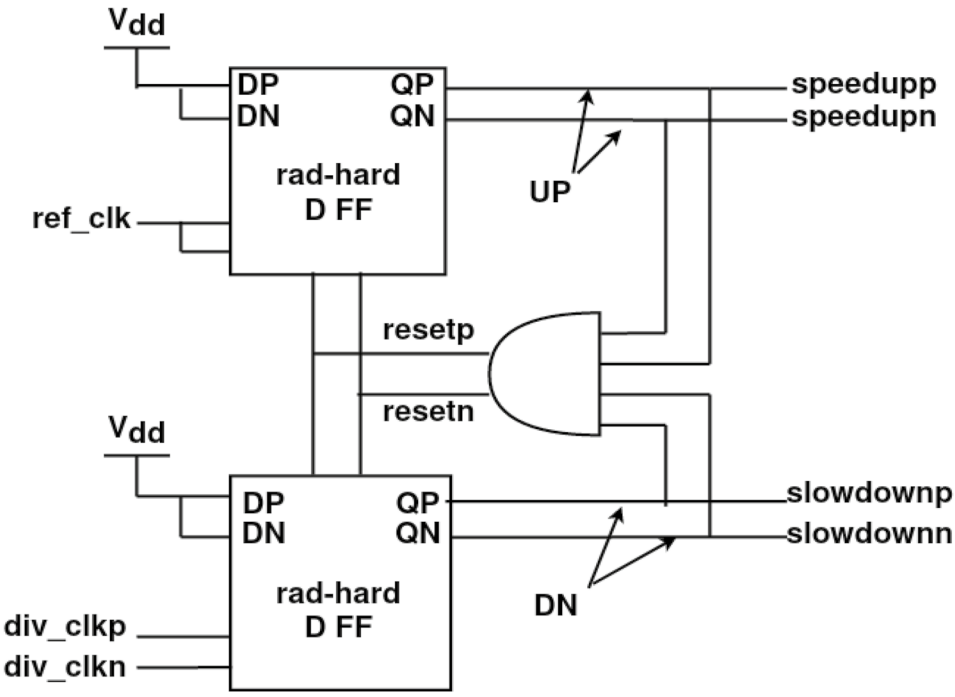


Fig. 11 Block diagram of phase frequency detector

$$Q_t = I_{peak}[\tau_r + \tau_f + (t_{d_f} - t_{d_r}) - \tau_r e^{\frac{-(t_{d_f} - t_{d_r})}{\tau_r}}] \quad (5)$$

If the difference between the fall delay time and rise delay time (t_{d_f} - t_{d_r}) is higher than τ_r, then the last term of Q_t is neglected and the calculation of the total charge is simplified.

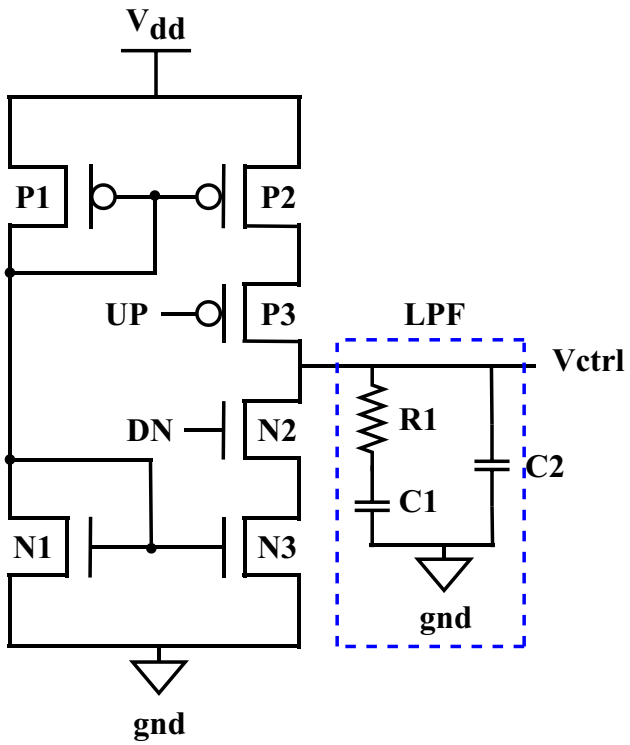


Fig. 12 Charge pump with low pass filter

According to the reported research [20, 39] τ_r and τ_f values are 38 ps and 150 ps, respectively for a 65 nm CMOS technology. We use these values for all radiation-hardened-based calculations. The fitting parameters for DE current source are shown in Table 1. This DE current model is used for injecting SET current on the sensitive node (drain of PMOS / NMOS) of the proposed VCO. Some values are constant for it. Figure 13 shows equivalent circuits for generating a positive and a negative transient pulse. When the size of the NMOS transistor increases which dissipates the deposit charge value, the magnitude and duration of the SET pulse diminish rapidly [39]. It is found that when technology scales down, the probability of longer SET pulses increases for combinational logic [28].

3.1.1 SET Effects on Frequency and Phase Noise

In this research work, we have used the DE current model equation 4 to inject SET current at the sensitive node of the proposed RHBD CSR-VCO. After that, we calculated the total deposit charge by using equation 5. The effect of SET on frequency and phase noise (referred to as PN in dB_c/Hz at offset frequency 1 MHz) is shown in Table 2. It is found that when the total deposit charge value (in fC) of a node is increased, the oscillation frequency is decreased and phase noise is increased of the proposed VCO.

By using the parameters values of the DE current model for introducing SET at a sensitive node of the proposed

Table 1 Fitting parameters of transient current for the drain of PMOS and NMOS transistors

Constant values	Variables			
τ_r = 38 ps and	(t_{d_f} - t_{d_r}) (ns)	5	10	15
τ_f = 150 ps [20, 39]	Q_t (nC)	0.536	0.8	1.2

VCO, we have found that our proposed RHBD CSR-VCO is SET tolerated upto 1050 fC i.e. when the total charge value at the node is greater than 1050 fC its oscillation frequency waveform is affected at particular time duration at which time SET current pulse is injected. This proposed VCO design is more radiation tolerated as compared to reported research work [20, 24].

3.2 SET Quantification

The most sensitive area of PLL for SETs is VCO [12]. The VCO is used for the generation of oscillating frequency. To analyze the radiation exposure on the VCO a current pulse of different peak values is injected on the most sensitive node at different time intervals such as 5ns, 10ns, and 15ns. As a result, a high current pulse is found at a node which causes the short-term failure in oscillation as shown in Fig. 14. This mechanism for calculation of single event upset can be quantified by calculating the displacement of output phase ϕ_{disp} which is known as phase displacement (in radians) [23]. ϕ_{disp} is calculated as given in equation 6

$$\phi_{disp} = \frac{2\pi|T_{set} - T_{clk}|}{T_{clk}} \tag{6}$$

where, ϕ_{disp} is the phase displacement in radians, T_{set} is the perturbation period of the clock, and T_{clk} is the period of the nominal clock.

The effect of phase displacement due to the current pulse is illustrated in Fig. 15 on hardened and conventional VCO.

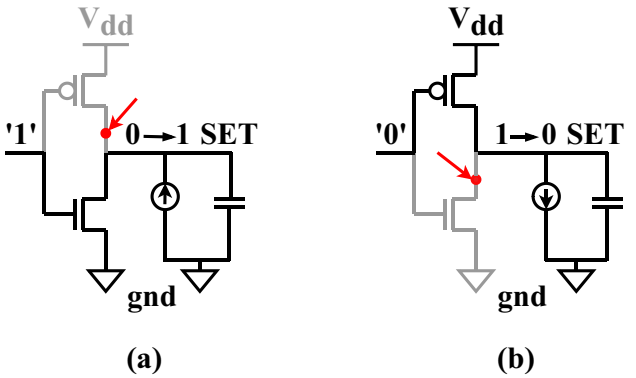


Fig. 13 Equivalent circuits for generating **a** a positive transient pulse, and **b** a negative transient pulse

Table 2 Effect on frequency and phase noise with variation in SET current values

I_{peak} (μA)	100	150	200	250	300
Q_t (fC)	500.14	750.2	1000	1250	1500
f_{osc} (GHz)	1.753	1.745	1.731	1.705	1.671
PN (dB_c/Hz)	−91.92	−91.18	−88.89	−77.35	−72.98

PN- Phase Noise @ 1 MHz

The different values of delivered charge particles Q_t (0.536 nC, 0.800 nC, and 1.20 nC) are obtained by inserting the different peak values of DE current pulse. It is found that when the charge particle value increases corresponding to the increase of input voltage its phase displacement value also increases. The immense value of phase displacement is found for conventional VCO as compared to the proposed RHBD CSR-VCO. The proposed RHBD CSR-VCO shows a 71.6% improvement as compared to conventional CSR-VCO. Therefore, the proposed radiation-hardened CSR-VCO works in a radiation harsh environment and it can be used for radiation-hardened PLL applications.

3.3 Transient Analysis of the Proposed VCO

When a high set current I_t value is injected at the sensitive nodes such as node n2 of the proposed VCO its node voltage changes from logic 0 to logic 1 or vice-versa as shown in Fig. 14. Due to the high deposit total charge at the sensitive node, the proposed VCO's outputs are also affected at that duration of injected current. It is found that the recovery time of sensitive node voltage is decreased with the low injected current pulse value [19].

The deposit charge is swept away by the drive current I_d of the ON state transistors and the sweeping time increases

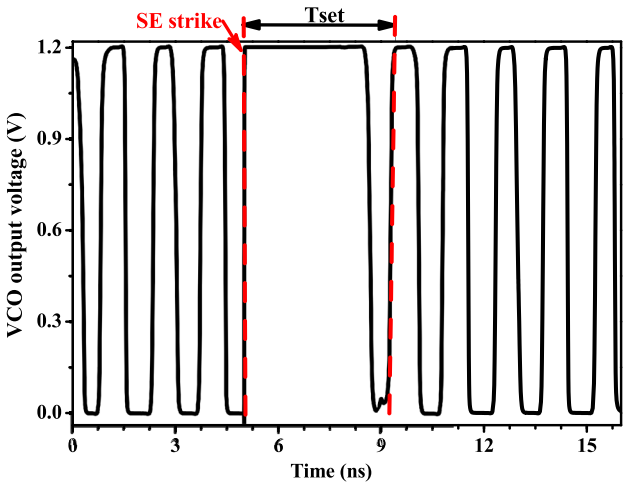


Fig. 14 T_{set} calculation for phase displacement

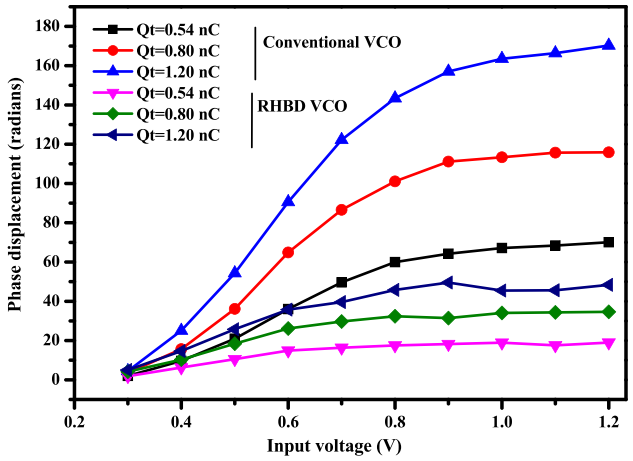


Fig. 15 Phase displacement (radians) versus input voltage (volts) for proposed and conventional five-stage VCO at different Q_t values

with the amount of the deposit charge. Additionally, for the node outp (or node Vn), the recovery time is smaller than the node outn (or node Vp). This is due to the drive current I_d of the PMOS transistor is smaller than the NMOS transistor. The proposed VCO is SET tolerated upto 1050 fC of deposit total charge Q_t at the sensitive node. The simulation results verified that it is superior to the SET resistance of a single node. The high value of injected current is induced transiently in the output of the proposed VCO by hitting a single node.

3.4 VCO Frequency Transfer Characteristics

The graph of Fig. 16 shows the oscillation frequency at the different VCO's input voltage (V_{ctrl}) for the conventional and proposed VCO. The result represents the center frequency of the proposed RHBD CSR-VCO (i.e. the frequency at which $V_{ctrl} = V_{dd}/2$) is approximately 1.34 GHz. It is found that oscillation frequency is increased, respectively with supply voltage and control voltage increment. The oscillation frequency was within 10% of $(f_{max} + f_{min})/2$ to ensure the proper balance between gain, jitter, and stability [5].

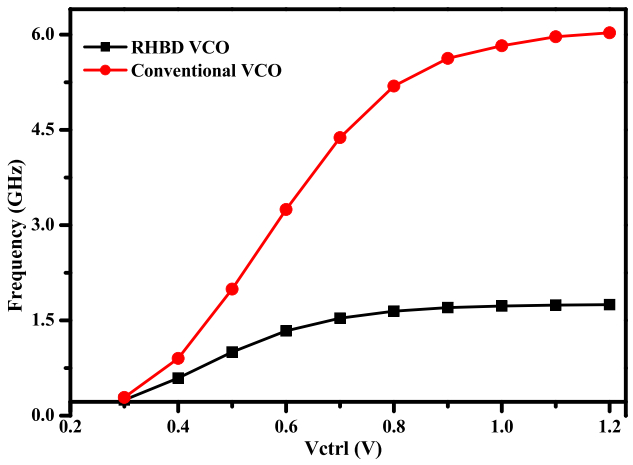


Fig. 16 Performance of the proposed RHBD CSR-VCO compared with conventional five-stage VCO frequency transfer characteristics at $V_{dd} = 1.2$ V

3.4.1 Effect of Process, Voltage and Temperature Variation Under Radiation Strike

The peak current value for DE current Eq. 4 is 30 μA i.e. the deposit total charge at the node is 0.15 pC [39] to find the required parameters of proposed VCO. The oscillation frequency and other parameters of the proposed VCO are calculated at different process corner, voltage, and temperature (PVT) variations which are shown in Figs. 17, 18, and 19, respectively.

The oscillation frequency, power dissipation, and phase noise at 1 MHz offset frequency are calculated under PVT variation. It is found that when the supply voltage (Vdd) increases the oscillation frequency and the power dissipation is increased. The oscillation frequency is increased and the power dissipation is decreased when the temperature is increased of the proposed VCO due to the operating current of the transistor being decreased by increasing temperature. Consequently, the power dissipation is decreased up to a certain temperature. In both cases, the oscillation frequency of the proposed VCO increases with temperature and voltage variation because it depends on the transistor's device current. Phase noise of the proposed VCO is also varied with PVT variation. At different process corners tt (typical-typical), ff (fast-fast), ss (slow-slow) with temperature variation for different parameters of the proposed VCO is calculated as shown in Table 3.

3.5 Power Analysis

The average power dissipation is measured by using a CADENCE Virtuoso ADE-L calculator for both radiation-hardened and conventional VCO. The average power dissipation has decreased accordingly at lower control voltage with lower supply voltage as shown in Fig. 20 for both conventional and the proposed five-stage ring VCO. The gate separation input RHBD technique based CSR-VCO has a low leakage current as compared with conventional CSR-VCO. Therefore, The proposed CSR-VCO has dissipated less power as compared to the conventional five-stage ring VCO.

The comparison of power with the proposed radiation-hardened VCO and PLL with the reported radiation-hardened VCOs and PLLs are presented in Tables 4 and 5. The proposed RHBD VCO has lower power dissipation as compared to the other recently reported VCOs.

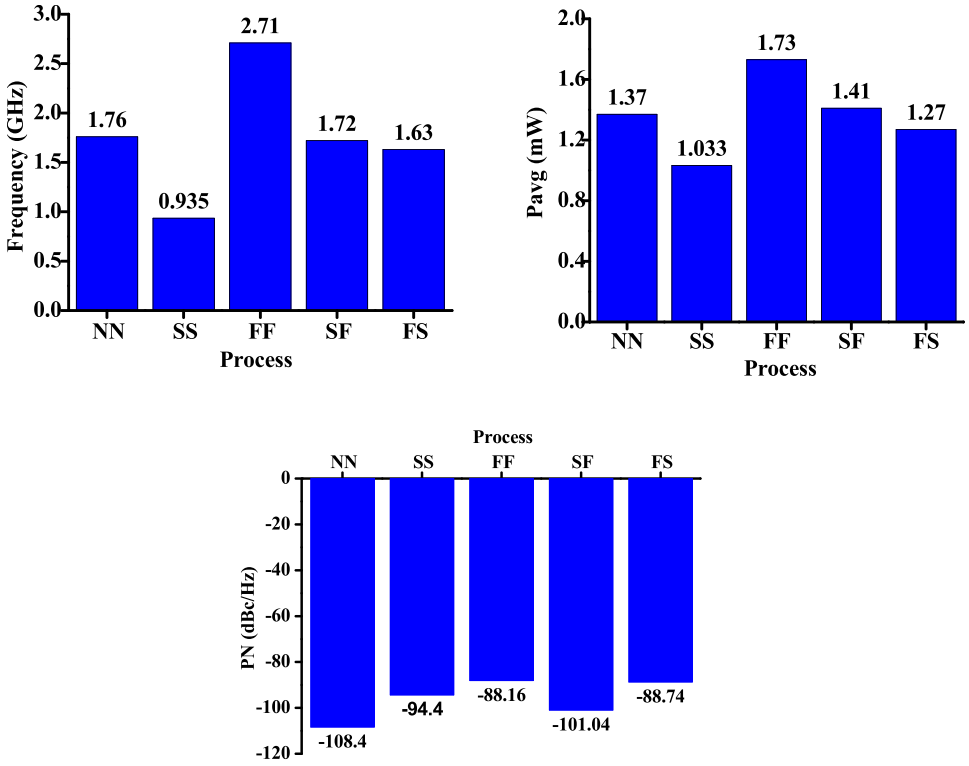


Fig. 17 Process variation of the proposed CSR-VCO

3.6 Performance Comparison

The performance comparison of the proposed CSR-VCO with reported VCOs is presented in Table 1. The reported papers [15, 38] have achieved high oscillation frequency with high power dissipation, a small frequency tuning range, and radiation-intolerant, which makes them unsuitable for high-speed communication applications such as satellite

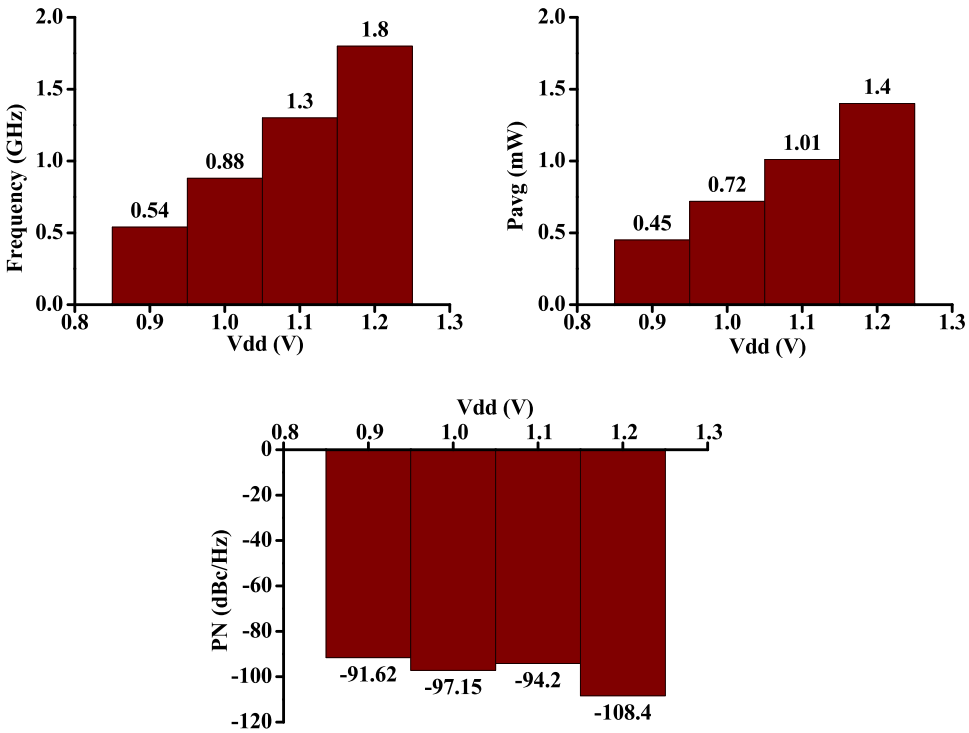


Fig. 18 Supply voltage variation of the proposed CSR-VCO

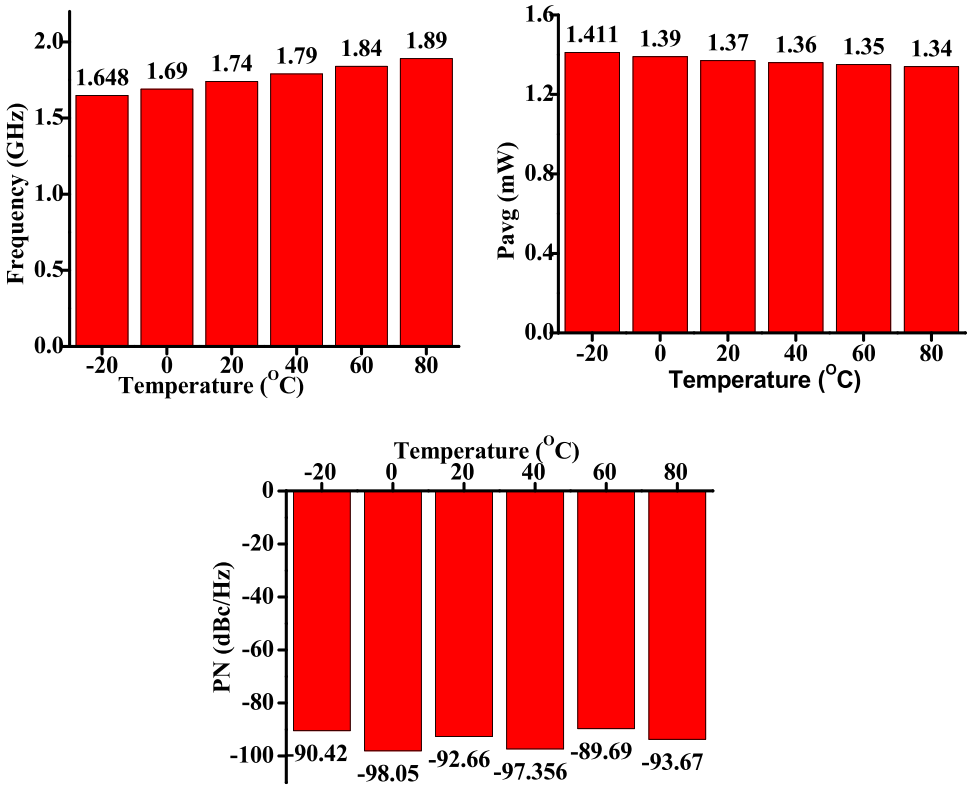


Fig. 19 Temperature variation of the proposed CSR-VCO

Table 3 Performance of the proposed RHBD CSR-VCO at PVT variation

Parameters	tt @ 27 °C	ff @ 80 °C	ss @ -40 °C
P_{avg} (mW)	1.37	1.71	1.10
Frequency (GHz)	1.75	2.88	0.78
Frequency range (GHz)	0.40 - 2.23	0.88 - 3.37	0.11 - 0.80
PN (dB_c/Hz)	−89.04	−106.3	−94.75
Tuning range (%)	82.06	73.89	86.25

Tuning range = $(f_h - f_l)/f_l$, PN- Phase Noise @ 1 MHz

communication. The proposed CSR-VCO provides higher performance compared to the reported works in terms of oscillation frequency, average power dissipation, and tuning range. Additionally, it is radiation tolerant and consumes less power in both 180 nm and 65 nm CMOS technologies using the gate separation input RHBD technique.

The figure of merit (FOM) of the proposed radiation-hardened VCO and PLL can be calculated from the power dissipation and the phase noise of the simulated oscillation frequency by [4]

Table 4 Performance comparison with other recently reported VCOs

Reference	[15]	[38]	[30]	[4]	[14]	[36]	VCO^{180}	VCO^{65}
Year	2017	2019	2021	2022	2022	2023	**2023**	**2023**
Structure	ring	ring	ring	ring	ring	ring	**ring**	**ring**
Technology (nm)	180	40	90	65	22	130	**180**	**65**
Supply voltage (V)	1	1.1	1.2	1.2	0.9	1.2	**1.8**	**1.2**
Oscillation Frequency (GHz)	1.03	1.38	2	1.28	5	0.72	**0.41**	**1.75**
Power dissipation (mW)	2.5	1.1	0.290	7	-	0.799	**0.216**	**1.36**
Frequency tuning range (%)	0.53	37.68	80	-	62	-	**75**	**82**
PN (dB_c/Hz)	−105.5	−98.05	-81	-105	−99.2	-92	**-137.3**	**-108.4**
Radiation-hardened	NO	NO	YES	YES	YES	YES	**YES**	**YES**
FOM(dB_c/Hz)	161.78	160.43	152.39	158.69	-	150.12	**196.21**	**171.89**

Frequency tuning range =$(f_h - f_l)/f_l$, PN- Phase Noise @ 1 MHz, FOM- Figure of Merit

The bold data distinguish between the proposed and the other reported works

Table 5 Performance comparison of previously reported radiation-hardened PLLs to the proposed RHBD PLL

Reference	**Proposed PLL**	[14]	[29]	[27]
Year	**2023**	2022	2017	2021
Technology (nm)	**65**	22	65	65
Supply voltage (V)	**1.2**	0.9	1.0	1.2
Frequency (GHz)	**2.045**	5	2.56	6.25
P_{avg}(mW)	**1.82**	4.87	6	2.85
RMS period jitter (ps)	**1.225**	-	5.6	5.77
Phase noise @ 1MHz	**-135.9**	−99.2	-97	-100
FOM (dB_c/Hz)	**199.513**	166.304	157.383	171.369

The bold data distinguish between the proposed and the other reported works

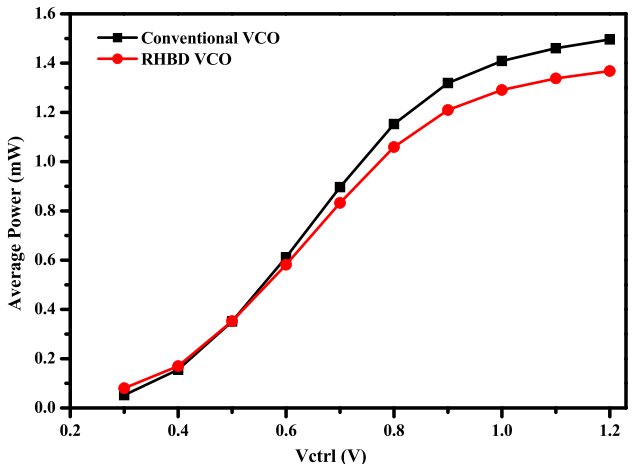


Fig. 20 Average power of the proposed RHBD CSR-VCO compared with conventional five-stage VCO at $V_{dd} = 1.2$ V

$$FOM = 20\log(\frac{f_{osc}}{\Delta f}) - 10\log(\frac{P(mW)}{1mW}) - PN_{dB_c/Hz} \quad (7)$$

where, PN is the phase noise in (dB_c/Hz) at offset frequency (Δf) and f_{osc} is the oscillation frequency of the VCO.

4 Conclusion

The separation of gate inputs technique is used for implementing RHBD based PLL for SET mitigation in a radiation environment. It is found that the proposed RHBD based current starved ring VCO reduces the phase displacement and power consumption by 71.6% and 62.63%, respectively as compared to conventional VCO. The oscillation frequency of the proposed ring VCO is 1.75 GHz. The period jitter reduces 78.13% improvement and FOM 13.72% improvement for proposed RHBD PLL as compared to recently reported RHBD based PLL, respectively. The proposed RHBD based VCO is protected against radiation with deposited charges upto 1050 fC charge. The design is robust and functions under radiation including the statistical mismatches in the transistor. The experimental results show that the RHBD CSR-VCO has a higher figure of merit (FOM) compared to other reported VCOs and PLLs in both 180 nm and 65 nm technologies. This indicates that the RHBD CSR-VCO is capable of achieving high performance and can be effectively used in low-power and high-speed communication applications, even in radiation-prone environments.

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Declarations

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Consent for Publication Not applicable.

Consent for Participate Not applicable.

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Rachana Ahirwar is with Electrical and Electronics Engineering Department at Atal Bihari Vajpayee Indian Institute of Information Technology and Management, Gwalior, MP, INDIA.

Prof. Manisha Pattanaik is a professor of Electrical and Electronics Engineering at Atal Bihari Vajpayee Indian Institute of Information Technology and Management, Gwalior, MP, INDIA.

Prof. Pankaj Srivastava is a professor of Engineering Science at Atal Bihari Vajpayee Indian Institute of Information Technology and Management, Gwalior, MP, INDIA.