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Editorial

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This issue begins with a survey of machine intelligence applications to testing. The topics discussed in the nine following articles are single event upset (SEU), verification, graphics processing unit (GPU), software testing, memory testing, hardware security, and 3-dimensional-stacked device testing. Three papers among these, placed fifth, sixth and eighth, are enhanced and enlarged versions developed by authors from their presentations at the IEEE 24th Latin American Test Symposium (LATS), Veracruz, Mexico, 21-24 March, 2023.

The first article of this issue surveys machine intelligence (MI) applications. This survey examines applications in test methods for analog, radio frequency (RF), digital, and memory circuits. It then lists MI applications to hardware security and emerging technologies, highlights potential research directions, and ends with a long bibliography. Contributors are Roy from Intel Corp., Santa Clara, CA, Millican from Dynetics Inc., Huntsville, AL, and Agrawal from Auburn University, Auburn, AL, USA.

Next three articles focus on the single event upset (SEU) phenomenon in finFET device, phase-locked loop circuit, and FPGA, respectively. Thus, the second article studies the deposited charge in 14nm SOI FinFET. The effects of linear energy transfer (LET), volume of particle hits, characteristic radius, and decay time of Gaussian function for the deposited charge are combined in an analytical model, which is shown to be efficient and accurate. Authors are Liu, Cai, and Li from Air Force Engineering University in China.

The third article presents a radiation-hardened design for phase locked loop (PLL), a circuit used for stable frequency signal generation in electronic systems. Realizing that the most sensitive part in this circuit is a voltage-controlled oscillator (VCO), the proposed design builds the VCO as a ring oscillator with radiation hardened inverters. Actual design and measurements demonstrate effective radiation hardening and tuning range. This work is contributed by Ahirwar, Pattanaik, and Srivastava from ABV-Indian Institute of Information Technology and Management, Gwalior, MP, India.

The fourth article focuses on SRAM-based FPGA (static random-access memory-based field-programmable gate array), often used in aerospace electronics. However, the space radiation environment poses a risk of inducing anomalies in spacecraft FPGA systems, caused from the single event effect (SEE) and space electrostatic discharge (SESD) effect. The paper points out that the SEE can cause either a single or a multi-bit upset but SESD mostly causes multi-bit upsets. Besides, the effect of SESD may also depend on the initial state of the SRAM cell. This research is reported by Cao, Liu, Tian, Zeng and Xue from Yangzhou University, Yangzhou, China, Cai and Cui from Innovation Academy for Microsatellites of Chinese Academy of Sciences, Shanghai, China, Mei and Lv from China Academy of Space Technology, Beijing, China, and Zhao from Harbin Institute of Technology, Shenzhen, China.

The fifth article proposes a formal verification method for optimizing a register-transfer level (RTL) design. The objective is to minimize the hardware area and power consumption while maintaining the required computation accuracy. Authors are Bosio from Ecole Centrale de Lyon, Institute of Nanotechnology, France, Germiniani and Pravadelli from University of Verona, Italy, and Traiola from University of Rennes, Inria, CNRS, IRISA, Rennes, France.

The sixth article explores ways to enhance the reliability of graphics processor units (GPU) in the presence of single event effects (SEE). This work illuststrates the benefits of including special function units (SFU) within the GPU. An SFU consists of dedicated hardware for efficient trigonometric and transcendental operations. Two radiation hardened SFU architectures for GPU are compared with triple modular redundancy (TMR) applied directly to the GPU. These results are presented by Rodriguez Condia, Guerrero-Balaguera, Patiño Núñez, Limas, and Sonza Reorda from Politecnico di Torino, Turin, Italy.

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The seventh article addresses software tests and uses machine learning. Identifying the faulty modules of software with the maximum accuracy, precision, and efficiency are the main objectives of this study. An autoencoder algorithm initially selects the relevant attributes of the training dataset, while a K-means clustering method lowers clustering error and test time. Results on the standard NASA PROMIS data sets are reported. Contributors of this research are Arasteh from Istinye University, Istanbul, Türkiye and Applied Science Private University, Amman, Jordan, Golshan from Tabriz Branch, Islamic Azad University, Tabriz, Iran, Shami from Seraj Institute, Azerbaijan Province, Tabriz, Iran, and Kiani from Fatih Sultan Mehmet Vakif University, Istanbul, Türkiye.

The eighth article develops a design for testability (DFT) scheme for ReRAM memory cells. Resistive random-access memory (ReRAM) is a memory where cells are constructed with memrister, a two-terminal circuit element with certain non-linear electrical behavior. The idea behind this DFT scheme is to enable measurement of the resistive properties of each memory cell. Presenting this work are Copetti, Gemmeke and Bolzani Poehls from RWTH Aachen University, Germany, and Fieback and Hamdioui from TU Delft, The Netherlands.

The ninth spot goes to hardware security. The paper examines diverse types of interference attacks on an IoT (internet of things) network. A simulation-based study suggests defensive measures. Bokka and Sadasivam from Puducherry Technological University, Puducherry, India are contributors of this work.

The tenth article gives a fault-tolerant design for 3-dimensional stacked integrated circuits. Such devices require signal paths known as through silicon vias (TSVs) between stacks. The proposed design duplicates each TSV with a complementary TSV and adds test and repair circuitry. Authors Wen and Huang report this work from National Tsing Hua University, Hsinchu, Taiwan.