



# Failure Probability due to Radiation-Induced Effects in FinFET SRAM Cells under Process Variations

Victor Champac<sup>1</sup> · Hector Villacorta<sup>1,2</sup> · R. Gomez-Fuentes<sup>3</sup> · Fabian Vargas<sup>4</sup> · Jaume Segura<sup>5</sup>

Received: 18 August 2023 / Accepted: 15 January 2024 / Published online: 27 February 2024  
© The Author(s), under exclusive licence to Springer Science+Business Media, LLC, part of Springer Nature 2024

## Abstract

This work studies radiation-induced effects in FinFET technology, the leading technology in advanced nodes for high-end embedded systems. As the fin height (HFIN) and the number of fins (NFIN) are two critical parameters in the development of newer technologies, the soft-error robustness to radiation-induced effects in FinFET SRAM cells with HFIN and NFIN) is evaluated using Technology Computer-Aided Design (TCAD) tools. The ion strike direction and the process variations are considered. An analytical method to evaluate the failure probability of the memory cell due to radiation-induced effects under process variations is proposed. The amount of critical and collected charges of the memory cell are obtained with TCAD tools. The proposed method can be used to get insight into the robustness behavior of the memory cell with HFIN and NFIN and to guide the obtention of HFIN and NFIN parameters in developing new FinFET technologies.

**Keywords** Soft errors · Radiation-induced effects · Failure probability · Memory cell · FinFET technology

## 1 Introduction

Alpha particles from the packaging materials, high energy neutrons from cosmic radiations and the interaction of cosmic ray thermal neutrons are three significant sources of radiation-induced soft errors [3]. In space, high-energy heavy ions may cause damage to human health and electronic components [12]. The energy of incident ions can be reduced after passing through shielding, and even more, secondary particles of lower energy may be produced [12]. Low energy ions with high Linear Energy Transfer (LET)

are also of interest as they cause adverse effects on human health and electronic components [12]. The impact of an oxygen ion on AlGaIn/GaN device was investigated in [15].

Fin Field-effect Transistor (FinFET) technology has become mainstream for advanced nodes due to its improved short-channel effects. Thus, there is a strong interest in better understanding FinFET SRAMs' cell sensitivity to radiation-induced effects. Even more, evaluating the benefits of strategies to mitigate radiation-induced effects in FinFET-based static random-access memory (SRAM) cells is of primary interest. A Single Event Upset (SEU) due to a radiation particle strike on silicon can lead to a system malfunction. Hardening techniques have been proposed to mitigate radiation-induced effects [11]. They are mainly divided into layout-level, circuit-level and system-level techniques [11]. Guard rings and guard drains techniques have been proposed to mitigate the impact of radiation-induced effects in the Complementary Metal-oxide Semiconductor (CMOS) process [16]. Well-configuration techniques have also been proposed [7]. It has been presented in [6] to add complementary doped regions near the active region to generate an electrical field that drives the charge generated by the ion track out of the sensitive terminals. Approaches addressing circuit-level are described in [1, 5, 8, 19, 25]. The use of a built-in current sensor to monitor abnormal current dissipation in the SRAM memory power bus has been proposed in [24]. An abnormal

---

Responsible Editor: L. M. B. Poehls

---

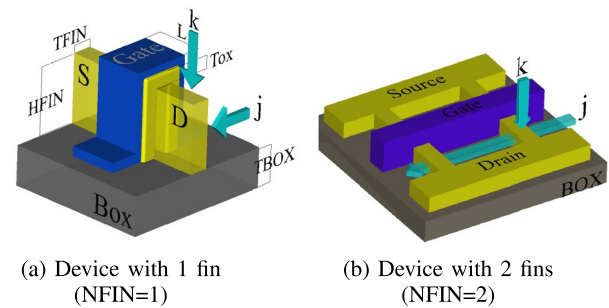
✉ Victor Champac  
champac@inaoe.mx  
Fabian Vargas  
vargas@ihp-microelectronics.com

- <sup>1</sup> National Institute for Astrophysics, Optics and Electronics, INAOE, Andrés Bello, México
- <sup>2</sup> Panamerican University, Mexico City, México
- <sup>3</sup> University of Sonora, Hermosillo, México
- <sup>4</sup> IHP-Leibniz Institute for High Performance Microelectronics, Frankfurt, Germany
- <sup>5</sup> GSE-UIB, University of Balearic Islands, Mallorca, Spain

current indicates a single-event upset (SEU) in the memory. System-level solutions are commonly sitting around the use of error detection and correction (EDAC) approaches [10]. Fin height and the number of fins are critical parameters impacting the performance of FinFET-based circuits. The impact of the fin height on SRAM soft error sensitivity and cell stability is studied in [25]. Technologies with multiple fin heights have improved static noise margin in bulk FinFET SRAM cells [8]. The impact of changing fin height on the DC and RF Performance of a 14-nm silicon on insulator (SOI) FinFET structure is studied in [5]. Reducing the number of fins (fin depopulation) also impacts the performance of FinFET devices [19]. Soft-error rate improvements in 14-nm FinFET technology in comparison to a previous technology node have been found [21]. A more scaled technology uses taller (height) fins and fewer fins. The soft-error rate (SER) behavior with technology scaling is of particular interest [2, 17]. Also, analytical models are of interest to evaluate the impact of radiation-induced effects. An analytical approach to calculate the soft error rate induced by neutrons has recently been proposed [28]. It has been found that process variations may significantly impact the SER behavior in advanced FinFET SRAMs [17].

The main goal of this work is to evaluate the FinFET SRAM cells' failure probability due to radiation-induced effects considering process variations. We focus on memory cell behavior as a function of HFIN and NFIN and their variations. The collected charge in a FinFET-based SRAM cell due to an incident Oxygen ion has been analyzed using 3D TCAD Sentaurus simulations. Different energies for the oxygen ion have been simulated. Even though the results obtained in this work are based on the Oxygen ion, the proposed methodology can be extended to any type of ion element with no prejudice to the quality of the results. The influence of process variations is considered. An analytical formulation is proposed to evaluate the failure probability of FinFET SRAM cells to radiation-induced effects. Results are presented for a 10nm-SOI Tri-Gate FinFET technology.

The rest of the paper is organized as follows: Section 2 presents the basics of the FinFET transistor, process variation modeling, and TCAD Sentaurus simulation setup. Section 3 analyzes the impact of an ion strike on the behavior of a FinFET SRAM cell. LET and ion energy loss, and the collection charge is presented. The electron density profile due to an ion strike is also presented. Section 4 analyzes the impact of HFIN and NFIN on the FinFET SRAM performance under process variations. Section 5 proposes an analytical formulation that considers process variations to compute the failure probability of a FinFET SRAM cell due to an ion strike. Section 6 presents a summary and remarks of the results. Graphical analysis is used to verify the consistent behavior of the proposed analytical formulation. Finally, Section 7 presents the conclusions of the work.



**Fig. 1** Tri-gate FinFET transistors.  $\hat{k}$ : ion strikes with a normal incidence direction and  $\hat{j}$ : ion strikes horizontally the drain body horizontally

## 2 FinFET Transistor and TCAD Sentaurus Simulation Set-Up

### 2.1 FinFET Transistor

Figure 1a illustrates the physical structure of a single fin SOI Tri-Gate FinFET transistor. The metal gate surrounds a thin slice of silicon, known as *fin*, at the two sides and top sides; consequently, three current channels are created. One current channel is created at each side of the fin surrounded by the metal gate, and the third channel is created at the top of the fin. Some essential parameters are indicated in Figure 1a.  $L$  is the channel length,  $HFIN$  is the fin height,  $TFIN$  is the fin thickness,  $TOX$  is the oxide thickness and  $TBOX$  is the buried oxide thickness. Figure 1b illustrates the physical structure of a 2-fins SOI Tri-Gate FinFET transistor.

The FinFET devices have been built with Synopsys Sentaurus TCAD tool [22]. The gate of a FinFET is defined in Sentaurus by wrapping three layers over the fin channel region. The first layer around the fin is the Silicon oxide, the second is the Hafnium oxide, and the third is Titanium nitride. The used FinFET parameters are based on a model card of 10nm Tri-Gate SOI FinFETs (See Table 1). The used device parameters follow ITRS 2010 [27].  $N_{SD}$  is the source and drain doping concentration and  $N_{CH}$  is the channel doping concentration. The power source ( $V_{DD}$ ) is set to 0.8V.

**Table 1** FinFET's parameters used in this work [27]

Parameter	Value
$L(\text{nm})$	10
$TFIN(\text{nm})$	5
$HFIN(\text{nm})$	12.5
$EOT(\text{nm})$	0.585
$N_{SD} (\text{cm}^{-3})$	$3 \times 10^{20}$
$N_{CH} (\text{cm}^{-3})$	$1 \times 10^{15}$
EOT:Equivalent Oxide Thickness	

SRAM cells using FinFETs with multiple fin heights have been discussed in [20]. First, a uniform shallow-trench isolation (STI) recess is made, and then the STI is recessed with a mask. The fin with a second different height is created in the selectively recessed region.

## 2.2 Process Variation Modeling

Process variations in gate work function (WF), channel length (L), fin thickness (TFIN), fin height (HFIN), and oxide thickness (TOX) have been considered. Local variations of individual transistors within SRAM cells are uncorrelated, while global variations of cell transistors are correlated. Local variation of the Gate work function (WF) due to the metal gate granularity is independent for each transistor. WF variation is assumed to have a Normal distribution with  $\sigma_{WF}=20\text{meV}$  [4]. Local variation for L and TFIN is due to Line Edge Roughness. Gate LER (known as GER) is defined for L variation, and Fin LER (known as FER) is defined for TFIN variation. Normal distributions have been assumed to model GER and FER variations with  $\sigma_{GER,FER}=0.66\text{nm}$  [26]. No local variations have been considered for HFIN and TOX. Global variation is assumed to be  $3\sigma=10\%$  from the nominal value for each parameter. HFIN and TOX are not expected to exhibit significant local variation since they are determined by film thickness but not the lithography [14].

## 2.3 TCAD Simulation Setup

3D TCAD simulations with Synopsys Sentaurus TCAD tool suite [22] were used to evaluate the response of FinFET SRAM cells to heavy-ion strikes. Two ion strike conditions have been considered (vertical and horizontal arrows in Figs. 1a and b). In the first condition, the ion strikes at the transistor drain terminal with a normal incidence ( $\hat{k}$  direction) and crosses the drain body vertically. In the second, the ion strikes horizontally the drain body ( $\hat{j}$  direction). The *Linear Energy Transfer* (LET), the ion range depth, and the profile

lateral radius values are the input parameters to the heavy-ion model for TCAD transient simulation. The radial dose model used in [9] determines the profile lateral radius. The spatial charge distribution of the ion track was characterized by a Gaussian distribution function [9]. The charge collection behavior (by means of the LET value) for the different materials has been considered in the TCAD simulation.

## 3 Impact of an Ion Strike on the Behavior of a FinFET SRAM Cell

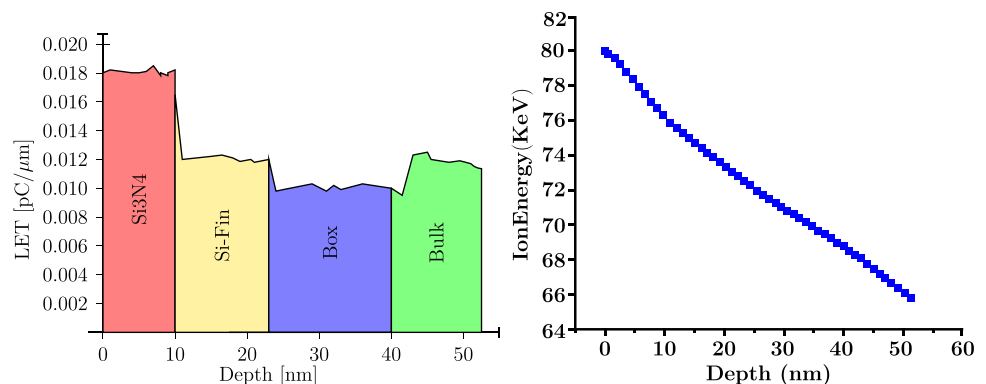
This section analyzes the impact of an ion strike on the behavior of a FinFET SRAM cell. LET and ion energy loss, and the collection charge is illustrated. The electron density profile due to an ion strike is also shown. Ion strikes in 1-fin and 2-fin transistors have been studied.

### 3.1 LET and Ion Energy Loss

LET has been analyzed as a function of the target material depth ( $LET(z)$ ) through different layers. Using SRIM software [31], the LET and ion energy profile as a function of the depth has been obtained. Figure 2a shows the LET for the different layers at the drain region of the FinFET transistor (See Fig. 1), for an Oxygen ion strike with an energy of 80keV in the  $\hat{k}$  direction. It can be observed that the LET presents different magnitudes for each layer (Figure 2a). Figure 2b illustrates the energy loss as the ion track strike penetrates the layers. Energy is lost as the heavy ion penetrates the layers, and generates a large population of electron-hole pair (See Fig. 2b).

Figure 3 shows the LET and ion energy profile as a function of the target material depth for an ion strike in the  $\hat{j}$  direction (See Fig. 1). In this case, the ion Oxygen strikes the drain body horizontally. It can be observed that the ion strike travels through different layers in comparison to an ion strike in the  $\hat{k}$  direction. Lower energy is lost for the case in the  $\hat{j}$  direction.

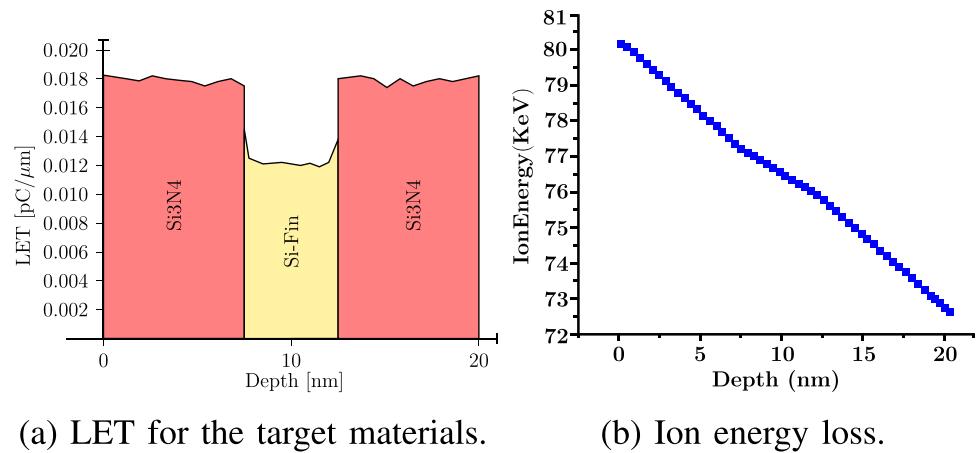
**Fig. 2** LET and ion energy loss for an oxygen ion strike of 80keV in the  $\hat{k}$  direction. NFIN=1



(a) LET for the target materials.

(b) Ion energy loss.

**Fig. 3** LET and ion energy  
Loss for an oxygen ion strike  
of 80keV in the  $\hat{j}$  direction.  
NFIN=1



LET and ion energy profile has also been obtained for a FinFET transistor with two fins (NFIN=2) using SRIM software [31]. The LET and ion energy profile for the case of an ion strike in the  $\hat{k}$  direction is similar to the case with a single fin, as it has been assumed that the ion strikes only one fin. The LET and ion energy profile for the case of an ion strike in the  $\hat{j}$  direction is shown in Fig. 4. It can be observed that higher energy is lost as the ion penetrates through more layers in comparison to the case of an ion strike in a single fin.

### 3.2 Collection Charge

The excess of electrons generated by the ion strike at the silicon fin is collected by the drain terminal of the FinFET transistor. The collected charge ( $Q_{coll}$ ) is different for each strike direction. Figure 5 shows the drain to body transient current generated by the strike of ion oxygen in the  $\hat{k}$  direction. The drain-to-body current is obtained from TCAD simulation. The ion strike causes a transient current from the drain to the body, i.e., from lower to higher potentials (See Fig. 5). In more detail, electrons present much higher mobility than holes, which are left behind,

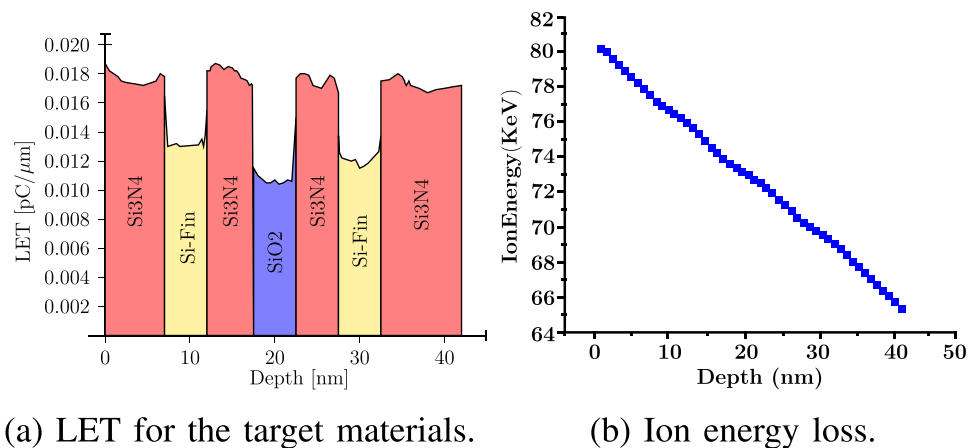
while electrons are fast collected towards higher potentials. Thus,  $Q_{coll}$  is computed as the integral of this transient current. The minimum collected charge that causes a bit-flip in the SRAM cell is called critical charge ( $Q_{crit}$ ).

Figure 6 shows the collected charge ( $Q_{coll}$ ) as a function of oxygen ion energy for strikes in  $\hat{k}$  and  $\hat{j}$  directions. It can be observed that for the same ion energy, for instance, for an ion Oxygen with 20keV, the collected charge in the  $\hat{k}$  direction is larger than for the  $\hat{j}$  direction. In other words, more charge is collected when the heavy ion impacts in the  $\hat{k}$  direction than in the  $\hat{j}$  direction. This is in full agreement with Figs. 2 and 3: as the ion loses more energy in the  $\hat{k}$  direction while crossing the silicon material, and as a consequence, it is also expected that the charge collected in this direction is larger than in the  $\hat{j}$  direction. The deposited charge and bipolar amplification of the parasitic BJT transistor explain the previous behavior.

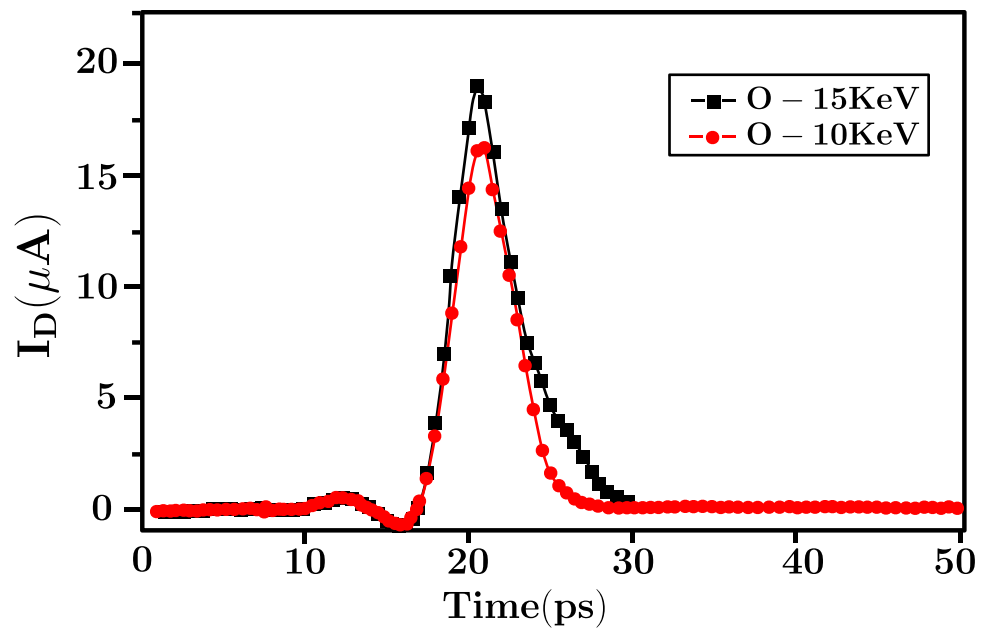
### 3.3 Electron Density Profile to an Ion Strike

The circuit schematic of the studied FinFET SRAM cell designed with 1-fin for the driver transistors (M3 and M5) is shown in Figure 7. Each transistor of the SRAM memory cell

**Fig. 4** LET and ion energy  
Loss for an oxygen ion strike  
of 80keV in the  $\hat{j}$  direction.  
NFIN=2

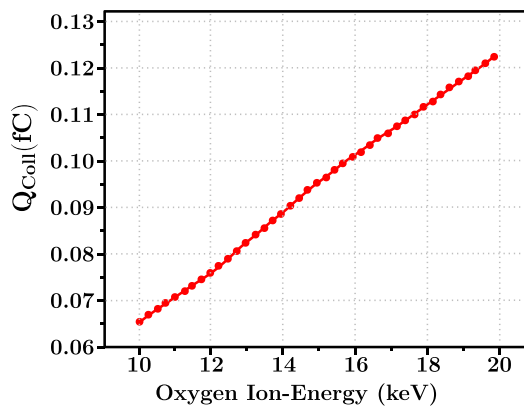


**Fig. 5** Drain-to-body transient current generated by the strike of an ion oxygen in the  $\hat{k}$  direction

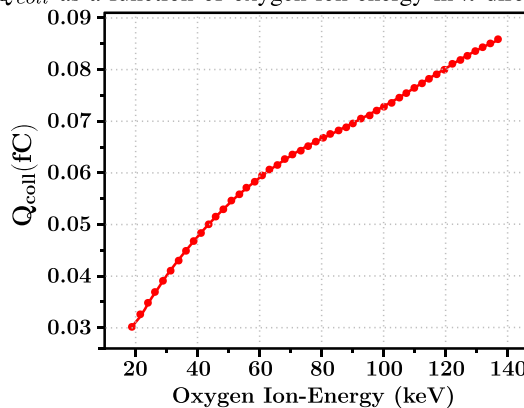


has been created in the TCAD Sentaurus suite tool. An oxygen ion striking the reverse biased depletion region of transistor M5 is considered. When the ion strikes the silicon fin, a track

of electron-hole pairs (EHPs) is generated in the silicon fin, thus, the electron density in the silicon fin changes due to the ion strike. The drain terminal collects electrons, and  $Q_{coll}$  is the amount of the collected charge. The memory flips its stored state if  $Q_{coll}$  is larger than the critical charge ( $Q_{crit}$ ). Assume that a logic '1' is stored at node N2 (See Fig. 7).



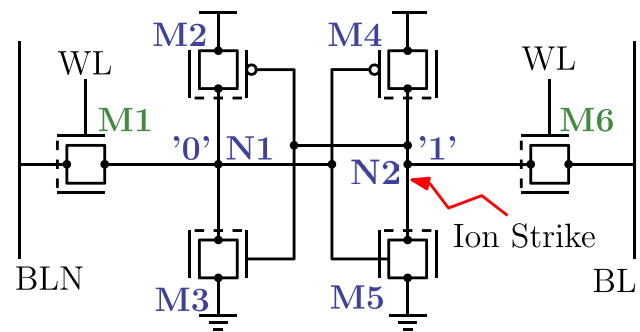
(a)  $Q_{coll}$  as a function of oxygen ion energy in  $\hat{k}$  direction.



(b)  $Q_{coll}$  as a function of oxygen ion energy in  $\hat{j}$  direction.

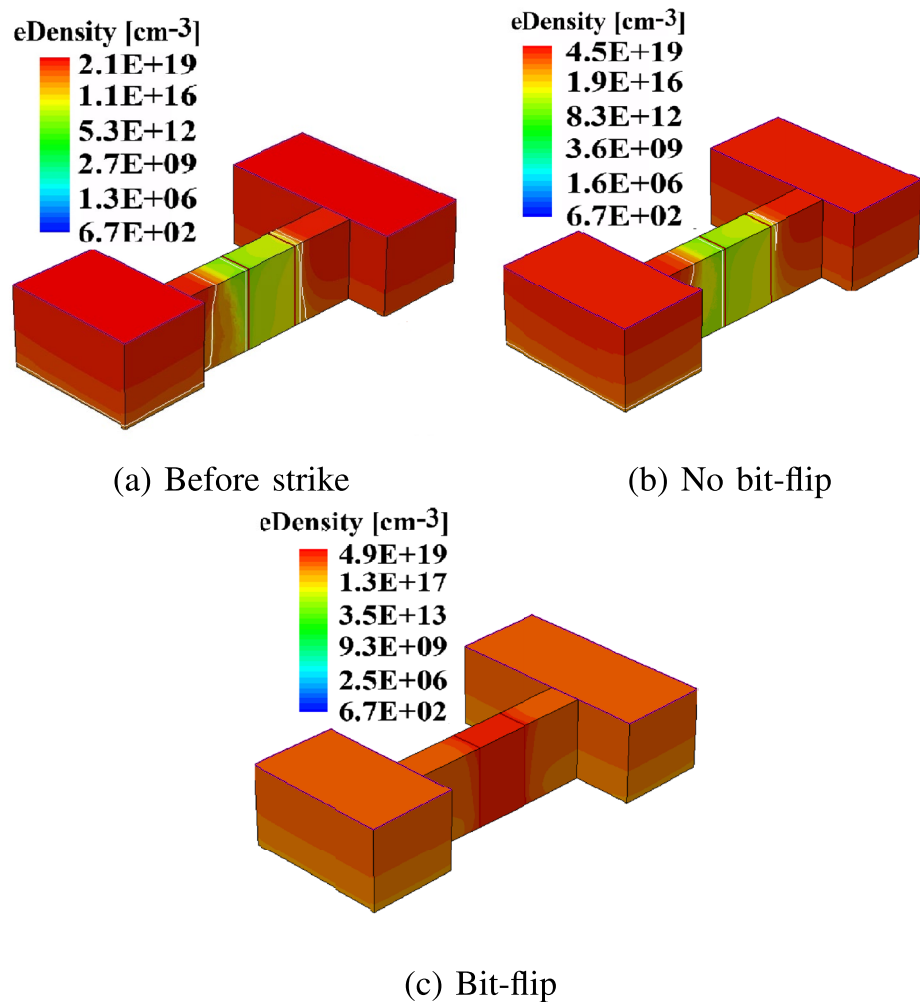
**Fig. 6** Collected charge in drain region due to an oxygen ion strike

- Figure 8a shows the electron density profile before the ion strike (steady-state condition).
- Figure 8b shows the electron density profile at the drain region of transistor M5 when an oxygen ion with the energy of 10keV strikes node N2. The electron density is increased at the FinFET structure, which is higher than for steady-state conditions (See Fig. 8a). However, the energy of the oxygen ion is not enough to cause a bit-flip in the SRAM cell; thus, the electron density progressively decreases, due to the collection of part of the electrons towards higher potentials by one side, and due to the recombination of part of the electrons with holes, by the other side.



**Fig. 7** Schematic circuit of the FinFET SRAM cell

**Fig. 8** Electron density profile of the FinFET structure



- Figure 8c shows the electron density profile at the drain region of transistor M5 when an oxygen ion with the energy of 20keV strikes node N2. In this case, the same physical phenomenon is produced, by since the ion has enough energy (larger than the critical charge) to produce an upset, the SRAM cell flips.

In this case, the same physical phenomenon is produced, by since the ion has enough energy (larger than the critical charge) to produce an upset, the SRAM cell flips.

#### 4 Impact of HFIN and NFIN on the FinFET SRAM Performance

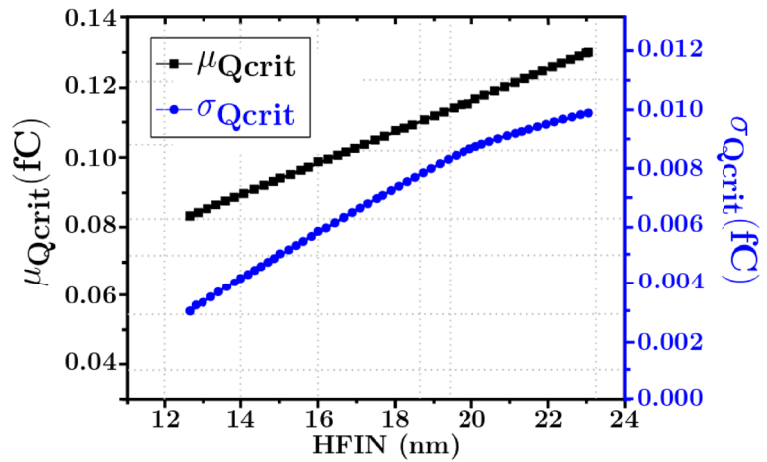
This section illustrates the impact of HFIN and NFIN on the behavior of SRAM cells under process variations. Normal distribution functions have been assumed for  $Q_{coll}$  and  $Q_{crit}$ .  $\mu_{Q_{coll}}$  and  $\sigma_{Q_{coll}}$  are the mean and standard deviation of  $Q_{coll}$ , and  $\mu_{Q_{crit}}$  and  $\sigma_{Q_{crit}}$  are the mean and standard deviation of  $Q_{crit}$ .

The mean and standard deviations of  $Q_{crit}$  and  $Q_{coll}$  have been obtained with Design of Experiments (DOE) analysis using a full factorial design with 3 levels for each parameter [25]. TCAD Sentaurus simulations were carried-out for the DOE analysis.

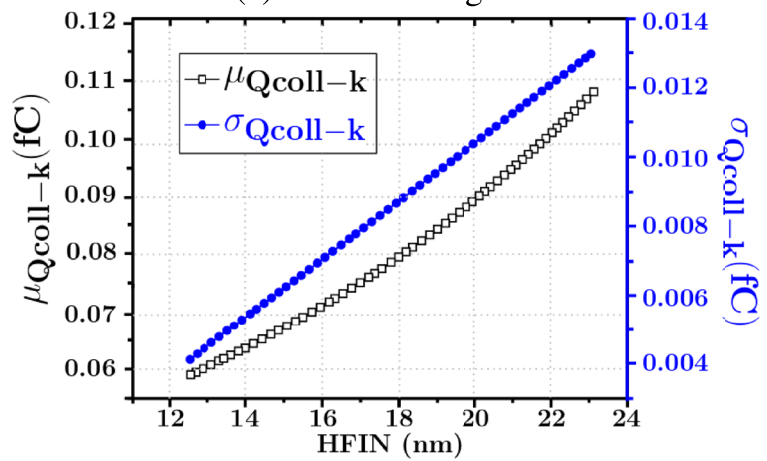
Figure 9 illustrates the impact of an ion strike on the critical and collected charges as a function of HFIN for the 1-fin SRAM cell (See Fig. 7). Ion strikes are considered in the  $\hat{k}$  and  $\hat{j}$  directions. As the dynamic of the charge injection and the operating voltage of the cell are defined, the critical charge depends on the capacitance at node N2 [13]. The critical charge's mean increases as HFIN increases (See Fig. 9). The increase of the critical charge is due to capacitance at node N2 increasing as HFIN increases (See Fig. 9).

The critical charge's standard deviation also increase with HFIN (See Fig. 9a). Increasing HFIN also affects the collection charge mechanism. Figure 9b shows the behavior of the collected charge ( $\mu_{Q_{coll}}$ ) as a function of HFIN. For the  $\hat{k}$  direction,  $\mu_{Q_{coll}}$  increases as HFIN increases. As HFIN increases, the heavy ion range depth into the silicon fin increase (sensitive area). Due to this, more EHPs are generated, increasing the electron density within the fin

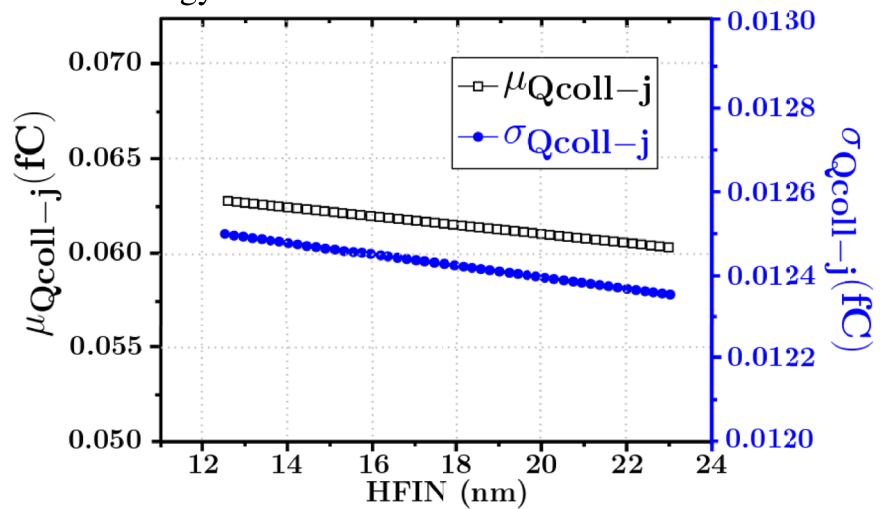
**Fig. 9** Mean and standard deviation of the critical and collected charges for the 1-fin FinFET SRAM cell



(a) Critical charge



(b) Collected charge for an oxygen ion with an energy of 18keV strikes in the  $\hat{k}$  direction.



(c) Collected charge for an oxygen ion with an energy of 100keV strikes in the  $\hat{j}$  direction

and, consequently, increasing the collected charge. A similar trend has been found in [30]. On the other hand,  $Q_{coll}$  barely decreases with HFIN for the  $\hat{j}$  direction (See Fig. 9c). This behavior is because the heavy ion range depth for the  $\hat{j}$  direction almost does not change as HFIN increases.

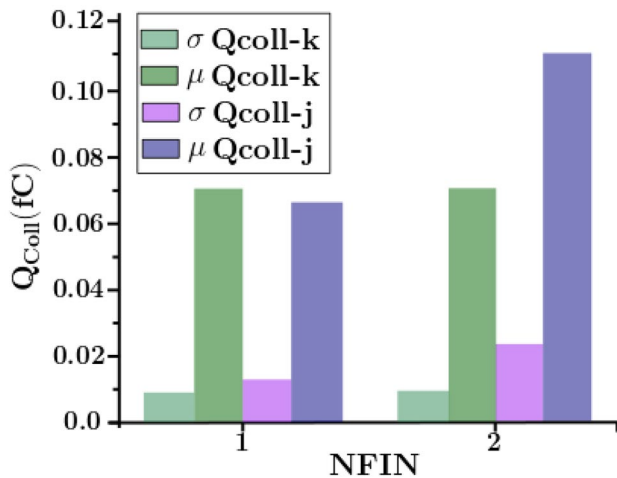
The node capacitance at node N2 (See Fig. 7) increases as NFIN increases, and as a consequence, the  $Q_{crit}$  increases as NFIN increases. It is important to note that NFIN can only take integer values. The  $Q_{crit}$  increases by 80% by increasing NFIN from 1 to 2 fins. The standard deviation also increases by 80%.

Figure 10 illustrates the impact of an ion strike on the collected charges as a function of NFIN for the SRAM cell. For the 2-fin SRAM cell, the driver transistors M3 and M5 in Fig. 7 are designed with two fins.  $\mu_{Q_{coll-k}}$  does not increase as NFIN increases because it has been assumed a single ion is striking the device.  $\mu_{Q_{coll-j}}$  increases as NFIN increases due to a more sensitive area with more fins. The standard deviation of the collected charge change as NFIN increases.

The previous results show that HFIN and NFIN impact the behavior of the memory cell. Even more, process variations must be taken into account as they affect the performance of the memory cell.

## 5 An Analytical Formulation to Compute the Failure Probability of a FinFET SRAM Cell due to an Ion Strike

This section first briefly discuss a simple metric to evaluate the soft-error robustness due to an ion strike. Next, an analytical formulation considering process variations to compute the failure probability of a FinFET SRAM cell due to an ion strike. The proposed method is applied to 1-fin and 2-fin SRAM cells, and finally, the consistent behavior of the analytical formulation is verified.



**Fig. 10** Collected charges for an oxygen ion strike. Used energy is 18keV in the  $\hat{k}$  direction, and 100keV in the  $\hat{j}$  direction, HFIN=16nm

## 5.1 Soft-Error Robustness Metric

The results show that the critical and collected charges' performance depends on HFIN and NFIN. Furthermore, the collected charge is influenced by the direction of the ion strike. Thus, the soft-error robustness (or cell error robustness) depends on  $Q_{crit}$  and  $Q_{coll}$  [23, 32]. The following equation (R) can be used to evaluate the soft-error robustness of the FinFET SRAM cell:

$$R = \frac{Q_{crit} - Q_{coll}}{Q_{crit}} \quad (1)$$

The simple metric that does not consider process variations can be used as a first guess to evaluate the soft-error robustness due to an ion strike. However, the results presented previously show that process variations should be considered.

## 5.2 An Analytical Formulation to Compute the Failure Probability

The failure probability of an SRAM cell due to the impact of an ion strike is  $P_F = P(Q_{coll} \geq Q_{crit})$ . Then, the non-failure probability ( $P(Q_{coll} < Q_{crit})$ ) is  $P_{NF} = 1 - P_F$ .  $P_F$  can be obtained by using the bivariate normal distribution [18],

$$f(x, y)_{Q_{crit}, Q_{coll}} = \frac{1}{2\pi\sigma_{Q_{crit}}\sigma_{Q_{coll}}\sqrt{1-\rho^2}} \exp \left\{ -\frac{1}{2(1-\rho^2)} \left[ \frac{(x-\mu_{Q_{crit}})^2}{\sigma_{Q_{crit}}^2} - 2\rho \frac{(x-\mu_{Q_{crit}})(y-\mu_{Q_{coll}})}{\sigma_{Q_{crit}}\sigma_{Q_{coll}}} + \frac{(y-\mu_{Q_{coll}})^2}{\sigma_{Q_{coll}}^2} \right] \right\} \quad (2)$$

where  $\rho$  is the correlation factor between  $Q_{crit}$  and  $Q_{coll}$ .

$Q_{crit}$  and  $Q_{coll}$  (for  $\hat{k}$  and  $\hat{j}$  directions) have been modeled as a function of the process parameters and NFIN. Normal distributions  $Q_{crit}$  and  $Q_{coll}$  (for  $\hat{k}$  and  $\hat{j}$  directions) are obtained using a full factorial DOE with three levels for each parameter (See Eqs. 3 and 4). The experiments defined by DOE analysis are carried out with TCAD Sentaurus.

$$Q_{coll}|\hat{k}, \hat{j} = \beta_0 + \beta_1.NFIN + \beta_2.TFIN + \dots + \beta_i.TFIN.L + \dots + \beta_n.HFIN^4 \quad (3)$$

$$Q_{crit} = \gamma_0 + \gamma_1.NFIN + \gamma_2.TFIN + \dots + \gamma_i.TFIN.L + \dots + \gamma_n.HFIN^4 \quad (4)$$

The correlation between  $Q_{crit}$  and  $Q_{coll}$  is given by [18],

$$\rho = \frac{E[Q_{coll}Q_{crit}] - \mu_{Q_{coll}}\mu_{Q_{crit}}}{\sigma_{Q_{coll}}\sigma_{Q_{crit}}} \quad (5)$$

The term  $E[Q_{coll}Q_{crit}]$  is the expected value of the product of the random variables  $Q_{coll}$  and  $Q_{crit}$ . This product

can be obtained by using a *Taylor Series* expansion over the  $Q_{crit}$  and  $Q_{coll}$ . Let us make  $Q_{coll} = f(\mu_{x_1}, \dots, \mu_{x_m})$  and  $Q_{crit} = f(\mu_{x_1}, \dots, \mu_{x_m}) \cdot E[Q_{coll}Q_{crit}]$  in Eq. (5) can be obtained by applying the definition of the expected value of a product and central moments to the random variables,

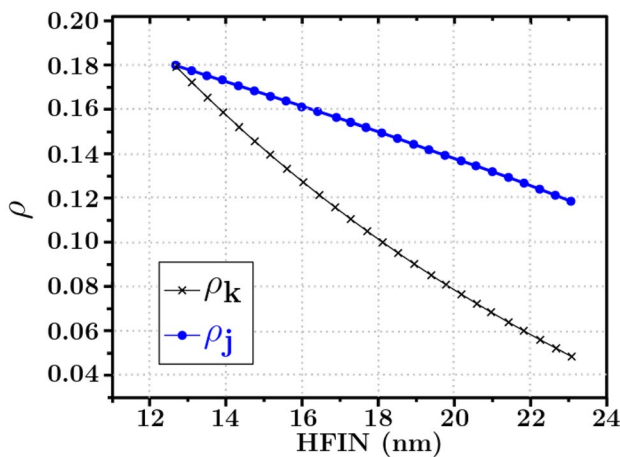
$$E[Q_{coll}Q_{crit}] = Q_{coll}Q_{crit} + \frac{1}{2} \sum_{i=1}^m \left[ Q_{crit} \frac{\partial^2 Q_{coll}}{\partial x_i^2} + 2 \frac{\partial Q_{coll}}{\partial x_i} \frac{\partial Q_{crit}}{\partial x_i} + Q_{coll} \frac{\partial^2 Q_{crit}}{\partial x_i^2} \right] \sigma_{x_i}^2 \quad (6)$$

The  $\rho$  value can be computed using Eqs. (5) and (6). In Fig. 11 is illustrated the  $\rho$  behavior as a function of HFIN. It can be observed that  $\rho$  decreases as HFIN increases for both ion strike directions. Similarly, the  $\rho$  behavior as a function of NFIN can be obtained.

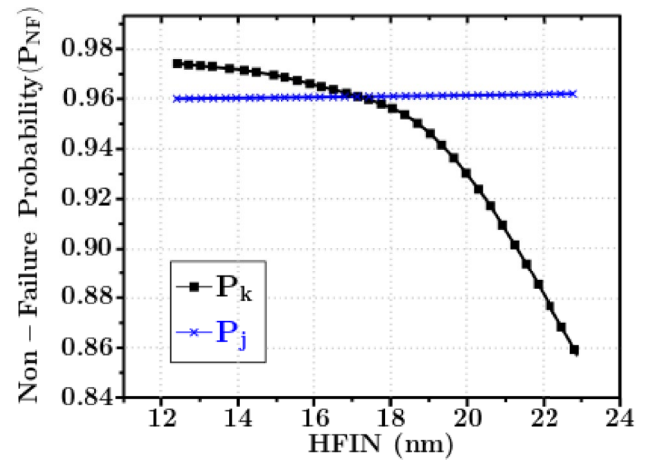
### 5.3 Analysis of the Failure Probability of SRAM Cells due to an Ion Strike

Figure 12 shows the non-failure probability ( $P_{NF}$ ) of the 1-fin SRAM cell for strikes in the  $\hat{k}$  and  $\hat{j}$  directions.  $P_{NF}$  is illustrated for two energy values of the ion strike (18keV and 80keV). Figure 12a shows the non-failure probability in  $\hat{k}$  ( $P_k$ ) and  $\hat{j}$  ( $P_j$ ) directions for an oxygen ion with an energy of 18keV. It can be observed that  $P_k$  exponentially decreases as HFIN increases.  $P_k$  is 0.97 for HFIN=12.5nm, while  $P_k$  is 0.86 for HFIN=23nm. On the other hand,  $P_j$  is 0.96 for HFIN=12.5nm and barely increases as HFIN increases.

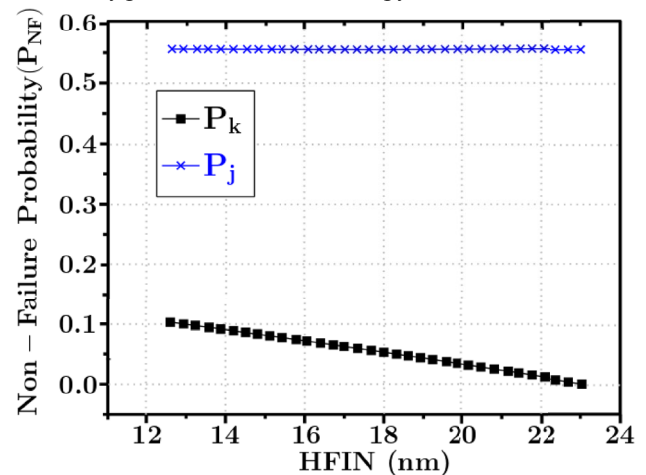
Figure 12b shows the non-failure probability of the 1-fin SRAM cell for an oxygen ion with an energy of 80 keV. It can be observed that  $P_k$  decreases linearly as HFIN increases. The value of  $P_k$  for an oxygen ion with an energy of 80keV is considerably smaller than for the oxygen ion



**Fig. 11** Correlation factor as a function of HFIN. Oxygen ion strike of 18keV



(a) Oxygen ion with an energy of 18keV.



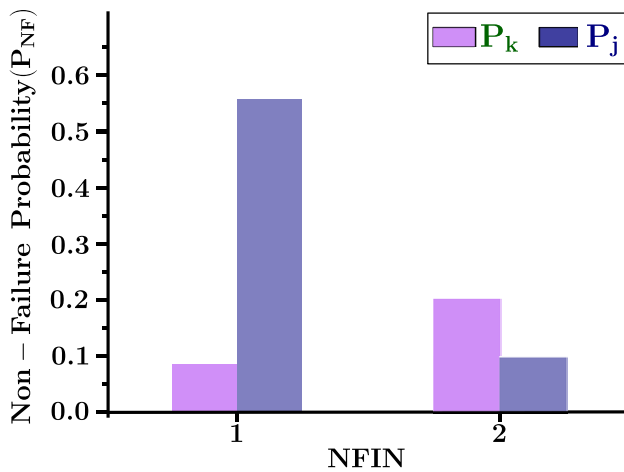
(b) Oxygen ion with an energy of 80keV.

**Fig. 12** Non-failure probability for 1-fin SRAM cell

with an energy of 18keV. The smaller  $P_k$  is because for the oxygen ion with the energy of 80keV, the value of  $Q_{coll}$  is nearly the value of  $Q_{crit}$ . Similarly, the value  $P_j$  is smaller for the oxygen ion with the energy 80keV than for the oxygen ion with the energy of 18keV.  $P_j$  is 0.55 for HFIN=12.5nm and barely increases as HFIN increases.

It should be noted that the behavior of the non-failure probability as a function of HFIN obtained analytically (See Fig. 12) agrees with that observed in the graphical analysis approximation (See Fig. 14).

Figure 13 shows the non-failure probabilities for the 1-fin and 2-fin SRAM cells.  $P_{NF}$  is illustrated only for a single energy value of the ion strike (80 keV). For an ion strike in the  $\hat{k}$  direction, it can be observed that the non-failure probability increases as the number of fins increases. The non-failure probability rises because it has been assumed that a single ion strikes the device, and the critical charge increases for more fins. For an ion strike in the  $\hat{j}$  direction,



**Fig. 13** Non-failure probabilities for 1-fin and 2-fin SRAM cells for a strike with an oxygen ion with an energy of 80keV, HFIN=16nm

it can be observed that the non-failure probability decreases as the number of fins increases. The non-failure probability decreases because the sensitive area to collect charge increases as the number of fins increases.

#### 5.4 Verification of the Proposed Analytical Formulation

Because Monte Carlo simulations would require a significant amount of time in TCAD Sentaurus, the consistent

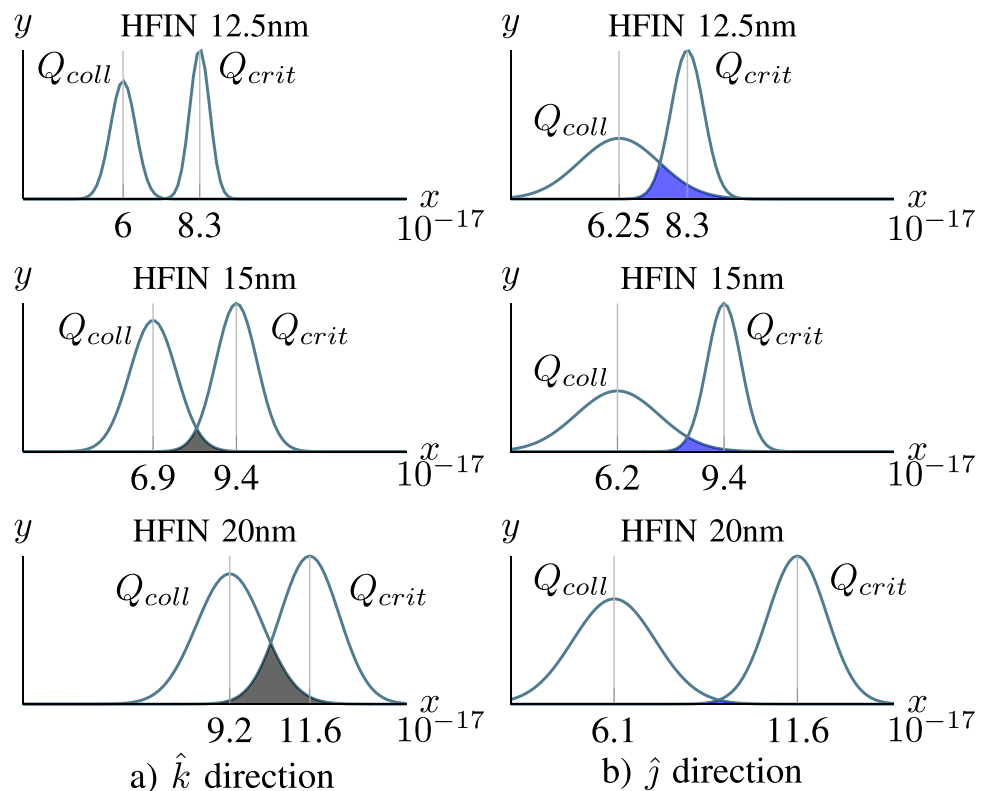
behavior of the proposed analytical formulation is verified by graphical analysis. Figure 14 illustrates the approximated non-failure probability using graphical analysis. For the  $\hat{k}$  direction, the mean and standard deviation are obtained from Fig. 9a. Note that an oxygen ion with an energy of 18 keV was used. The  $\hat{j}$  direction data have been similarly obtained. Let us assume there is no correlation between  $Q_{crit}$  and  $Q_{coll}$ . The memory cell has a failure for those values of  $Q_{coll}$  greater than  $Q_{crit}$ .

- For an ion strike in the  $\hat{k}$  direction (See Fig. 14a), it can be observed that the intersection area of the normal distribution of  $Q_{coll}$  with  $Q_{crit}$  increases as HFIN increases. Hence, the possibility of a non-failure occurrence of the memory cell reduces as HFIN reduces. This behavior is consistent with that observed in Fig. 12a.
- For an ion strike in the  $\hat{j}$  direction (See Fig. 14b), it can be observed that the intersection area of the normal distribution of  $Q_{coll}$  with  $Q_{crit}$  decreases as HFIN increases. Hence, the possibility of a non-failure occurrence of the memory cell increases as HFIN increases. This behavior is consistent with that observed in Fig. 12a.

#### 6 Summary Results and Remarks

Next, the results are summarized and their implications are suggested.

**Fig. 14** Non-failure probability approximation by graphical analysis



**HFIN.-** For an incident ion strike in the  $\hat{k}$  direction, the results obtained in this paper show that both the critical charge and the collected charge increase as HFIN increases, and as a consequence of the combined effect, the non-failure probability decreases as HFIN increases. For an incident ion strike in the  $\hat{j}$  direction, the non-failure probability barely changes as HFIN increases.

**Number of fins.-** For an incident ion strike in the  $\hat{k}$  direction, the non-failure probability increases as the number of fins increases. For an incident ion strike in the  $\hat{j}$  direction, the non-failure probability decreases as the number of fins increases.

The obtained results suggest that increasing the number of fins is an effective way to reduce the non-failure probability. Regarding the incident direction of the ion strike, setting up a proper orientation of the electronic equipment in the field may increase the robustness against radiation-induced effects as suggested in [29].

As a result of this work, it has been found that process variations significantly influence the performance of the FinFET SRAM memory cell under radiation effects. An analytical formulation to compute the failure probability of a FinFET SRAM cell has been proposed. Our work is based on an oxygen ion striking the FinFET SRAM memory cell, but our methodology can be extended to another type of striking particles.

## 7 Conclusion

The behavior of FinFET-based memory cells to radiation-induced effects has been studied using TCAD tools. Our main concern is the impact of HFIN and NFIN on memory cell behavior. The results show that HFIN and NFIN impact the robustness of the memory cell under radiation-induced effects. The ion strike direction also plays an essential role in memory behavior. An analytical method considering process variations has been proposed to evaluate the failure probability due to radiation-induced effects in the memory cell. The impact of HFIN and NFIN is highlighted in the evaluation of the failure probability. Collected and critical charges of the memory cells used to evaluate the failure probability are obtained with TCAD tools. The behavior of the proposed method is in full agreement with graphical analysis. The proposed method can be used to get insight into the robustness of the SRAM cell to radiation induced effects, as function of HFIN and NFIN. Therefore, the proposed method can be used to guide defining the required HFIN and NFIN in the upcoming FinFET technologies. Embedded memory systems devoted to high-end applications will benefit the most from the proposed method.

**Acknowledgements** This work was supported by CONACYT (Mexico) under the postgraduate program No. 212460.

**Data Availability Statement** The datasets generated during and/or analysed during the current study are available from the corresponding author on reasonable request.

## Declarations

**Competing Interest** The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

## References

- Argyrides C, Chipana R, Vargas F, Pradhan DK (2011) Reliability Analysis of H-Tree Random Access Memories Implemented With Built in Current Sensors and Parity Codes for Multiple Bit Upset Correction. *IEEE Trans Reliab* 60(3):528–537. <https://doi.org/10.1109/TR.2011.2161131>
- Azimi S, De Sio C, Sterpone L (2021) Analysis of radiation induced transient errors on 7 nm FinFET technology. *Microelectron Reliab* 126. ISSN 0026-2714. <https://doi.org/10.1016/j.microrel.2021.114319>
- Baumann RC (2001) Soft errors in advanced semiconductor devices-part I: the three radiation sources. *IEEE Trans Device Mater Reliab* 1(1):17–22. <https://doi.org/10.1109/7298.946456>
- Brown AR, Idris NM, Watling JR, Asenov A (2010) Impact of metal gate granularity on threshold voltage variability: a full-scale three-dimensional statistical simulation study. *Electron Device Letters IEEE* 31(11):1199–1201. <https://doi.org/10.1109/LED.2010.2069080>
- Boukourt NEI, Lenka TR, Patane S, Crupi G (2022) Effects of Varying the Fin Width, Fin Height, Gate Dielectric Material, and Gate Length on the DC and RF Performance of a 14-nm SOI FinFET Structure. *Electronics* 11:91. <https://doi.org/10.3390/electronics11010091>
- Calomarde A, Rubio A, Moll F, Gamiz F (2020) Active Radiation-Hardening Strategy in Bulk FinFETs. *IEEE Access* 8:201441–201449. <https://doi.org/10.1109/ACCESS.2020.3035974>
- Chatterjee I, Narasimham B, Mahatme NN, Bhuvu BL, Reed RA, Schrimpf RD, Wang JK, Vedula N, Bartz B, Monzel C (2014) Impact of technology scaling on SRAM soft error rates. *IEEE Trans Nucl Sci* 61(6):3512–3518. <https://doi.org/10.1109/TNS.2014.2365546>
- Chen et al (2013) A 10 nm si-based bulk FinFETs 6T SRAM with Multiple Fin heights technology for 25% better Static Noise Margin. In: *Proceeding IEEE VLSI Technology Symposium (VLSIT)*
- Pageeha O, Howard J, Block R (1994) Distribution of radial energy deposition around the track of energetic charged particles in silicon. *J Appl Phys* 75(5):2317–2321. <https://doi.org/10.1063/1.356274>
- Goerl RC, Villa PRC, Poehls LB, Bezerra EA, Vargas FL (2018) An efficient EDAC approach for handling multiple bit upsets in memory array. *Microelectron Reliab* 88–90:214–218. <https://doi.org/10.1016/j.microrel.2018.07.060>
- Guo J, Zhu L, Liu W, Huang H, Liu S, Wang T, Xiao L, Mao Z (2017) Novel Radiation-Hardened-by-Design (RHBD) 12T Memory Cell for Aerospace Applications in Nanoscale CMOS Technology. *IEEE Trans Very Large Scale Integr Syst (VLSI)* 25(5):1593–1600. <https://doi.org/10.1109/TVLSI.2016.2645282>
- James B, Tran LT, Vohradsky J, Bolst D, Pan V, Carr M, Guatelli S, Pogossou A, Petasecca M, Lerch M, Prokopovich DA, Reinhard MI, Povoli M, Kok A, Hinde D, Dasgupta M, Stuchbery A, Perevertaylo V, Rosenfeld AB (2019) SOI Thin Microdosimeter Detectors for Low Energy Ions and Radiation Damage Studies. *IEEE Trans Nucl Sci* 66(1):320–326. <https://doi.org/10.1109/TNS.2018.2885996>

13. Karnik T, Hazucha P (2004) Characterization of soft errors caused by single event upsets in cmos processes. *IEEE Trans Dependable Secur Comput* 1(2):128–143
14. Lu DD (2011) Compact models for future generation CMOS, Ph.D. dissertation, University of California, Berkeley
15. Mateos-Angulo S, Rodriguez R, del Pino J, Gonzalez B, Khemchandani SL (2019) Single event effects analysis and charge collection mechanisms on AlGaIn/GaN HEMTs. *IEEE Trans Nucl Sci* 35. <https://doi.org/10.1088/1361-6641/ab058a>
16. Narasimham B, Gambles JW, Shuler RL, Bhuva BL, Massengill LW (2008) Quantifying the effect of guard rings and guard drains in mitigating charge collection and charge spread. *IEEE Trans Nucl Sci* 55(6):3456–3460. <https://doi.org/10.1109/TNS.2008.2007119>
17. Narasimham B, Luk H, Paone C, Montoya A-R, Riehle T, Smith M, Tsau L (2023) Scaling Trends and the Effect of Process Variations on the Soft Error Rate of advanced FinFET SRAMs. In: 2023 Proceeding IEEE International Reliability Physics Symposium (IRPS). Monterey, CA, USA, p 1–4. <https://doi.org/10.1109/IRPS48203.2023.10118025>
18. Papoulis A, Pillai SU (2002) Probability, random variables and stochastic processes. McGraw Hill Higher Education. <https://doi.org/10.1109/TASSP.1985.1164715>
19. Ryckaert J, Baert R, Verkest D, Na M, Weckx P, Jang D, Schuddincx P, Chehab B, Patil S, Sarkar S, Zografos O (2019) Enabling Sub-5nm CMOS Technology Scaling Thinner and Taller!. In: 2019 Proceeding International Electron Devices Meeting (IEDM). p 29.4.1–29.4.4. <https://doi.org/10.1109/IEDM19573.2019.8993631>
20. Sachid AB, Hu C (2012) Denser and More Stable SRAM Using FinFETs With Multiple Fin Heights. *IEEE Trans Electron Devices* 59(8):2037–2041. <https://doi.org/10.1109/TED.2012.2199759>
21. Seifert N, Jahinuzzaman S, Velamala J, Ascazubi R, Patel N, Gill B, Basile J, Hicks J (2015) Soft Error Rate Improvements in 14-nm Technology Featuring Second-Generation 3D Tri-Gate Transistors. *IEEE Trans Nucl Sci* 62(6):2570–2577. <https://doi.org/10.1109/TNS.2015.2495130>
22. Sentaurus TCAD (2019) Synopsys. Mountain View, CA, USA
23. Tosaka Y, Kanata H, Satoh S, Itakura T (1999) Simple method for estimating neutron-induced soft error rates based on modified BGR model. *IEEE Electron Device Letters* 20(2):89–91. <https://doi.org/10.1109/55.740661>
24. Vargas F, Nicolaidis M (1994) SEU-tolerant SRAM design based on current monitoring. In: Proceeding of IEEE 24th International Symposium on Fault-Tolerant Computing, Austin, TX, USA, p 106–115. <https://doi.org/10.1109/FTCS.1994.315652>
25. Villacorta H, Segura J, Champac V (2016) Impact of Fin-Height on SRAM Soft Error Sensitivity and Cell Stability. *J Electron Test Theory Appl* 32(3):307–314. <https://doi.org/10.1007/s10836-016-5591-3>
26. Wang X, Brown AR, Cheng B, Asenov A (2011) Statistical variability and reliability in nanoscale FinFETs, Electron Devices Meeting (IEDM), 2011 Proc. IEEE International. <https://doi.org/10.1109/IEDM.2011.6131494>
27. Wang X, Brown AR, Cheng B, Asenov B (2011) Statistical variability and reliability in nanoscale FinFETs, 2011 Proc. International Electron Devices Meeting, Washington, DC, USA, p 5.4.1–5.4.4. <https://doi.org/10.1109/IEDM.2011.6131494>
28. Wrobel F, Aguiar Y, Marques C, Lerner G, Garcia Alia R, Saigne F, Boch J (2023) An Analytical Approach to Calculate Soft Error Rate Induced by Atmospheric Neutrons. *Electronics* 12(1):104. <https://doi.org/10.3390/electronics12010104>
29. Yang S-H, Lei Z-F, Huang Y, Wang S-L, Liang T-J, Tong T, Li X-H, Peng C (2022) Impact of incident direction on neutron-induced single-bit and multiple-cell upsets in 14 nm FinFET and 65 nm planar SRAMs. *Chin Phys B* 31(12)
30. Yu J-T, Chen S-M, Chen J-J, Huang P-C (2015) Fin width and height dependence of bipolar amplification in bulk FinFETs submitted to heavy ion irradiation. *Chin Phys B* 24(11)
31. Ziegler JF (2003) Stopping and Range of Ions in Matter SRIM-2003. [www.srim.org](http://www.srim.org), <https://doi.org/10.1016/j.nimb.2004.01.208>
32. Ziegler JF, Lanford WA (1979) Effect of Cosmic Rays on Computer Memories. *Science* 206(4420):776–788. <https://doi.org/10.1126/science.206.4420.776>

**Publisher's Note** Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

Springer Nature or its licensor (e.g. a society or other partner) holds exclusive rights to this article under a publishing agreement with the author(s) or other rightsholder(s); author self-archiving of the accepted manuscript version of this article is solely governed by the terms of such publishing agreement and applicable law.

**Victor Champac** is a Titular Professor with the National Institute for Astrophysics, Optics and Electronics (INAOE), Puebla, Mexico. He is a Senior Member of IEEE. He serves on the Editorial Board of the *Journal of Electronic Testing: Theory and Applications* (JETTA). He has served as Co-General Chair of the IEEE Latin-American Test Symposiums and participated in the Program Committees of several international conferences. His areas of interest are defect modeling and new test strategies for advanced technologies, process variation tolerant circuit design, reliable analysis and design of neuromorphic computing.

**Hector Villacorta** is a IEEE Member and is currently working with the Polytechnic University of Aguascalientes, Mexico. He also is a member of the Innovative Design and Test Group of the National Institute for Astrophysics, Optics and Electronics (INAOE), Puebla, Mexico and with the Electronic System Group, University of the Balearic Islands, Mallorca, Spain. He has a PhD on Electronics from INAOE. His research interests include new test methods for advanced technologies and very large scale integration (VLSI) circuit design tolerant to process variation and radiation.

**R. Gomez-Fuentes** received the Electrical Engineering Science Master Degree in 2001 from Tecnológico de la Laguna. He received the Ph.D. in 2007 from the National Institute for Astrophysics, Optics and Electronics. In 2009, he joined University of Sonora (México) where is Titular Professor. His research lines include: defect modeling and development of new test strategies in leading technologies, design and test of VLSI circuits, fault detection and diagnosis using artificial neural networks and its applications to VLSI technologies and circuit design under process variations.

**Fabian Vargas** obtained the PhD Degree in Microelectronics from the Institut National Polytechnique de Grenoble (INPG), France, in 1995. At present, he is Senior Scientist at IHP - Leibniz Institute for High Performance Microelectronics, in Germany. He works in the area of computer systems architecture focusing on test, fault-tolerance and security for critical applications. F. Vargas has served as Technical Committee Member and Guest-Editor in many IEEE-sponsored conferences and journals. He holds 8 BR and international patents, co-authored a book and published over 200 refereed papers. co-founded the IEEE-Computer Society Latin American Regional Test Technology Technical Council (LA-TTTC) in 1997 and the IEEE Latin American Test Symposium - LATS (former Latin American Test Workshop - LATW) in 2000. F. Vargas received for several times the Meritorious Service Award of the IEEE Computer Society for providing significant services as chair of the IEEE LA-TTTC and LATS. F. Vargas is Senior Member of IEEE and Golden Core Member of the IEEE Computer Society.

**Jaume Segura** is a Full Professor in the Electronic System Group, University of the Balearic Islands, Mallorca, Spain. His research interests include device and circuit modeling and very large scale integration (VLSI) design and test. He has a PhD in electronic engineering from the Polytechnic University of Catalunya, Barcelona, Spain.