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A Quadruple-Node Upsets Hardened Latch Design Based on Cross-Coupled Elements

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Abstract
With the continuous scaling of CMOS technology, single-event multi-node upsets (MNU) induced by charge sharing has continued to occur in latches when hit by high-energy particles. This paper presents a quadruple-node upset (QNU) tolerant latch design (referred to as P-DICE latch) to achieve both high reliability and low area overhead. The P-DICE latch takes advantage of the error-blocking properties of Cross-Coupled Element and C Element to tolerate QNU, and achieves 100% self-recovery of SNU and DNU. Compared with previous eight MNU hardened latches, the P-DICE latch has the lowest overhead in terms of area, area-power-delay product (APDP), and area-power-delay soft error rate ratio product (APDSP), and has the highest critical charge. Moreover, the proposed P-DICE latch can tolerate QNU caused by high-energy particles to ensure the reliability of the circuit. Compared with eight MNU hardened latches, the proposed P-DICE latch achieves 24.58% reduction in area, 33.05% reduction in power, 17.19% reduction in delay, 48.29% reduction in area-power-delay product, 61.60% reduction in APDSP, and 142.82% improvement in critical charge on average.

Keywords Radiation hardening · Soft error · Quadruple-node upsets · Reliability

1 Introduction

With the scaling of semiconductor technology, digital circuits are becoming more susceptible to soft errors with reduction of supply voltage and increase of transistors density [1]. Especially integrated circuits in aerospace applications are often affected by a series of destructive forces: solar wind, extreme temperature fluctuations, cosmic radiation and Van Allen radiation belt, which generate α Particles, neutrons and heavy ions. When an energetic particle hits the diffusion region of a reverse bias transistor, a soft error can occur [2–5].

In addition, in nanoscale CMOS technology, large-scale integration and reduced transistor sizes may cause single particle charge collection when particles impact, thus may affecting double adjacent nodes, triple adjacent nodes and even quadruple adjacent nodes. Soft errors include single-node upset (SNU), double-node upsets (DNU), triple-node upsets (TNU), and even quadruple-node upsets (QNU), etc. Soft errors can severely affect the reliability of safety–critical applications, especially for those circuits and systems used in harsh radiative environments such as aerospace. The existing SNU hardened scheme is not effective because of multiple-node upset induced by charge sharing in nanometer scale. Soft errors are transient faults, so the radiation hardening by design (RHBD) methods can be used to eliminate soft errors and recover correct data. In fact, some TNU tolerant latches have been proposed [6–8], and these designs are mainly used in applications with

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harsh radiation environments. As pointed out in [7], the DNU self-recovery ability is also important for aerospace applications. With the increase of density and possibility of charge sharing induced multiple-node upset, the logic states of adjacent nodes are more and more susceptible to each other in case of high-energy particle striking. Clearly, design for reliability against SNU only are no longer sufficient for safety–critical applications. Therefore, not only SNU, DNU and TNU, but also QNU needs to be taken into account in nanometer technology.

Many novel hardened latches have been proposed to effectively tolerate single-event multiple-node upsets (MNU) [9–13]. For example, [9] uses the method of multiple voters, but it cannot self-recover, even the SNU, it cannot self-recover; in [12], the feedback method is used to tolerate DNU, but the area cost is larger at the same time; the structure proposed in [14] can only tolerate DNU, and in the case of TNU, the wrong logic value will be stored in the latch. Increasing drive ability of part of the transistors appear to be an effective way to tolerate soft errors, but the nodes still upset in high-energy particle. Similarly, layout-based hardened schemes (e.g., increased node spacing) can make the latch MNU-tolerant, but these techniques increase the complexity of the integrated circuit design [14]. Therefore, the RHBD techniques is an effective way to tolerate soft error.

This paper focuses on the radiation hardening by design of the latch. Previous hardening techniques mainly focus on SNU or DNU hardening based on spatial redundancy, such as (Dual Modular Redundancy) DMR, (Triple Modular Redundancy) TMR and (Mutual-Interlock Construction for Nodes) MICN [15]. Latches employing DMR, TMR and MICN techniques such as (Feedback Redundant SEU/SET-tolerant Latch) FERST [16], TMR [17] and (Dual Interlocked storage Cell) DICE [18] are typical examples of SNU hardened structures. Unfortunately, single-node hardened design solutions are no longer adequate for high reliability. So many DNU hardened latches have been proposed, e.g., DONUT [19], LIHL [20]. In addition, in the past few years, researchers have started to consider TNU and QNU hardening for high robustness. These schemes can fully tolerate TNU or QNU, with the cost of low critical charge and high area overhead.

In order to alleviate the problems of existing hardened latches, based on the RHBD methods, this paper proposes a QNU-tolerant latch named as P-DICE latch. The latch takes advantage of the error blocking ability of the Cross-Coupled Element (referred to CCE) and the C Element (referred to CE) to achieve QNU tolerance. The P-DICE latch mainly consists of a P-DICE loop consisting of twenty CCEs and a CE, with tolerance of TNU/QNU and 100% self-recovery of SNU/DNU. Due to the use of clock-gated technology and fewer transistors, the P-DICE latch is optimal in terms of area, APDP, APDSP and critical charge compared to the latest QNU hardened latches.

The rest of this paper is organized as follows: Section 2 discusses existing hardened latches. Section 3 details the implementation of the proposed latch design, the fault tolerance principle, and simulation results. Section 4 gives the results of the data comparison. Section 5 concludes the paper.

2 Existing Hardened Latch Designs

In the classical design of radiation hardening, CE and DICE are frequently used. Figure 1 shows the schematic of these CEs and DICEs. Figure 1(a)–(i) show the CCE, transmission gate (TG), DICE, clock-gated DICE, two-input CE, clock-gated two-input CE, three-input CE, four-input CE, and five-input CE, respectively. The basic principle of the CE is that the CE acts as an inverter when the input values of the CE are the same. However, when the input value of CE is different, CE goes to a high impedance state (retaining the previous output value). Therefore, CE can block the propagation of soft errors. The clock-gated CE can be controlled by a clock signal (CK) and a complementary clock signal (NCK). The basic principle of the DICE is to take advantage of the error-blocking ability of the CCE with a dual modular redundance to achieve 100% self-recovery of SNU. The CE and DICE are the most frequently used structures in the hardened structures. This is not only because CE has excellent blocking ability and DICE has self-recovery ability, but also because they achieve both blocking and self-recovery functions stably at the same time, and the number of transistors is minimal, so these structures are often used in hardened structures. In this section, we will introduce several newly multi-node-upset hardened latches based on CE and DICE proposed in recent years.

Figure 2(a) shows the TNU-latch [21]. The TNU-latch can prevent the propagation of TNU errors to the output Q. However, this structure uses many transistors, which leads to high area overhead and power consumption. Figure 2(b) shows the D-latch [22]. The D-latch is a QNU tolerant latch that can prevent QNU propagating to the output Q. However, the use of clock-gating to all six CEs causes a very serious glitch at the output Q. This glitch may propagate to the next level of logic circuits, making errors in logic circuits and affecting circuit reliability. Figure 2(c) shows the LCQNUSR [23]. LCQNUSR does not actually tolerate QNU completely, even in some DNU cases, and Q will remain in a wrong logic state and cannot self-recovery. For example, if Q and N_3 are upset at the same time, Q will keep the wrong logic state without self-recovery. So this structure is a pseudo QNU hardened latch, or even a pseudo DNU hardened latch because it cannot completely tolerate DNU.

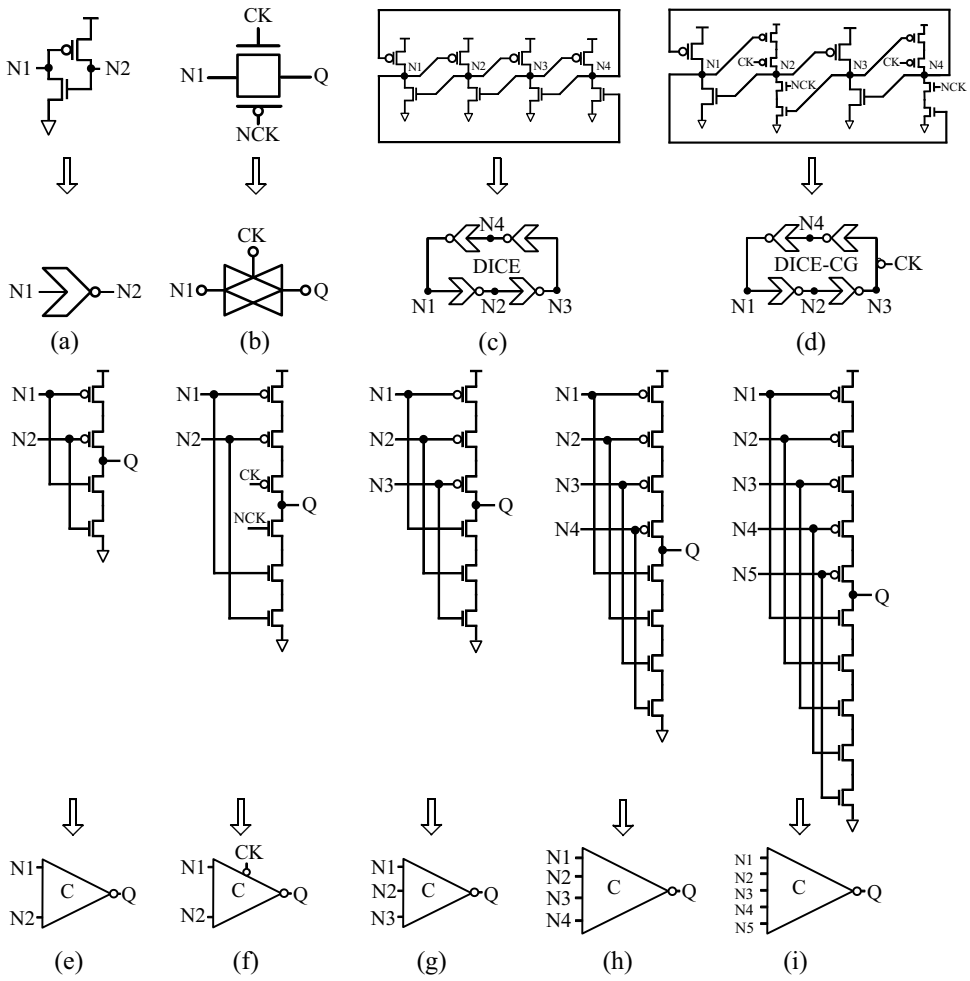

Fig. 1 Structures of CEs and DICEs. **a** CCE. **b** TG. **c** DICE. **d** Clock-gated DICE. **e** Two-input CE. **f** Clock-gated two-input CE. **g** Three-input CE. **h** Four-input CE. **i** Five-input CE

Figure 2(d) shows the 4NUHL [24]. 4NUHL is able to tolerate QNU. But 4NUHL cannot achieve 100% self-recovery of DNU. In addition, 4NUHL occupies high power consumption due to large number of transistors used. Figure 2(e) and (f) show the QNUTL and the QNUTL-CG [25], respectively. QNUTL-CG uses a clock-gating technique on the DICE to reduce power consumption compared to QNUTL. Similar to the 4NUHL, these two latches cannot fully achieve 100%

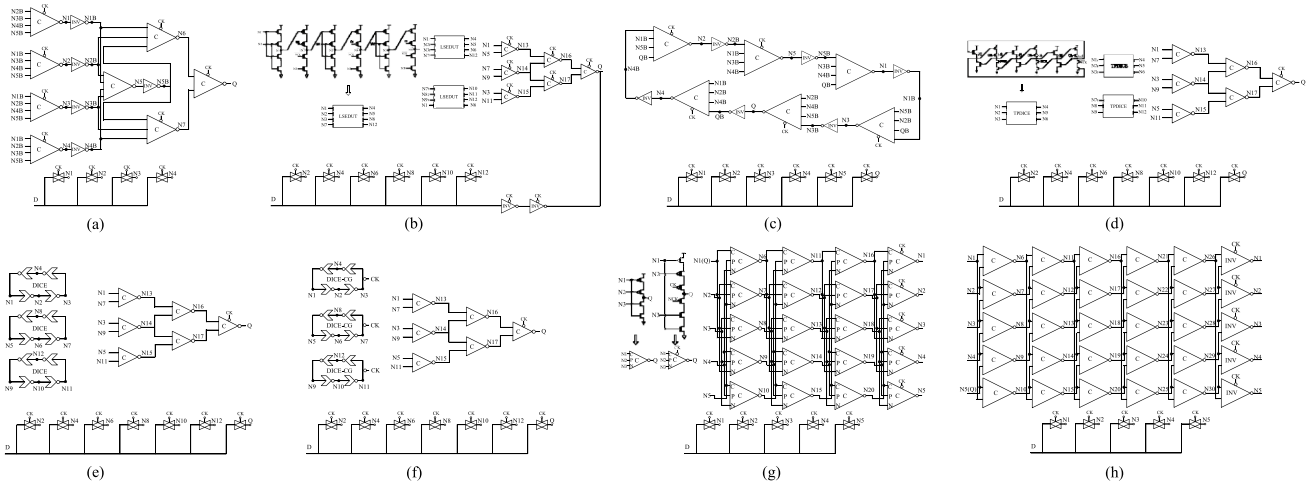

Fig. 2 Typical MNU-hardened latches. **a** TNU-latch. **b** D-latch. **c** LCQNUSR. **d** 4NUHL. **e** QNUTL. **f** QNUTL-CG. **g** ISC-QRL. **h** QRHIL

self-recovery of the DNU, and the power consumption is relatively high. Figure 2(g) shows the ISC-QRL [26]. ISC-QRL cannot be self-recoverable in some case of QNU. For the node group {N_1 (Q), N_2, N_8, N_{15}}, when Q is upset from 0 to 1, Q keeps the wrong logic value that cannot be recovered. Therefore, this structure is a pseudo QNU hardened latch and has a large area and power consumption. Figure 2(h) shows QRHIL [27]. QRHIL can fully tolerate QNU, but the power consumption is large.

3 The Proposed Latch Design

3.1 Circuit Schematic and Fault Tolerance Principle

The circuit schematic of the proposed P-DICE latch is shown in Fig. 3. The latch consists of a ring P-DICE composed of five DICEs (consist of twenty CCEs), a five-input clock-gated CE, and six TGs. P-DICE is used to maintain the correct logic value during the latching period, achieving 100% self-recovery of SNU and DNU. A five-input clock-gated CE is used to block soft error. TG is used to initialize the latch logic value. In the latch, D and Q are input and output respectively. NCK is the complementary clock signal of CK.

When CK = 1 and NCK = 0 (TGs are on), the latch works in the transparent period. D propagates to internal nodes N_1, N_3, N_5, N_7, N_9 and Q. Then, N_2, N_4, N_6, N_8, N_{10}, N_{11}, N_{12}, N_{13}, N_{14}, N_{15} will turn to the complementary logic value of D. Note that at this time, CE is off and D propagates to Q only through a TG. CE is closed by CK and NCK during the transparent period to reduce the current competition phenomenon and transmission delay.

When CK = 0 and NCK = 1 (TGs are off), the latch switches to latching period. At this time, the logic value of Q is determined by the logic values of the five internal nodes N_2, N_4, N_6, N_8 and N_{10}. Since the soft errors generated during the transparent period will be refreshed by input D, so the point is to deal with soft errors during the latching period. Next, we discuss the fault tolerance principle of SNU/DNU/TNU/QNU during the latching period.

In this paper, the schematic shown in Fig. 1(a) represents the CCE, when the N_1 of the CCE is 0, the PMOS is on. At this time, the N_2 is 1 and the NMOS is on, and this state is called the CCE on-state. Similarly, when the N_2 of CCE is 1, it will also make CCE on. When the N_1 of CCE is 1 and the N_2 is 0, both PMOS and NMOS transistors of CCE are off, and this state is called the off-state of CCE.

When the CCE is on, it has the ability of error blocking. We take the case of N_1 upset from 0 to 1 for example. At this time, PMOS transistor is off, NMOS transistor is on. N_2 can restore the logic value of N_1 by turning on the NMOS transistor. So, if one node upset to the wrong logic state while the CCE is on, it does not propagate to the other node of the CCE. When the CCE is off, we take the case of N_1 upset from 1 to 0 as an

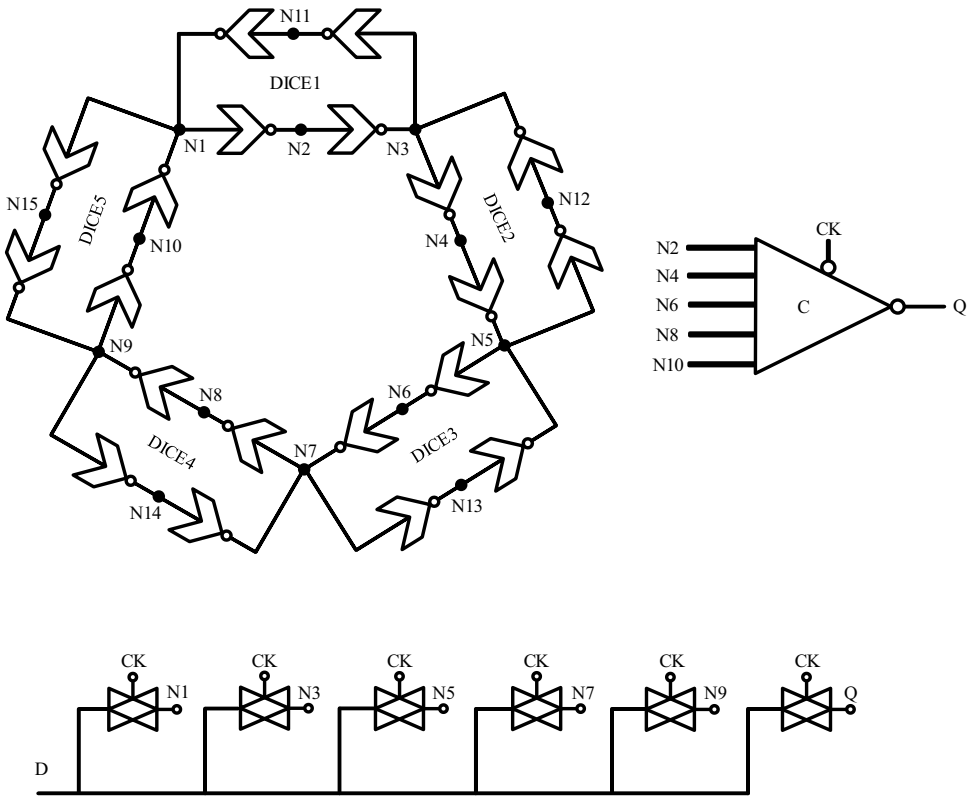

Fig. 3 Schematic of the proposed P-DICE latch

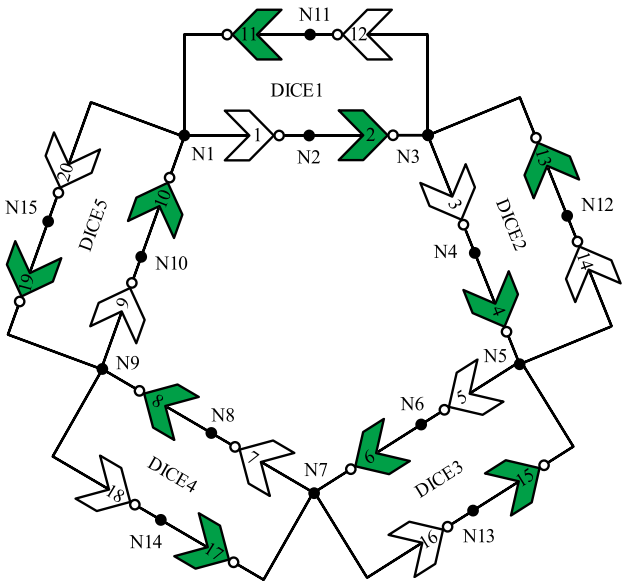

Fig. 4 D = 1 working state of P-DICE latch (green indicates on-state, white indicates off-state)

example. It will cause both MOS transistors to turn on, and CCE is on. So, a CCE in an off-state cannot tolerate SNU at either node. Since the CCE has error blocking ability in the on-state, the SNU can only affects the neighboring nodes.

We take the case of D = 1 for fault tolerance analysis for example. Internal nodes $N_1 = N_3 = N_5 = N_7 = N_9 = 1$. As shown in the Fig. 4, we use CCE_1 to represent the CCE between nodes N_1 and N_2:

First, SNU is considered. DICE uses the CCE with error blocking and dual mode redundancy structure design, so when SNU occurs, it can self-recover from any SNU. Obviously, the proposed latch can tolerate SNU.

Then, DNU is considered. P-DICE latch has 100% self-recovery ability of DNU. For example, if node pair $\{N_1, N_2\}$ are upset, CCE_{10} and CCE_{11} are off, CCE_1 and CCE_{20} are on. Because N_{10}, N_{11} still maintain the correct logic value, so CCE_{10} and CCE_{11} are still on, it can restore the logic value of nodes N_1 and N_2. And since N_{15} is a node inside $DICE_5$, it will only generate a glitch and will soon recover itself. The other DNU cases can be followed by analogy. The DNU injections in Fig. 5(b) confirms that the P-DICE latch can achieve 100% self-recovery of the DNU.

Next, TNU is considered. In this case, according to the soft error tolerance methods, it can be divided into two categories, TNU self-recovery category and TNU blocking category. And then subdivided into 12 types of TNUs according to the number of affected nodes in each DICE.

Since the reason is based on the classification of affected nodes in DICE, a part of the TNU blocking category is self-recoverable. The statistics for each type of TNU are shown in the following Table 1.

Note: "☆" means that one node is upset, "☆☆" means that two nodes are upset, and so on. The black "★" represents non-shared nodes, such as nodes N_2 and N_{11} within $DICE_1$; the colored "★★★" represents shared nodes, and the same-colored nodes represent the same node that is shared. In the first row, for example, the node N_1 is in both $DICE_1$ and $DICE_5$, so node N_1 is represented in red, and similarly, node N_3 is represented in blue. The last row S/T represents the self-recover number divided by the total number.

The TNU self-recovery category is exemplified by the type 1: one DICE has three upset nodes and each of two DICEs has only one upset node such as $\{N_1, N_2, N_3\}$ and $\{N_1, N_{11}, N_3\}$. If node group $\{N_1, N_2, N_3\}$ are upset, N_1 upset from 1 to 0, CCE_1 is on, N_2 becomes wrong logic value 1; N_3 upset from 1 to 0, CCE_{12} is on, N_{11} upset to

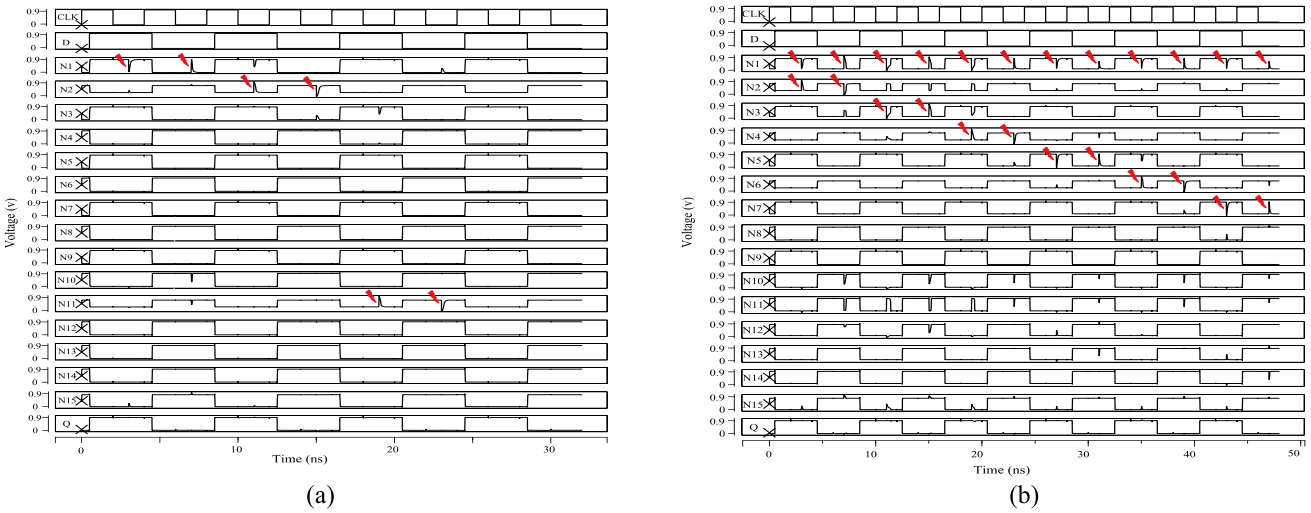

Fig. 5 **a** The results of SNU injection. **b** The results of DNU injection

Table 1 The Statistics for Each Type of TNU

Type	$DICE_1$	$DICE_2$	$DICE_3$	$DICE_4$	$DICE_5$	Example	S/T
1	★★★	★			★	{N_1 , N_2 , N_3}	35/35
2	★★★				★	{N_1 , N_2 , N_{11}}	
3	★★	★	★	★	★	{N_1 , N_3 , N_7}	
4	★	★	★	★	★	{N_1 , N_5 , N_8}	
5	★★	★★	★		★	{N_1 , N_3 , N_5}	288/420
6	★★	★★			★	{N_1 , N_3 , N_4}	
7	★★				★★	{N_1 , N_2 , N_{10}}	
8	★★	★	★		★	{N_1 , N_3 , N_6}	
9	★★	★			★	{N_1 , N_2 , N_4}	
10	★★	★				{N_2 , N_4 , N_{11}}	
11	★	★	★		★	{N_1 , N_4 , N_6}	
12	★	★	★			{N_2 , N_4 , N_6}	
			Total				323/455

wrong logic value 1. Then all four nodes N_1, N_2, N_3 and N_{11} in $DICE_1$ are upset, and the upset of N_1 and N_3 will turn on the CCE_{20} and CCE_3 at the same time. However, since nodes N_4 and N_{15} are within different $DICE_2$ and $DICE_5$ without shared nodes. It is equivalent to recovery of single node upset for $DICE_2$ and $DICE_5$. Therefore, upsets at N_4 and N_{15} only generate a glitch and $\{N_4, N_5\}$ will not upset to the wrong logic value. At the same time, since N_{10} and N_{12} still maintain their correct logic values, N_1 and N_3 can be restored to their correct logic values via CCE_{10} and CCE_{13}, and N_1 and N_3 can be restored to correct logic values via CCE_{11} and CCE_2 for N_{11} and N_2 nodes. That is, the TNU can be self-recover in this case, so the wrong logic value will not propagate to Q.

The TNU blocking category is exemplified by the type 5: two DICEs have two upset nodes and two DICEs each has only one upset node. For example, when node group $\{N_1, N_3, N_5\}$ are all upsets, then CCE_2, CCE_4, CCE_{10}, CCE_{11}, CCE_{13}, CCE_{15} turn off, CCE_1, CCE_3, CCE_5, CCE_{12}, CCE_{14}, CCE_{20} turn on, then $DICE_1$ (N_1, N_2, N_3, N_{11}) and $DICE_2$ (N_3, N_4, N_5, N_{12}) are all upsets to the wrong logic values. However, N_6 and N_{15} are in $DICE_3$ and $DICE_5$, so only glitches will be generated. Although $DICE_1$ and $DICE_2$ are turned into incorrect logic values at this time, $DICE_4$ and $DICE_5$ are not affected, so N_8 and N_{10} still maintain correct logic values. Output Q will not be affected due to the blocking effect of five-input CE.

Finally, QNU is considered. In this case, according to the soft error tolerance methods, it can be divided into two categories: QNU self-recovery category and QNU blocking category. And then according to the number of affected nodes in each DICE, it can be subdivided into 17 types of QNU. Because of the classification of affected nodes in DICE, some of the QNU blocking category can self- recovery. The statistics for each type of the QNU are shown in the following Table 2.

Note: "☆" means that one node is upset, "☆☆" means that two nodes are upset, and so on. The black "★" represents non-shared nodes, such as nodes N_2 and N_{11} within $DICE_1$; the colored "★★★★" represents shared nodes, and the same-colored nodes represent the same node that is shared. In the first row, for example, the node N_1 is in both $DICE_1$ and $DICE_5$, so node N_1 is represented in red, and similarly, node N_3 is represented in blue.

We take the case of type 1 of QNU self-recovery for example. One DICE has four upset nodes, and another two DICEs each has one upset node. When node group $\{N_1, N_2, N_3, N_{11}\}$ are upset, CCE_2, CCE_{10}, CCE_{11}, CCE_{13} are off, CCE_1, CCE_3, CCE_{12}, and CCE_{20} are on, N_2 and N_{11} are upset. N_4 and N_{15} will only produce glitches because they are within $DICE_2$ and $DICE_5$. At the same time, since N_{10} and N_{12} still maintain the correct logic values, N_1 and N_3 can be restored to correct logic values by CCE_{10} and CCE_{13}. N_1 and N_3 then restore the N_{11} and N_2 to the correct logic values through CCE_{11} and CCE_2, in a word, QNU can self-recover in this case. Therefore, the logic value of output Q is not affected.

We take the case of type 8 of QNU blocking category for example. Three DICEs each has two upset nodes, and another two DICEs each has one upset node. When node group $\{N_1, N_3, N_5, N_7\}$ are all upset, then CCE_2, CCE_4, CCE_6, CCE_{10}, CCE_{11}, CCE_{13}, CCE_{15}, CCE_{17} are off, and CCE_1, CCE_3, CCE_5, CCE_7, CCE_{12}, CCE_{14}, CCE_{16}, CCE_{20} are on. Then $DICE_1$ (N_1, N_2, N_3, N_{11}), $DICE_2$ (N_3, N_4, N_5,

Table 2 The Statistics for Each Type of QNU

Types	$DICE_1$	$DICE_2$	$DICE_3$	$DICE_4$	$DICE_5$	Example	S/T
1	★★★★	★			★	{N_1, N_2, N_3, N_{11}}	15/15
2	★★★	★	★	★	★	{N_1, N_2, N_3, N_7}	
3	★★★	★★	★		★	{N_1, N_2, N_3, N_5}	
4	★★★	★★			★	{N_1, N_2, N_3, N_4}	
5	★★★				★★	{N_1, N_2, N_{11}, N_{15}}	
6	★★★	★	★		★	{N_1, N_2, N_3, N_6}	
7	★★★	★			★	{N_1, N_2, N_4, N_{11}}	
8	★★	★★	★★	★	★	{N_1, N_3, N_5, N_7}	
9	★★	★	★★	★	★	{N_1, N_2, N_5, N_7}	
10	★★	★★	★		★	{N_1, N_2, N_4, N_5}	723/1350
11	★★	★★			★	{N_1, N_2, N_4, N_{12}}	
12	★★	★★				{N_2, N_4, N_{11}, N_{12}}	
13	★★	★	★	★	★	{N_1, N_2, N_5, N_8}	
14	★★	★	★		★	{N_1, N_2, N_4, N_6}	
15	★★	★	★			{N_2, N_4, N_6, N_{11}}	
16	★	★	★	★	★	{N_1, N_4, N_6, N_8}	
17	★	★	★	★		{N_2, N_4, N_6, N_8}	
Total							738/1365

N_{12}) and $DICE_3$ (N_5, N_6, N_7, N_{13}) are all upset. However, N_8 and N_{15} are in $DICE_4$ and $DICE_5$, so only glitches will be generated. Although $DICE_1$, $DICE_2$ and $DICE_3$ are turned into wrong logic values at this time, and they cannot self-recovery, but $DICE_5$ is not affected, and N_{10} still maintains correct logic value. The output Q is not affected due to the blocking ability of the five-input CE. In summary, the P-DICE latch is able to tolerate QNU.

3.2 Simulation Result

The proposed latch uses the 32 nm Predictive Technology Model (PTM) [28] with a supply voltage of 0.9 V, a room temperature of 25 °C, and a clock frequency of 250 MHz for simulations. The transistors aspect ratio is set as follows: W/L = 4 for PMOS and W/L = 2 for NMOS for the TG; W/L = 2 for PMOS and W/L = 1 for NMOS for the rest of the transistors [35]. The size of the transistors is increased to enhance the driving ability of the TG, so that all latches can work normally. Synopsys HSPICE is used to simulate the proposed latch. In order to compare fairly, the transistor sizes of all latch structures compared have the identical size. We use the double exponential current source [29] of Eq. (1) to simulate the transient current caused by the incident of high-energy particles, and inject SNU, DNU, TNU and QNU into the proposed P-DICE latch. In Eq. (1), "Q" is the charge collected by high-energy particles hitting nodes. "t" is the simulation time for fault injection. "τ_1" is the collection time constant of the junction particle and "τ_2" is the ion-track establishment time constant.

$$I(t) = \frac{Q}{\tau_2 - \tau_1}(e^{-\frac{t}{\tau_2}} - e^{-\frac{t}{\tau_1}}) \quad (1)$$

Figure 5(a) shows the SNU injections performed at the proposed P-DICE latch. Due to the symmetry of the structure, SNU fault injections at nodes N_1, N_2, and N_{11} are necessary. Two types of SNU fault injections, $0 \rightarrow 1$ and $1 \rightarrow 0$, are performed at 3 ns, 7 ns, 11 ns, 15 ns, 19 ns, and 23 ns for nodes N_1, N_2, and N_{11}, respectively. As can be seen in Fig. 5(a), the P-DICE latch can self-recover from any possible SNU, so the P-DICE latch is SNU-tolerant.

Figure 5(b) shows the DNU injections at the proposed P-DICE latch, which includes six node pairs {N_1, N_2}, {N_1, N_3}, {N_1, N_4}, {N_1, N_5}, {N_1, N_6} and {N_1, N_7}. Such six node pairs can cover all the possible combinations of the DNU. DNU injections from performed at 3 ns, 7 ns, 11 ns, 15 ns, 19 ns, 23 ns, 27 ns, 31 ns, 35 ns, 39 ns, 43 ns and 47 ns. As can be seen from Fig. 5(b) that the proposed P-DICE latch can achieve 100% DNU self-recover with high reliability.

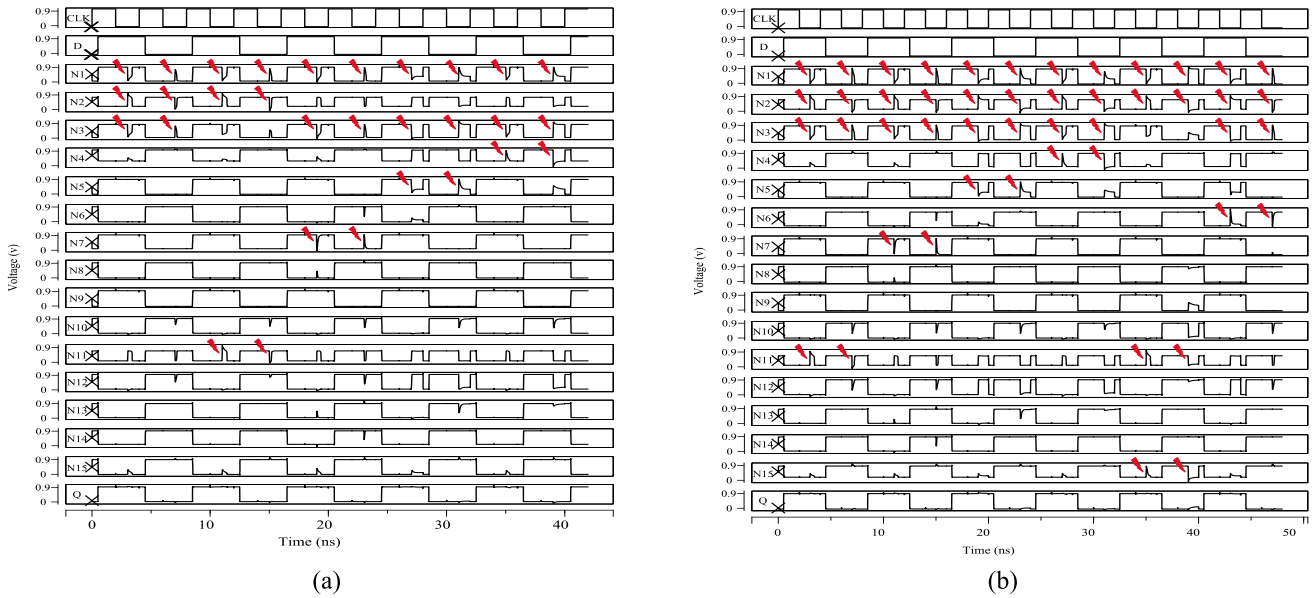

Fig. 6 **a** The results of TNU injection. **b** The results of QNU injection

Figure 6(a) shows the TNU injections of types of 1, 2, 3, 5 and 6. The fault injections are performed at 3 ns, 7 ns, 11 ns,15 ns, 19 ns, 23 ns, 27 ns, 31 ns, 35 ns, and 39 ns for the nodes of the above cases, respectively. As can be seen in Fig. 6(a), although the TNU cannot 100% self-recover with some upset nodes, the output Q still maintains the correct logic value due to the blocking ability of the five-input CE.

Figure 6(b) shows the QNU injections of types of 1, 2, 3, 5 and 6. The fault injections are performed at 3 ns, 7 ns, 11 ns, 15 ns, 19 ns, 23 ns, 27 ns, 31 ns, 35 ns, 39 ns, 43 ns and 47 ns for each of the four nodes in the above cases, respectively. As can be seen in Fig. 6(b), although most of the QNU are not self-recoverable with some upset nodes, the output Q still maintains the correct logic value due to the blocking ability of the five-input CE. Therefore, the proposed P-DICE latch can tolerate QNU.

4 Data Comparison

In order to compare the performance of the proposed hardened latch, multi-node-upset hardened latches are compared here, which are referred to as TNU-Latch, D-Latch, LCQNUSR, 4NUHL, QNUTL, QNUTL-CG, ISC-QRL, and QRHIL. To make the performance comparison fair, these latches have the same parameter settings as the proposed P-DICE latch.

Table 3 shows the comparison of the latches in terms of hardening capacity. The first column shows the latch names, including eight latches compared, and the last row shows the proposed P-DICE latch in this paper. The second column "SNU Tol." stands for SNU tolerance, i.e., the output Q is not affected after an upset occurs inside the latch, but it does not consider whether the upset node can recover. The third column "SNU Rec." means that the SNU can be

Table 3 Comparison of latch hardening capacity

Latch	SNU Tol	SNU Rec	DNU Tol	DNU Rec	TNU Tol	QNU Tol
TNU-Latch	√	100%	√	91%	√	×
D-Latch	√	82%	√	50%	√	√
LCQNUSR	√	100%	×	86%	×	×
4NUHL	√	100%	√	82%	√	√
QNUTL	√	100%	√	91%	√	√
QNUTL-CG	√	100%	√	91%	√	√
ISC-QRL	√	100%	√	100%	√	×
QRHIL	√	100%	√	100%	√	√
Proposed	√	100%	√	100%	√	√

self-recovery, that is, the upset node can be corrected to the right logic value by the feedback loop. The Table 3 shows that although most of these structures compared are tolerant of QNU, the self-recovery for SNU and DNU is not ideal. The ISC-QRL latch and QRHIL latch have high QNU self-recovery rate, with the cost of high area and power overhead.

Table 4 shows the results of the overhead comparison for the latch designs. The first column contains the names of the latches, including previous eight latches and average values, and finally the proposed P-DICE latch in this paper. The second column is the area overhead, which is estimated using the method of [30]. As can be seen from Table 4 that the QRHIL can tolerate the QNU at the cost of the highest area overhead. The proposed P-DICE latch incurs the lowest area overhead. The third column shows the propagation delay from D to Q. Since ISC-QRL and QRHIL are ring structures, it has current competition at the moment of circuit switching, resulting in a slightly higher delay. The fourth column shows the power consumption. D-latch has the lowest power consumption because of the introduction of clock-gating technology. However, the current competition can cause severe glitches at the output Q, which affects the reliability of the circuit. The proposed P-DICE latch shares internal nodes to reduce the area overhead and power consumption. The fifth column shows the comparison of the critical charge Qcrit. The Qcrit is calculated by [31]. The higher the critical charge is, the higher the reliability is. Since the proposed P-DICE latch shares five nodes, which strengthens the feedback path, it has a high critical charge. For example, when the node N_3 upset, not only the $DICE_1$ cell can recover it, but the adjacent $DICE_2$ cell can also recover it. The sixth column of the table shows the soft error rate ratio (SERR), which is calculated by the method of [32, 33] using the following Eq. (2), where $\beta = 62.5*10^{12}1/C$, and Eq. (2) is shown below:

$$SERR = \frac{\sum_{i=1}^{n} \frac{WOV_i}{T_{CK}} K_i \frac{\alpha}{\beta} e^{-\beta \bullet Q_{crit(i)}}}{\sum_{j=1}^{n} \frac{WOV_j}{T_{CK}} K_j \frac{\alpha}{\beta} e^{-\beta \bullet Q_{crit(j)}}} \quad (2)$$

SERR is normalized to the soft error rate ratio of each latch, and the SERR of the proposed P-DICE latch is 1.00 as reference. Lower SERR means higher reliability. As can be seen from the Table 4, the proposed P-DICE latch has the highest reliability. Two metrics, the APDP in column 7 and the APDSP in Column 8, were introduced in the comprehensive evaluation to evaluate the performance of the structure. The smaller the APDP and APDSP, the better the performance of the circuit, where APDP = area × power × delay [34] and APDSP = area × power × delay × SERR.

Table 4 shows that the proposed P-DICE latch are optimal in APDP and APDSP, because of the lowest area overhead, lower power consumption and fewer nodes. ISC-QRL has the largest APDP, which is mainly due to the largest delay, larger area and power consumption. QRHIL has the largest APDSP, which is mainly due to the largest number of transistors and higher power consumption. To make the comparison results more intuitive, based on the values in Table 4, we further calculated and analyzed the comparison with other latches, i.e., the relative ratio of the proposed latch to the comparison latch: △Area, △Delay, △Power, △Qcrit, △SERR, △APDP, △APDSP. Calculated through △ = (Compared latch—Proposed P-DICE latch) / Compared latch × 100%.

As shown in Table 5, the proposed P-DICE latch has a maximum improvement of 45.72% and an average improvement of 24.58% in area. In terms of delay, the maximum increase is 35.21%, with an average increase of 17.19%. For power consumption, the maximum improvement is 56.08%, and the average improvement is 33.05%. In terms of critical charge Q_{crit}, the maximum improvement is 225.21%, and the average improvement is 142.82%. In terms of SERR, the maximum improvement is 58.59%, and the average improvement is 30.08%. For APDP, the maximum improvement is 77.11% and the average improvement is 48.29%. For APDSP, the maximum improvement is 90.11% and the average improvement is

Table 4 Performance and overhead comparison

Latch	Area/10^{-2}um^2	Delay/ps	Power/uw	Q_{crit}/fC	SERR	APDP	APDSP
TNU-latch	13.82	1.69	1.51	1.25	1.02	23.36	36.22
D-Latch	17.20	1.36	0.57	1.30	1.41	13.23	18.69
LCQNUSR	14.75	1.80	0.68	1.19	1.04	17.99	18.64
4NUHL	13.82	1.36	1.78	1.75	1.31	33.30	43.72
QNUTL	11.98	1.35	1.30	1.71	1.27	21.05	26.78
QNUTL-CG	13.82	1.36	1.17	1.55	1.32	21.95	28.97
ISC-QRL	16.90	2.09	1.52	1.75	1.65	53.96	89.15
QRHIL	21.50	2.09	1.15	2.25	2.41	51.68	124.81
Average	15.47	1.64	1.17	1.59	1.43	29.57	48.37
Proposed	11.67	1.36	0.78	3.87	1.00	12.35	12.35

Table 5 Relative Changes in Performance and Overhead

Latch	△Area	△Delay	△Power	$\triangle Q_{crit}$	△SERR	△APDP	△APDSP
TNU-latch	15.56%	19.75%	32.80%	209.60%	1.96%	47.13%	65.90%
D-Latch	32.15%	-0.01%	-37.61%	197.69%	29.22%	6.63%	33.91%
LCQNUSR	20.88%	24.76%	-15.33%	225.21%	3.49%	31.35%	33.75%
4NUHL	15.56%	0.01%	56.08%	121.14%	23.82%	62.92%	71.75%
QNUTL	2.59%	-0.16%	39.88%	126.32%	21.39%	41.34%	53.89%
QNUTL-CG	15.56%	0.01%	33.37%	149.68%	24.22%	43.75%	57.37%
ISC-QRL	30.95%	35.21%	48.85%	121.14%	39.48%	77.11%	86.15%
QRHIL	45.72%	35.21%	32.06%	72.00%	58.59%	76.11%	90.11%
Average	24.58%	17.19%	33.05%	142.82%	30.08%	48.29%	61.60%

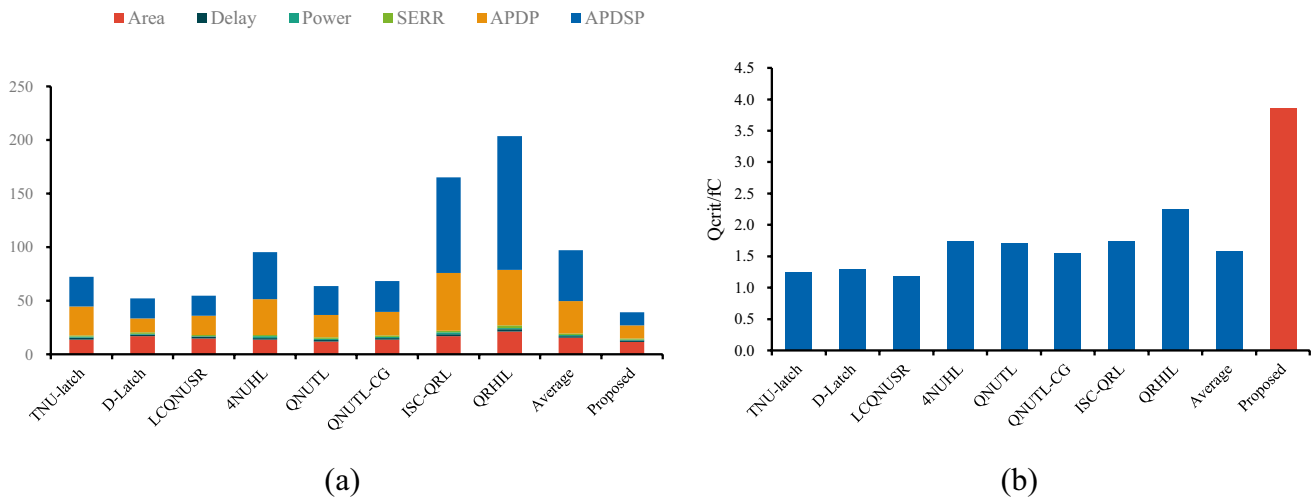

Fig. 7 Data comparison. **a** Comparison of the overhead of each latch. **b** Comparison of the critical charge of each latch

61.60%. In summary, Table 5 verifies the cost-effectiveness of the proposed P-DICE latch comprehensively.

Figure 7 shows the comparison among previous latches and the proposed P-DICE in terms of comprehensive overhead and critical charge. Figure 7(a) shows the comparison of absolute value in terms of area, delay, power, APDP and APDSP. The height of the line in the figure represents the comprehensive indicators comparison from five different perspectives, and it can be intuitively seen from the figure that the proposed latch is optimal in terms of area, APDP, and APDSP. It can be seen that P-DICE latch is also optimal in terms of the comprehensive indicators. Figure 7(b) shows the comparison in terms of critical charge Q_{crit}. The higher the critical charge is, the higher the reliability is. Compared with previous eight latches, the proposed P-DICE latch achieves the largest critical charge, with an average improvement of 142.82%. In summary, the proposed P-DICE latch achieves a good trade-off among area, delay, power consumption and radiation hardening capacity.

5 Conclusion

With the rapid development of integrated circuit technology, charge sharing induced multi-node upsets have become a serious reliability issue. In this paper, we proposed a P-DICE latch, which utilizes Cross-Coupled Elements and C-Elements to tolerate QNU. The proposed P-DICE latch is fully QNU tolerant and is capable of 100% self-recovery of SNU and DNU. Extensive simulations show that this latch has the lowest overhead in terms of area, APDP, APDSP and the largest critical charge compared to other eight hardened latches. Compared with state-of-the-art eight hardened latches, the proposed P-DICE latch is QNU tolerant and cost-effective making it suitable to high-reliability applications.

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Data Availability The datasets generated and analyzed during the current study are available from the corresponding author on reasonable request.

Declarations

Competing Interest The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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