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Editorial

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We begin 2024 by wishing well to our readers. As reported in my last editorial, the journal seems to have almost recovered from the pandemic related slowdown of previous years.

Peer reviews are an essential part of *JETTA*'s paper selection process. We thank our reviewers of 2023, whose names appear next to this editorial, for their contribution to the journal and to the profession.

The ten papers of this issue address analog circuit testing, single event upset (SEU), verification, memory testing, microfluidic device testing, printed circuit board (PCB) testing, and hardware security.

The first article discusses testing of analog circuits. An autoencoder consisting of neural networks is trained for fault diagnosis using simulation data and Fourier and wavelet packet transforms. Contributors of this work are Shang, Wei, Li, Ye, Zeng, Hu, He and Zhou from Guilin University of Electronic Technology, Guilin, China.

Next, three papers address problems of single event upsets (SEU).

The second article in this issue describes the design of a latch named P-DICE that works correctly tolerating up to four upset nodes caused by a single radiation event. It uses cross-coupled latches and a C-element, and is shown to have reduced area, power and delay compared to other available designs. Authors are Huang, Li, Sun, Liang and Yan from Hefei University of Technology, Hefei, China, and Ni from Anhui Polytechnic University, Wuhu, China.

The third article provides a design of a phased locked loop (PLL) circuit in which radiation hardening is implemented through redundancy and majority voting. Emphasis is given to controlling jitter in the operation, which is important since the PLL may be used to generate the on-chip clock signal. Authors are Yang and Huang from National Tsing Hua University, Taiwan.

The fourth article describes a design with similar objective as used in the second paper. This new high-performance quadruple-node-upset-tolerant (HQNUT) latch employes interlocked C-elements to construct feedback loops and filter errors out. It also proposes algorithm-based verification for quadruple-node-upset tolerance. Authors are Xu, Qin, Ma, Liu, Zhu and Wang from Anhui University of Science and Technology, Huainan, China, and Liang from Hefei University of Technology, Hefei, China.

The fifth article follows the theme of globally asynchronous locally synchronous (GALS) architecture, which simplifies problems of clock control in a large synchronous system. The paper presents novel strategies for design and verification. Contributors are Saranya and Rao from National Institute of Technology Karnataka, Surathkal, Mangaluru, Karnataka, India.

The sixth article, a detailed version of authors' presentation at the 2022 Latin American Test Symposium (LATS), is on memory testability. Like three earlier papers in this issue, this article also addresses radiation hardening, but for the emerging FinFET technology. The investigation identifies two critical parameters of FinFET SRAM cell that provide robustness against radiation-induced soft errors as fin height (HFIN) and number of fins (NFIN). This work is reported by a multinational team of Champac and Villacorta from National Institute for Astrophysics, Optics and Electronics, INAOE, Mexico, and Pan-American University, Mexico, Gomez-Fuentes from University of Sonora, Mexico, Vargas from IHP - Leibniz Institute for High-Performance Microelectronics, Germany, and Segura from GSE-UIB, University of Balearic Islands, Mallorca, Spain.

The seventh article focuses on a microfluidic device, also known as lab-on-a-chip, which has healthcare applications. Fluid droplets moving through tracks provide a digital behavior. This work shows how splitting and sharing of droplets can be implemented for improving the operation. The authors are Dong and X. Chen from Fuzhou University,

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Fujian, China, and Z. Chen from University of South Florida, Tampa, Florida, USA.

Then we have two papers on failures of printed circuit boards (PCBs).

The eighth article considers a case where a resistor mounted on a PCB used in an automobile. The random vibration environment is simulated by finite element analysis model that helps estimate the operational lifetime of the resistor. The contributor of this work is Huang from Chongqing Technology and Business University and Zonsen Industrial Group Co. Ltd., Chongqing, China.

The ninth article continues with the theme of PCB used in the presence of random vibrations. The study examines several types of solder joints for failures, including breaks and cracks. Authors are Yu, Dai and Li from Central South University, Changsha, China.

The tenth article is about hardware security. A formal verification approach is proposed for detecting hardware Trojan. First a Trojan-free design is described in RTL, such as Verilog or VHDL, and the function is expressed as assertions using SystemVerilog Assertion (SVA) language. A model checker then verifies the assertions. Next, Trojans are inserted in the RTL description to ascertain that the model checker fails some assertions. Authors are Ibrahim, Haytham, El-Kharashi and Safar from Ain Shams University, Cairo, Egypt, and Azmi from Electronics Research Institute, Cairo, Egypt.