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Effect of Sizing and Scaling on Power Dissipation and Resilience of an RHBD SRAM Circuit

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Abstract

Single Event Transients (SET) pose a growing challenge to reliability of memory circuits as the device dimensions continue to shrink. It is essential to assess the effect of decreasing technology lengths on the resilience and power dissipation of the circuit. This paper proposes Dual Interlocked Storage Cell (DICE) based Radiation Hardened by Design (RHBD) Static Random Access Memory (SRAM) circuit design with appropriate sizing ratios for 180 nm, 90 nm and 45 nm channel lengths. The effect of variation in voltage in these technology nodes is analysed by a comparison of power dissipation calculated through simulations on Cadence. For an input voltage of 1.1 V, the power dissipation is calculated as 0.175nW for 180 nm technology length, 0.086nW for 90 nm technology length and 0.018nW for 45 nm technology length. It shows that the power dissipation gets almost halved when the technology switch is made from 180 nm to 90 nm and the power dissipation decrease is almost ten times from 180 nm to 45 nm technology. Mobility and doping parameters are found to be varying with device dimensions and the magnitude of that variation is studied. The parameters are related with the vulnerability to SET and affect the circuit's resilience to radiation.

Keywords Radiation Hardening by Design (RHBD) · Dual Interlocked Storage Cell (DICE) · Singe Event Transient (SET) · Single Event Upset (SEU) · Static Random Access Memory (SRAM) · Technology Length · Transistor Sizing · Power Dissipation

1 Introduction

Caches and other on-chip memories require extremely rapid access times while also being simple to implement. Both of these objectives are satisfied by SRAM. In today's SoCs (System on Chips), microprocessors and microcontrollers, memory arrays have become extremely important. For any specific application, there are many factors that have to be considered such as need of memory size, access time of the data stored, access patterns and other system requirements. Memory size can be specified in terms of number of words or bits or bytes or the number of flip flops or registers needed for data storage.

Cache devices account for over half of all devices utilised in the design, and this percentage is expected to expand as microprocessor architecture improves. In SRAMs, the cache takes up a significant amount of space dedicated to its own design. Because of their low power consumption and quick data access, static RAMs have dominated the market in recent years, and they are now successfully used in the majority of digital applications. The static RAM, on the other hand, has an impact on the SoC's absolute power. Memory systems take up a lot more space on SoCs, and they also contribute a lot to the rising power consumption. The logic circuits and memory blocks are highly vulnerable to soft errors. Single Event Effects continue to be serious problem for more than five decades now which has caused financial losses in both space and terrestrial IC systems. A large body of research work has been actively devoted to fault tolerance in Very Large Scale Integration (VLSI) circuits because of the rising

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Table 1 Technology Scaling trend during 1978–2018 [3, 4]

Year	Device feature size (nm)	Year	Device feature size (nm)	Year	Device feature size (nm)
1978	3000	1995	350	2007	45
1984	1500	1999	180	2012	22
1990	800	2003	90	2018	9

dependability concerns. Classically, technological fault prevention methods or fault detection and recovery approaches have been used to prevent faults resulting from variabilities in manufacturing, aging and wear out. For very demanding applications, replication-based fault tolerant methods like dual or triple modular redundancy (DMR, TMR) have also been implemented. SRAM cell has a range of delicate parts per bit which makes it sensitive to soft errors. There is a rapid increase in soft errors in the nanometer regime due to the growth of technology [1, 2].

Earlier, the Complementary Metal Oxide Semiconductor (CMOS) technologies used for Integrated Circuit (IC) fabrication had larger diffusion node sized which made them inherently resilient to radiation events. The radiation strikes were unable to accumulate enough charge to upset the cells because the dimensions of the diffusion nodes were relatively large. But now, even a low energy strike can generate enough charge to upset the cell and corrupt the data stored in it because of technology scaling. The advancing process technologies result in increasing speeds in microprocessors and large scale integrated circuits (LSIs). SRAMs that serve as cache memories also need to keep up with these increases.

Table 1 shows the evolution of lower technology nodes. A scanning electron microscope (SEM) can be used to determine the physical length of a gate. In the fabrication plant, it is meticulously monitored.

In 1965, Gordon Moore anticipated that the number of components per chip will increase by a factor of two per year [5]. The goal of adhering to this law was to lower the cost of each component as well as the amount of electricity utilised by each component. Moore revised his prior prediction in 1975, predicting that the number of components per chip will double every two years due to a combination of component size scaling and chip area growth [6]. In 1974, Robert Dennard and colleagues proposed a methodology for scaling in Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) to deliver consistent improvements in circuit parameters such as transistor area, performance and power reduction [7]. The gate length, gate width, gate oxide thickness, and supply voltage of the transistor were all scaled by the same factor, and channel doping was increased by the inverse of the same scaling factor. This would result in transistors with a smaller area, higher driving current, and lower parasitic capacitance, all of which would contribute to lower active power. This method of scaling MOSFET transistors is commonly referred to as classic or traditional scaling. Until the release of the 130-nm generation in the early 2000s, it was widely used in the industry.

The last two decades have seen the emergence of new generations of process technologies in every two years. The upcoming generations come with an increase of about 0.7 times in the minimum feature size and 0.5 times increase in area scaling. So, the transistor density has been doubling every two years. For each new technology generation, scaling the minimum feature size, length, and width by around 30% (also known as Moore's magic number) potentially yields the following:

- Doubles device density while reducing area by (0.7*Y0.7*X) 50%, substantially lowering the cost per transistor by putting in more devices in the same area.
- Reduces total capacitance by 30%, which allows gate delays to be reduced by 30%, resulting in a 43% increase in operating speed.
- As a result of smaller transistors and lower supply voltage, power consumption (Power CV^2f) should drop by 30–65% for a given circuit [8].

Technology generations include 0.18 m, 0.13 m, 90 nm, 65 nm, 45 nm, and so on. The numbers represent the minimum width of a metal line. The length of a Poly-Si gate could be shorter. The different circuit architecture features, such as the size of contact holes, are 70% larger with each subsequent node than they were at the prior node.

Moore's magic number can be used to calculate the next generation technological node. For example, if the current technology node is 65 nm, then the next technology node will be (65*0.7) = 45 nm. All other technology nodes have been derived in the same way [9, 10]. The probability of one particle upset affecting more than a single SRAM cell increases dramatically for sub-130 nm CMOS technologies.

Although a lot of research work has been done on radiation hardened SRAM cells and sizing of SRAM, the novelty of the present article resides in the fact that we have proposed a quite new research problem to reduce the power dissipation of the memory circuit based on variation in sizing. We have studied the change in mobility and doping parameters for both NMOS and PMOS with scaling. The product µN and its relationship with collection current and rise time can be used to study the resilience to soft errors. The results presented in this article will prove useful to researchers working on Process Design Kit development.

Section 2 discusses the effect of change in sizing with decreasing technology lengths and proposes some models based on that. Section 3 is about the variation in power

Table 2 Proposed models showing transistor sizing with minimum power dissipation for 180 nm, 90 nm and 45 nm

Model	Transistor	Aspect Ratio (W/L)	W_p/W_n	CellRatio
Model 1	P1, P2, P3, P4	230 nm/180nm = 1.277	0.766	1.811
	N1, N2, N3, N4	300 nm/180nm = 1.666		
	Access Transistors	230 nm/250nm = 0.92		
Model 2	P1, P2, P3, P4	605 nm/360nm = 1.68	1.374	0.524
	N1, N2, N3, N4	220 nm/180nm = 1.222		
	Access Transistors	420 nm/180nm = 2.333		
Model 3	All Transistors	240 nm/100nm = 2.4	1	1
Model 4	All Transistors	220 nm/100nm = 2.2	1	1
Model 5	All Transistors	120 nm/100nm = 1.2	1	1
Model 6	PMOS	180 nm/90nm = 2	3	0.25
	NMOS	120 nm/180nm = 0.67		
	Access	120 nm/45nm = 2.67		
Model 7	PMOS	140 nm/45nm = 3.1	2.59	0.449
	NMOS	120 nm/100nm = 1.2		
	Access	120 nm/45nm = 2.67		
Model 8	PMOS	151.25 nm/90nm = 1.68	1.38	0.61
	NMOS	55 nm/45nm = 1.22		
	Access	90 nm/45nm = 2		

dissipation at different voltage supply and technology node. Section 4 discusses the simulation results along with graphical representations and the effect of doping and mobility on the Soft Error Rate of the circuit followed by conclusion.

2 Sizing Ratios for Diminishing Technology Lengths

When the size of transistors in a VLSI circuit is increased, the delay through the circuit and the circuit's area are also increased. While transistor area makes up a modest percentage of total chip space, this is because transistor sizes are usually reasonable. Large transistors can be used to reduce latency, however larger transistors actually increase delay beyond a certain threshold.

Radiation hardening by design conventionally have a lot of power dissipation due to high leakage currents in the N-channel metal oxide semiconductor (NMOS) and P-channel Metal Oxide Semiconductor (PMOS) involved in inverter which are a part of the redundant circuitry or feedback circuitry. Also, there are critical sizing ratio constraints for the circuit to operate properly and make the memory cell immune to upsets [11]. DICE based design is chosen in the current work as it has an advantage that it does not

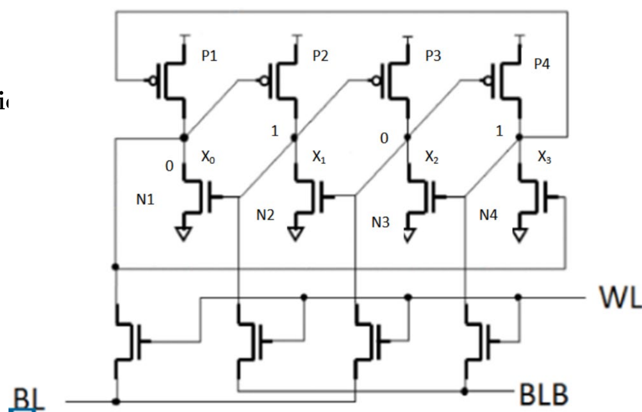

Fig. 1 Schematic of the DICE-based SRAM cell with (0101) stored initially

necessitate an increase in transistor size or in the capacitance of some nodes. The other transistors in the DICE cell can drive the single node that is afflicted by a transient fault back to its previous state.

The schematic of the implemented design is shown in Fig. 1. The circuitry makes use of twelve transistors instead of six to ensure resilience to single event upsets due to radiations. If any of the sensitive nodes in the circuit gets struck by an upset, the bit will be restored and only the original bit will be passed on.

The sizing ratios are varied to find out the best option of a design that gives performance as well as reduced power dissipation. The ratios vary with technology length and the widths and lengths chosen in a particular technology are summarized in Table 2. Cell Ratio is also given for all the proposed models since it is a measure of Static Noise Margin. A higher Cell ratio leads to a good Static Noise Margin. Power dissipation also varies with change in the lengths and widths of operating transistors.

The DICE based memory circuit makes use of redundancy to implement self-restoring logic. It uses double the circuitry in 6T SRAM in order to make the circuit immune to radiations. It has the capability to recover from any SEU that the circuit is exposed to unlike the standard SRAM cell. The schematic of the implemented design is shown in Fig. 1.

The ratio of width to length of the transistor, also referred to as Aspect ratio is varied keeping the cell ratio and pull up ratio constraints in mind so that the read and write functionality, respectively, are not disturbed. The ratio of the width of PMOS transistor to the width of the NMOS transistor (W_p/W_n) are also taken into account as this ratio should ideally be greater than one to get balanced rise and fall times during CMOS operation. Although exceptions may be made where area or power requirements suffer.

The transient output waveform for Model 2 is shown in Fig. 2 below.

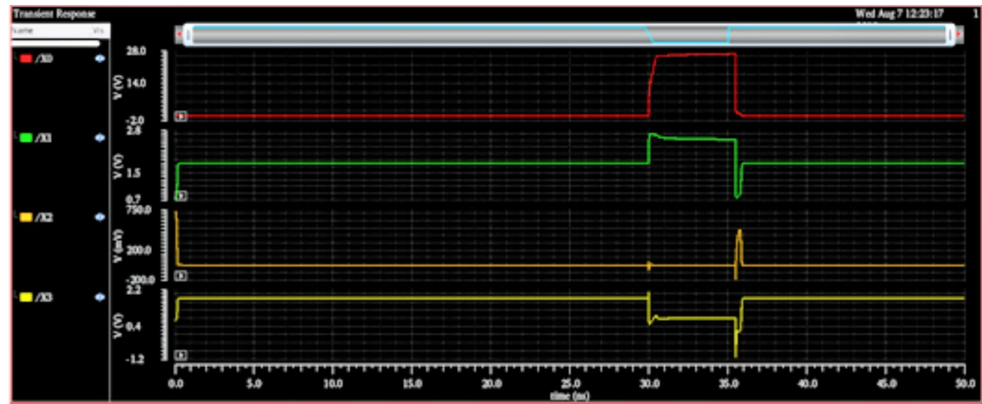

Fig. 2 Model 2 output: Behavior when amplitude of impulse is such that X_3 is able to recover from the effect of impulse at X_0 while 0 is stored at X_0 and 1 at X_3

The proposed Radiation hardened by design DICE cell has been implemented on various technology lengths as 180 nm, 90 nm and 45 nm with appropriate aspect ratios that assume circuit functionality. Process variation in sub-100 nm technology influences stability as well as other parameters of an SRAM cell [12–14].

3 Variation in Average Power

Power losses in VLSI circuits are an important concern today. SRAM is an indispensable part in most of the circuits and consumes a significant percentage of total power dissipation on a digital chip. Transistor sizing helps ensure the proper functionality of a circuit at the lowermost operating voltage. This optimization in the sizing of the SRAM is done so that area is not compromised because of the use of extra circuitry needed to achieve low power design. At both the circuit and microarchitectural design levels, variability considerations should be kept in mind to keep up with performance scaling and to ensure that the power consumption is within reasonable range. In addition to line width, scaling reduces other parameters such as MOSFET gate oxide thickness and power supply voltage. Historically, the speed of integrated circuits has increased by about 30% with each successive technology node. With advancement in technology node, the switching frequency, f, keeps on rising and the number of transistors per chip get doubled but power consumption per chip has only increased minimally in every node due to the drop in capacitance (C) and V_{dd}.

As technology advances, the impact of within-die random variants (as opposed to systematic variations) is growing. Furthermore, as the number of pipeline stages grows (and thus the number of logic levels per step decreases), random changes account for a bigger share of fmax loss. For variability tolerance, these facts indicate to the need of a microarchitecture with shorter pipelines. These seemingly contradicting findings highlight the importance of rigorous, variability-aware design.

Supply voltage scaling has resulted from the requirement for minimal power dissipation. V_{DD} is defined at two levels: maximum V_{DD} is used as a process's dependability limit, and lowest V_{DD} is used to define the target performance. Variations in transistor leakage current due to manufacturing and temperature variables as well as differences in active current demand across the die induce supply voltage shifts. The processor's running frequency is limited by these voltage changes, which increase temperature hot spots. For example, a 10% V_{DD} change can result in a delay of up to 20%. The voltage variations that are done in this work refrain from going into subthreshold values as that has a negative impact on the circuit. One of the major limitations is that with the decrease in supply voltage, delay in the SRAM circuit increases at a much higher rate than it does in the case of CMOS logic delay. Another important factor is that the data stored in SRAM cells get destroyed very often when the read operation is carried out at low voltages. Also, the chances of the occurrence of a failure during write operation are higher at lower operating voltages [15, 16]. The critical charge also rapidly decreases if V_{DD} is reduced with generation advancement, leading to an increase in the SER (Soft Error Rate) [17]. The critical charge for the proposed DICE cell is calculated as 59.5fC for the proposed Model 2 shown in Table 2 at 180 nm technology length.

4 Experimental Results

The performance of the DICE circuit implemented shows a declining trend with decreasing technology length of the MOS transistors used. The rate of occurrence of the Single Event Upsets also shows a rise at lower technology lengths. This has been verified through experimental implementation in earlier works as well [18]. All the simulations have been carried out on Cadence Virtuoso. Simulations were carried out for 180 nm, 90 nm and 45 nm technology nodes.

A double exponential current pulse denotes the physical phenomenon that is taking place whenever an SEU occurs

Table 3 Variation in power dissipation with technology scaling and voltage scaling

Voltage (V)	Power Dissipation at 180 nm for proposed Model 2 (nW)	Power Dissipation at 90 nm for proposed Model 4 (nW)	Power Dissipation at 45 nm for proposed Model 7 (nW)
3.3	1.052	0.76	0.1875
1.98	0.804	0.65	0.162
1.8	0.634	0.53	0.154
1.62	0.284	0.253	0.146
1.1	0.175	0.086	0.018

at a sensitive node. It has a rapid rise time and gradual fall time. Mathematically, the current pulse can be expressed in terms of the charge deposited at the struck node as well as the rise time and fall time of the current pulse as follows:

$$I(t) = \frac{Q}{\tau_\alpha - \tau_\beta}(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}) \quad (1)$$

where, I(t) denotes the transient current waveform, Q denotes the charge deposition, τ_α is the fall time of current pulse, and τ_β is the rise time.

A double exponential current source with varying magnitude ranging from 0.5μA to 1.15 A has been used to simulate the single event upset in the designed circuit. The effect of change in doping and mobility on the resilience of the circuit is analysed. The power dissipation calculations at decreasing operating voltages with scaling in technology length for the proposed models is shown in Table 3.

The proposed Model 2, Model 4 and Model 7 have been chosen to compare the power dissipation at 180 nm, 90 nm and 45 nm technology nodes respectively. Although the decrease in power dissipation with technology scaling is a previously established result, Table 3 confirms that the radiation hardened cell also follows the results of a CMOS cell. Figure 3 shows the variation in power dissipation with change in voltage and technology scaling. A similar earlier work that has considered the mobility difference in NMOS and PMOS devices has used the design rule so as to achieve minimum area. They have proposed a radiation hardened by design latch at 45 nm technology node [19]. Their widths have been chosen as 150 nm and 120 nm for PMOS and NMOS respectively which is comparable to our proposed models. They have used a current source of magnitude 80μA whereas our proposed work has used higher magnitude currents to simulate upset in the circuit. The power dissipation of their proposed circuit lies in the range of 377.9nW to 551.2nW.

Static Noise Margin is another important consideration related to stability of any memory cell [20]. The Read Static Noise Margin of the proposed Model 7 at 45 nm calculated at 1.1 V is calculated as 140mV and the Write Static Noise Margin came out to be 226mV. The write access time of the proposed DICE SRAM cell at 1.1 V for 45 nm comes out to be 644ps. The operating frequency of the cell is quite high approximately 14.28 GHz but it will be affected with the increase in memory capacity.

The impact of SET on any design varies with many factors including change in technology length [21]. Charge collection current and time constant are two important variables that depend on the energy of the striking particle and are crucial for determining the effect of SET at any stage. Whenever a particle with some specified energy strikes at a sensitive node in a digital circuit of a particular technology, the values of collection current and time constants for other technologies can be estimated for a particle collision with the same technology. Equations (2) and (3) represent the relation between I_0 and τ_α with other device parameters for a bulk CMOS transistor.

$$I_0 = q\mu N E_0 \quad (2)$$

$$\tau_\alpha = \frac{\mathrm{k}\varepsilon 0}{\mathrm{q}\mu\mathrm{N}} \quad (3)$$

where N is the rate of generation of electron-hole pairs proportional to the doping concentration, μ is the effective mobility, q is the electron charge, E_0 is the critical electric field and $k(\epsilon_0)$ is the substrate dielectric constant. Table 4 represents the change in device parameters with changing technology length for Cadence based simulations.

As sizing of PMOS transistors has greater effect on circuit performance compared to NMOS transistors, so the product μN for PMOS transistors is of prime consideration. With the decrease in technology length, the product decreases as shown in Fig. 4(b).

The number of dopant atoms has dropped with scaling, and the effective channel currently has hundreds of them. As it is impossible to uniformly deposit the same small number of dopant atoms across billions of transistors on a die, dopant concentration is becoming a major determinant of device variability.

Variations are present in every individual component and the characteristics of the circuit vary because of sum of the variations of components. Monte Carlo simulations have been carried out for different number of runs using Cadence Spectre at 180nm technology and the results are presented in Table 5. The power dissipation of DICE circuit is simulated for various process corners such as nominal (NN), fast slow (FS), slow fast (SF), fast fast (FF) and slow slow (SS)

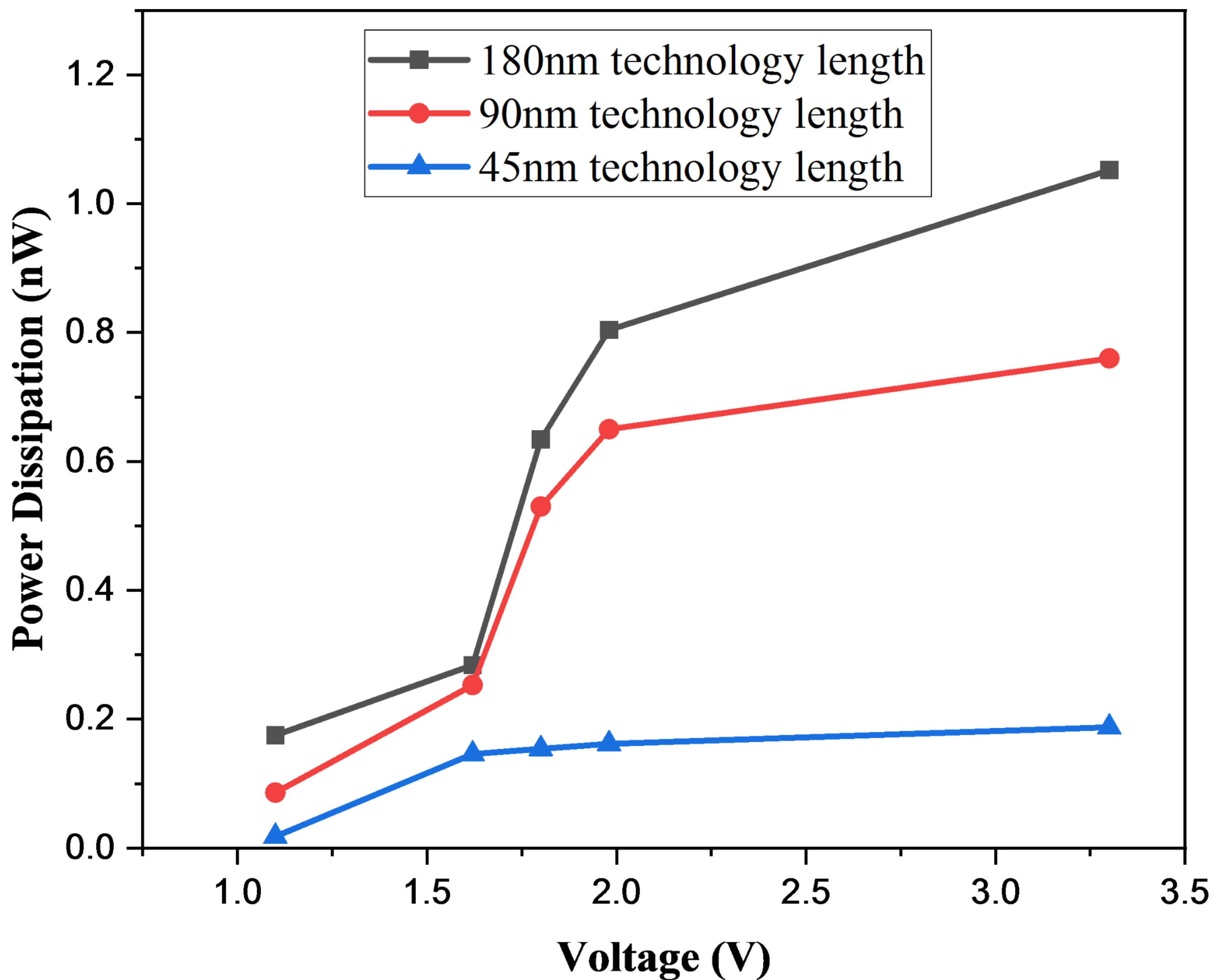

Fig. 3 Variation in power dissipation with change in voltage and technology scaling

Table 4 Change in device parameters as technology scales for computing SET parameters

Technology (nm)	V_{DD} (V)	Doping (μ) (cm^{-3})		Mobility (N) (m^2/V.s)		μN	μN
		PMOS	NMOS	PMOS	NMOS	PMOS	NMOS
180	1.8 V	3.9×10^{17}	3.9×10^{17}	0.0063	0.04	2.4×10^{15}	15.6×10^{15}
90	1.2 V	4×10^{17}	5.2×10^{17}	0.012	0.02	4.8×10^{15}	10.4×10^{15}
45	1 V	3.6×10^{17}	5.72×10^{17}	0.0156	0.026	5.6×10^{15}	14.8×10^{15}

for supply voltages varying in the range of ± 10% of V_{DD}. The temperature variation range is kept from 0^0 C to 100^0 C for testing memory circuits.

Miniaturization has been the fundamental engine driving the advancement of electronics. By shrinking transistors and interconnects, more circuits may be produced on each silicon wafer, lowering the cost of each circuit. Improvements in speed and power consumption have also been aided by miniaturization. Still, increased unpredictability in emerging process technology has a significant financial impact. As evident from Table 4, the product μN decreases with reduction in technology length. From Eqs. 2 and 3, it can be clearly seen that the collection current is directly proportional and rise time is inversely proportional to μN. It suggests the value of I_0 decreases and that of τ_α decreases for lower technology nodes. It means that the circuit at lower technology nodes is resilient to lesser amplitude of collection currents with longer rise times. So, the level of resilience drops down with technology scaling.

An application specific tradeoff has to be made between the radiation resilience level of the circuit and the circuit miniaturization. There are numerous applications from the

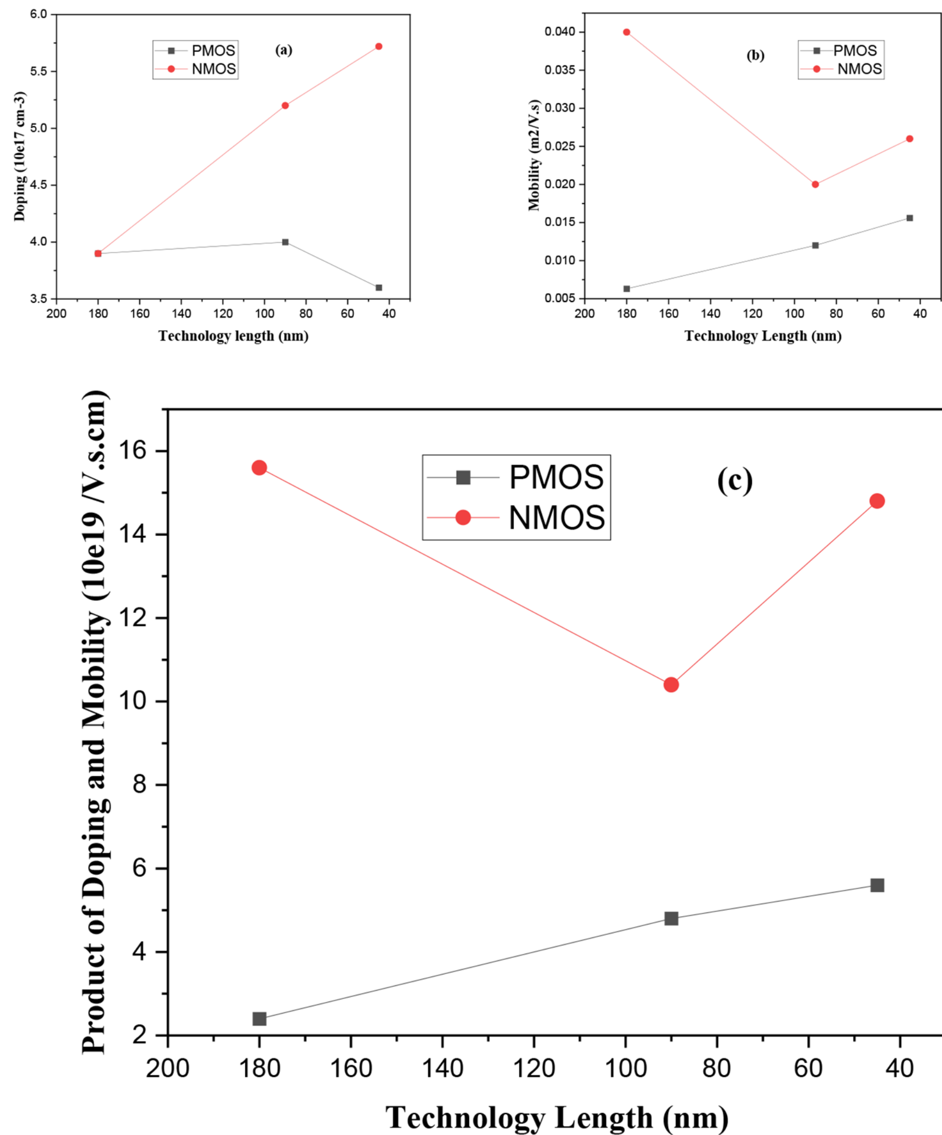

Fig. 4 Effect of technology scaling on (a) Doping of NMOS and PMOS transitors (b) Mobility of NMOS and PMOS transistors (c) μN, which is an important parameter in testing for SET

Table 5 Power dissipation in proposed DICE circuit under PVT (Process Voltage Temperature) variations

Parameter		Power Dissipation
Supply Variation	1.62 V	284.9pW
	1.8 V	343.2pW
	1.98 V	408.3pW
Process Variation (for 1000 samples at 85^0 C)	SS	124.1nW
	NN	125nW
	FS	132.9nW
	FF	134.8nW
	SF	135.6nW
Temperature Variation	$0\,^0$ C	343.2pW
	27^0 C	1.052nW
	85^0 C	124nW
	100^0 C	695.4nW

field of automation to space based devices and also portable devices in biomedical concerns. With the use of small and succinct sensors linked to the body, rapid technological breakthroughs have made it feasible to continuously monitor a patient's health. Blood pressure and oxygen levels in the human body can be detected through these biomedical sensors [22].

5 Conclusion

With increasing miniaturization, there is a change in device parameters such as threshold voltage, transistor channel length and transistor width. There are constraints on varying the sizing ratios of the transistors in order to ensure appropriate functionality of an SRAM circuit. A radiation resilient memory design has been proposed and simulated on

180 nm, 90 nm and 45 nm technology lengths with optimum sizing ratios to achieve low power design parameter. The minimum operating voltage varies with change in technology node. Power dissipation is observed to show a decreasing trend with technology scaling which is advantageous but on the other hand, the doping and mobility parameters lead to a decrease in circuit's radiation resilience. Doping shows an increase with scaling in technology whereas mobility shows a decrease. The collection current and rise time are affected resulting in change in device resilience.

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Data Availability This manuscript has no associated data.

Declarations

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