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Novel Fault-Tolerant Processing in Memory Cell in Ternary Quantum-Dot Cellular Automata

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Abstract
Processing-in-memory (PIM) is a computational architecture in which the processing unit and memory are integrated into a single unit. Different technologies and methods can be used to implement PIM, but a more optimal design for PIM can be obtained by using quantum-dot cellular automata (QCA) and Akers structure. In the chemical manufacturing process of such circuits, the manufacturing defects and therefore malfunction are possible. One of the most common defects is cell omission, which has not yet been investigated in PIM based on binary or ternary QCA. One of the aims of this study is to improve fault tolerance (FT) by transforming the circuit structure from binary to ternary QCA. The results of evaluating different structures confirm achieving this aim. Moreover, in this study, new basic PIM cells are proposed, and then, AND, OR, and Exclusive-OR (XOR) gates are designed based on these cells in ternary quantum-dot cellular automata (TQCA). The ternary structure is used to improve circuit performance, storage density, and processing capability. For better analysis and comparison, binary structures are also implemented. The results of the evaluations show that the proposed ternary structures are efficient in terms of occupied area, latency, cost, FT, and complexity, as well as better efficiency in processing and storing data because of the three-valued structure.

Keywords Fault tolerance · Ternary · QCA · Akers array · XOR · PIM

1 Introduction

Data processing and machine learning are two applications of processing-in-memory (PIM). Unlike the typical von Neumann architecture, a PIM architecture uses an integrated circuit for both storing and processing data [1, 2]. Therefore, PIM seems to be much more efficient in terms of area occupation, speed, etc. Several articles have presented different methods for implementing PIM architectures [3, 4]. Figure 1 shows the structure of von Neumann and PIM.

Downscaling in CMOS technology has caused some issues, such as high leakage current and thermal loss [5, 6]. A more efficient design for PIM can be provided using the Akers structure in quantum-dot cellular automata (QCA) [7], which is a nanoscale technology [8–10].

Multi-valued circuits have many advantages, such as increased computational speed, reduced number of inputs/outputs, and lower costs. Ternary logic is a type of multi-valued logic [11]. Several articles have used binary QCA (BQCA) to design PIM architectures, but ternary QCA (TQCA) has not been used in this area before.

In [12], BQCA circuits are employed in a processor. This reference uses an innovative algorithm to describe the proposed structures. Reference [13] proposes a new method for designing complex ternary functions. In [14], BQCA is used to realize XOR, XNOR, Toffoli, and CNOT gates. In [15], some ternary gates are designed. In another model proposed in [16], a memorizing cell is designed using a ternary structure. In [17], one memory architecture is presented. An optimal TQCA logic circuit is presented in [18] to compute an arbitrary ternary logic function. The XOR gate execution with Akers array and BQCA is suggested in [19]. In this design, a PIM architecture is built using a BQCA multiplexer. The latency of the design is 4.75 clock cycles and the occupied area is 0.23 μm2. In [7], NAND and NOR are implemented using Akers array, and QCA is used to design the PIM architecture. Moreover, the cell count of both

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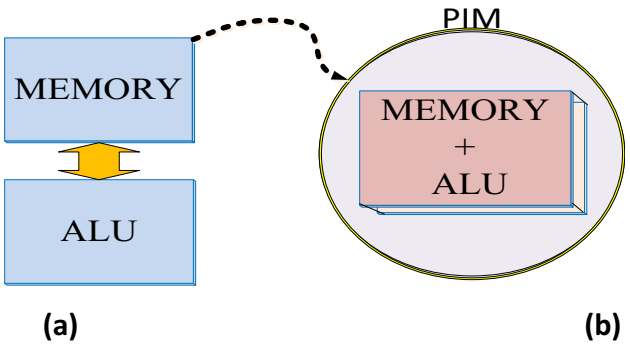


Fig. 1 **a** von Neumann and **b** PIM architectures

NAND and NOR gates is 147 and the occupied areas are 0.31 μm2 and 0.34 μm2, respectively. Some improvements are considered in the design of the PIM architecture, such as higher speed, lower energy consumption, and smaller occupied area.

There is also a possibility of defect in the manufacturing process of QCA circuits. One type of manufacturing defects is cell omission. There are several ways to increase fault tolerance (FT) in QCA circuits. In [20], with increasing number of binary cells, the circuits become more resistant to defects, but this approach increases the cell count, area occupation, and latency. In this study, we reduce the fault effect by transforming the circuit structure from binary to ternary, without significantly increasing the number of cells, latency, and occupied area.

In our previous work [21], we designed and examined a PIM architecture in ternary logic, and then, we proposed larger gates. Also, the effect of using optimal gates in optimizing the design of PIM structures was investigated. In this paper, other gates such as: XOR, AND, OR with a new proposed structure for ternary PIM are designed and simulated. Also, the effect of changing memory location, on circuit optimization, and the effect of changing the structure from binary to ternary on fault tolerance were investigated.

This study presents a novel basic PIM computing approach using flip-flop and Akers array with BQCA and TQCA structures. At first, the new basic PIM cells are proposed. Then, AND, OR, and XOR gates are designed with the proposed basic cells in BQCA and TQCA. Because the PIM architecture consists of two parts, i.e., memory and multiplexer, the effects of memory displacement on PIM architecture for basic cells and gates are investigated and compared. Finally, the fault tolerance and energy consumption of the basic cells are evaluated.

The differences between this article and the previous one [21] include the following:

1. In this manuscript, new structures are proposed for PIM in binary and ternary QCA.
2. Memory blocks are placed at the beginning and end of the circuit, and then its behavior is studied.
3. The effect of the fault is investigated for the first time for the structure of PIM in ternary QCA.
4. We observe that ternary QCA architecture are inherently more fault-tolerant than its binary counterpart.
5. The energy consumed in new primary cells has been calculated.

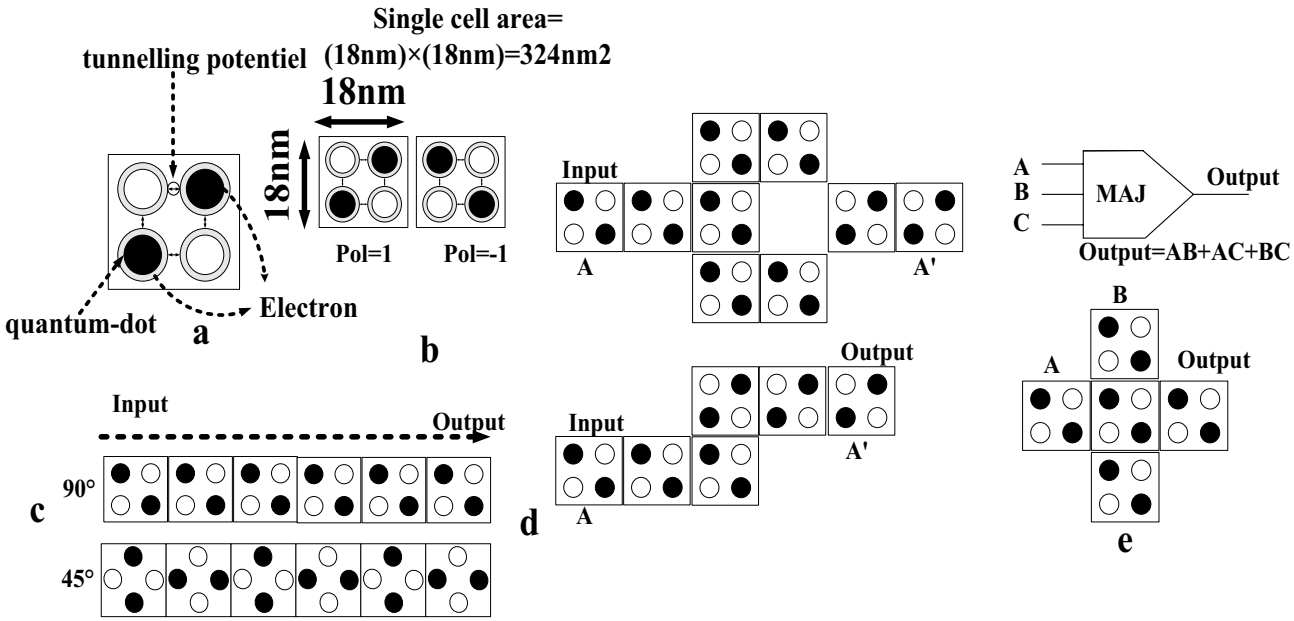


Fig. 2 BQCA cell structures; **a** QCA cell, **b** polarization and dimensions, **c** wire (90° and 45°), **d** inverter gate, and **e** majority gate

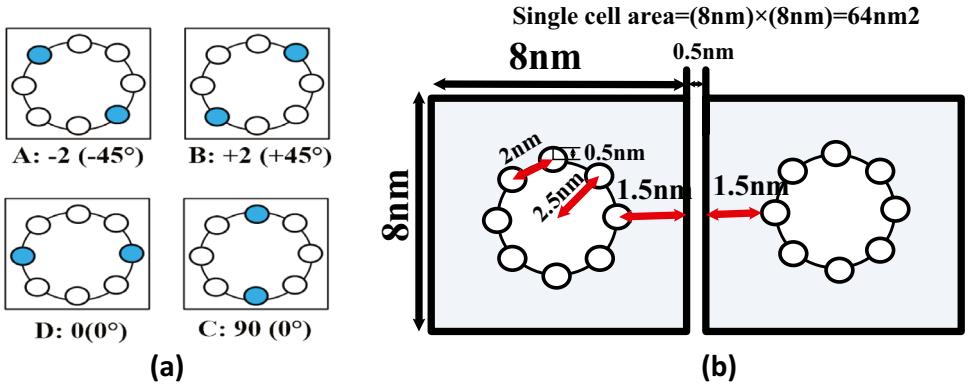


Fig. 3 **a** Four possible TQCA cell configurations and **b** TQCA cell dimensions [29]

6. In this article, new gates such as AND, OR and XOR with processing-in-memory capability have been designed and analyzed, in contrast to previous study [21].

The rest of this article is organized as follows: Sect. 2 provides an overview of BQCA, TQCA, and Akers array. In Sect. 3, the proposed structures of basic cells in BQCA and TQCA are presented. The proposed AND, OR, and XOR structures are presented in Sect. 4. In Sect. 5, the effect of missing cell defect and additional cell deposition are studied. the fault tolerance, and in Sect. 6, the energy consumption is analyzed. The conclusion is presented in Sect. 7.

2 Background Details

This section describes the performance of QCA and the basic structure of Akers array.

2.1 Binary QCA

QCA exploits Coulombic interactions instead of electric current. Electrons represent polarization states P = + 1 and P = -1, which correspond to logic '1' and '0' (Fig. 2a and b).

Figure 2b shows the dimensions of the cell. The implementations of wire, NOT, and majority gates in the BQCA structure are shown in Fig. 2c, d, and e, respectively. Using clock control in QCA, data transfer performance can be controlled. A QCA clock consists of four phases, i.e., switch, hold, release, and relax. In the switch phase, barriers are raised and electronic tunneling occurs. In the hold phase, barriers are held high and each cell is in a state of polarization. In the release phase, the barriers are lowered and electrons are released slowly. In the relax phase, the barriers are reduced and the electrons move freely [22]. In general, QCA implementations can be categorized as follows: molecular structure [23], metal structure [24], magnetic structure [25, 26], and semiconductor structure [27].

2.2 Ternary QCA

Ternary logic has many applications [28]. Bajec et al. introduce a ternary model for QCA [15]. The proposed TQCA cell consists of two electrons and eight quantum dots. In the design of ternary logic gates, four configurations represent a logic state [11]. D-state occurs only inside a cell and is not seen at the output. Ternary logic gates proposed in [11] can be used to design larger circuits. The ternary gates are simulated using TQCA-sim software, which is used to design basic gates.

The QCA research team at the University of Central Tehran [29] decided to solve the problems encountered in Ref. [11], so the simulator software was rewritten from scratch with new dimensions for ternary cells and the algorithm and its program size were optimized. The new optimized dimensions are shown in Fig. 3b.

In the new design proposed in [29], TQCA cells have four polarizations with values A: -2 (- 45), B: 2 (+ 45), C: 0 (+ 90), and D: 0 (0). Using QCA Sim-Ternary Edition simulator software originally introduced in Ref. [29], the ternary simulations are performed in the present study. States C and D have values of '0'. Ternary wire and inverter are shown in Fig. 4a and b. Majority gates have many applications; if one input is equal to A, the majority gate functions as an AND

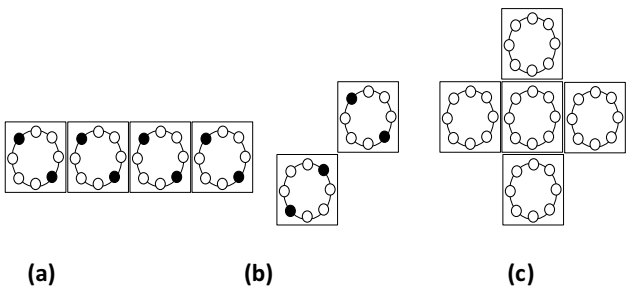


Fig. 4 **a** ternary wire, **b** ternary inverter, and **c** ternary majority gate [29]

Table 1 Ternary majority truth table [29]

INPUT1	INPUT2	INPUT3	OUTPUT
A	A	A	A
C	A	A	A
B	A	A	A
A	C	A	A
C	C	A	C
B	C	A	C
A	B	A	A
C	B	A	C
B	B	A	B
A	A	C	A
C	A	C	C
B	A	C	C
A	C	C	C
C	C	C	C
B	C	C	C
A	B	C	C
C	B	C	C
B	B	C	B
A	A	B	A
C	A	B	C
B	A	B	B
A	C	B	C
C	C	B	C
B	C	B	B
A	B	B	B
C	B	B	B
B	B	B	B

gate and if one input is equal to B, it functions as an OR gate. The majority gate is shown in Fig. 4c, and Table 1 shows the gate outputs for the applied inputs.

2.3 Akers Array

Akers logic array can be used for computing in memory. It was introduced by S. B. Akers in 1972. Figure 5 shows a 2×2 array of logic cells, which operate based on Eq. (1) [19] and [30]:

$$f1(X, Y, Z) = X\overline{Z} + YZ \tag{1}$$

Equation (1) is one of the four proposed Akers equations, which is used in this study to design a PIM architecture. In the Akers logic array structure, a basic cell has inputs 'X', 'Y', and 'Z', and one output 'F'. This output acts as the input to the next cells as shown in Fig. 5. Here, 'X' and 'Y' are binary or ternary inputs, and 'Z' is the control input. One of the outputs of each cell is given to the bottom cell and the other to the right neighboring cell. In the first step, the input 'X' is '0' and 'Y' is '1' [7].

2.4 Effect of Fault in QCA Circuits

Various types of faults may occur in QCA circuit fabrication. The first type that is investigated here is called cell displacement. Cell displacement is the case when a cell is misplaced from the standard location relative to neighboring cells (Fig. 6b). In many cases, this defect affects the operation of the circuit. Figure 6c shows the second type of defect, called cell misalignment. In this case, the cell is somewhat shifted from the proper place. This defect may or may not affect the output logical value. The third type of defect is called cell omission (Fig. 6d). In this fault, a cell is deleted. If a cell is added to an empty space, this situation is called extra cell deposition defect (Fig. 6e). If the other cells are able to transmit information, the output does not change, otherwise the output changes and an error

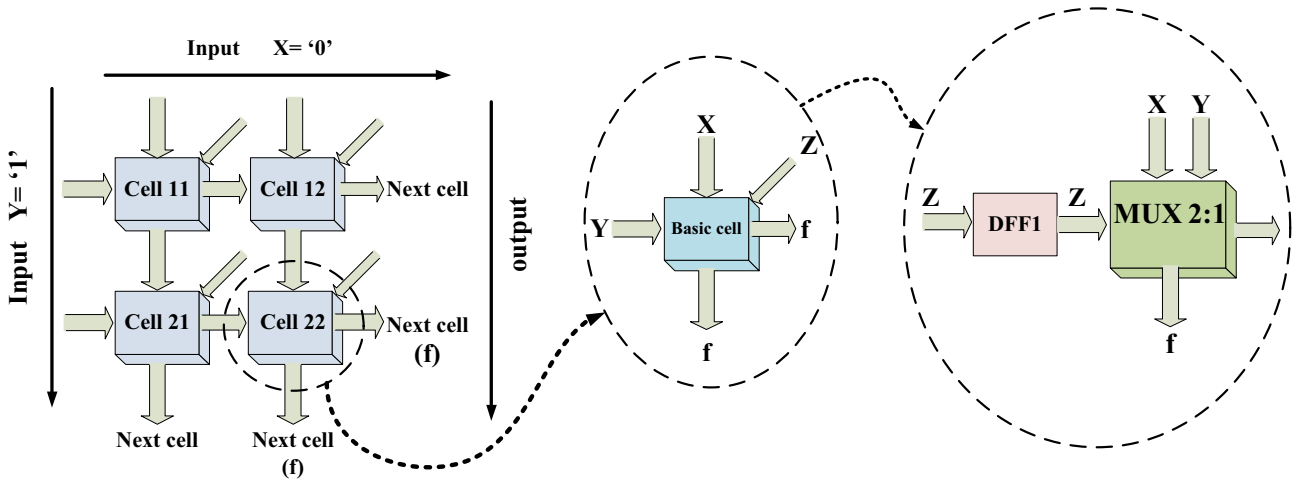


Fig. 5 Structure of 2×2 Akers array and a basic cell [30]

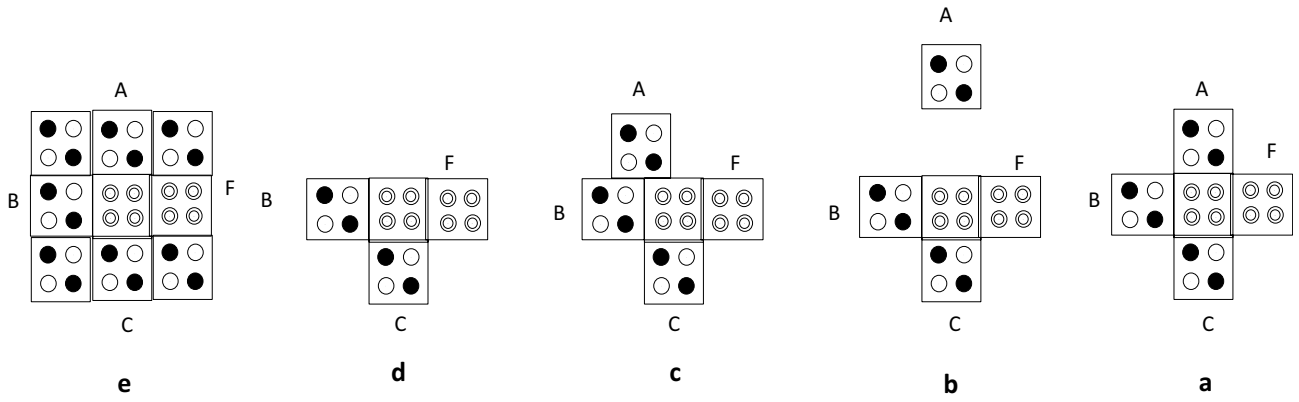


Fig. 6 **a** fault-free structure, **b** cell displacement, **c** cell misalignment, **d** cell omission, and **e** extra cell deposition [31]

occurs. It should be noted that there are also other defects, which can affect the QCA circuit operation.

In the present study, cell omission and extra cell defects are investigated. To evaluate the resistance of a circuit against the deletion or addition of cells, first, the cells of the circuit must be labeled (numbered). Then, the cells can be deleted or added in order while the output waveform is compared with the correct waveform, and finally, the comparison results have to be stored in a table. Fault tolerance is calculated by dividing the number of cells that produce the correct output (in the presence of defect) by the total number of cells (except input, output, or constant cells) according to Eq. (2) [20]:

$$FT = \frac{Number\ of\ correct\ output\ patterns}{Number\ of\ defective\ patterns} \times 100 \tag{2}$$

3 Proposed Novel Basic PIM Cell Structure in BQCA and TQCA Structures

In this paper, two main models are proposed using BQCA (Fig. 7) and TQCA (Fig. 8) structures. A bistable simulation engine and QCA Sim-Ternary Edition version 11/1/11 are used to simulate binary and ternary architectures [29].

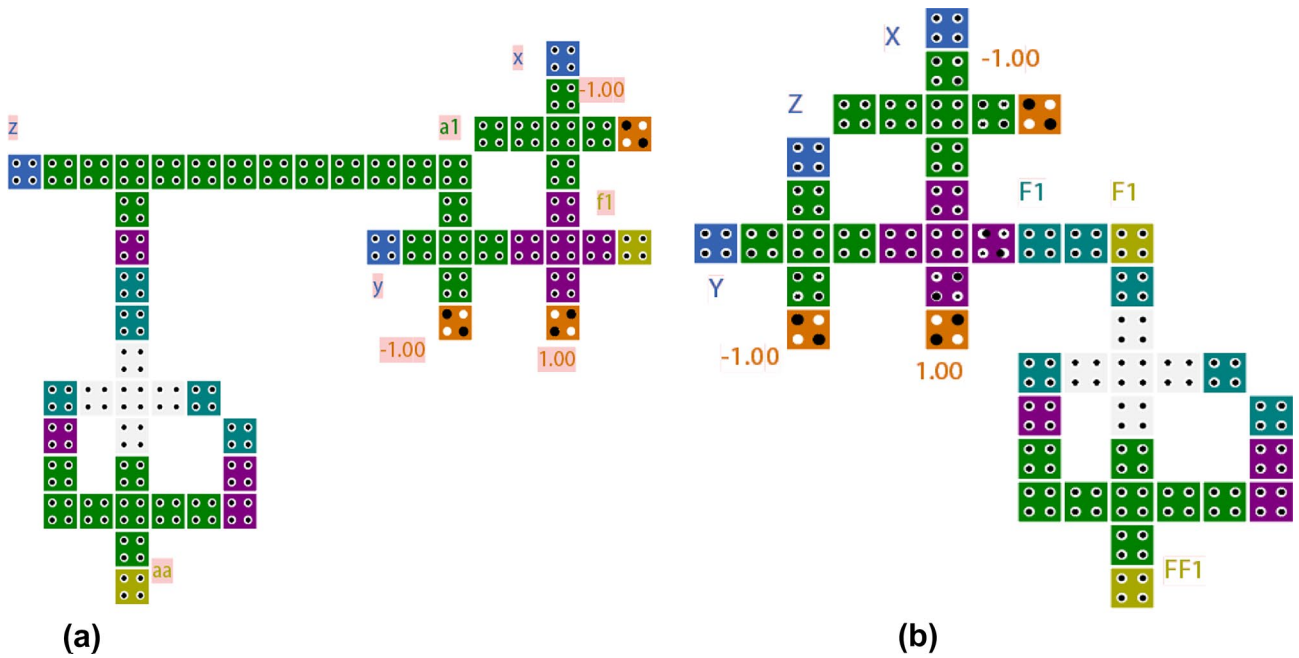


Fig. 7 Proposed binary models for the novel basic PIM cell; **a** B1 and **b** B2

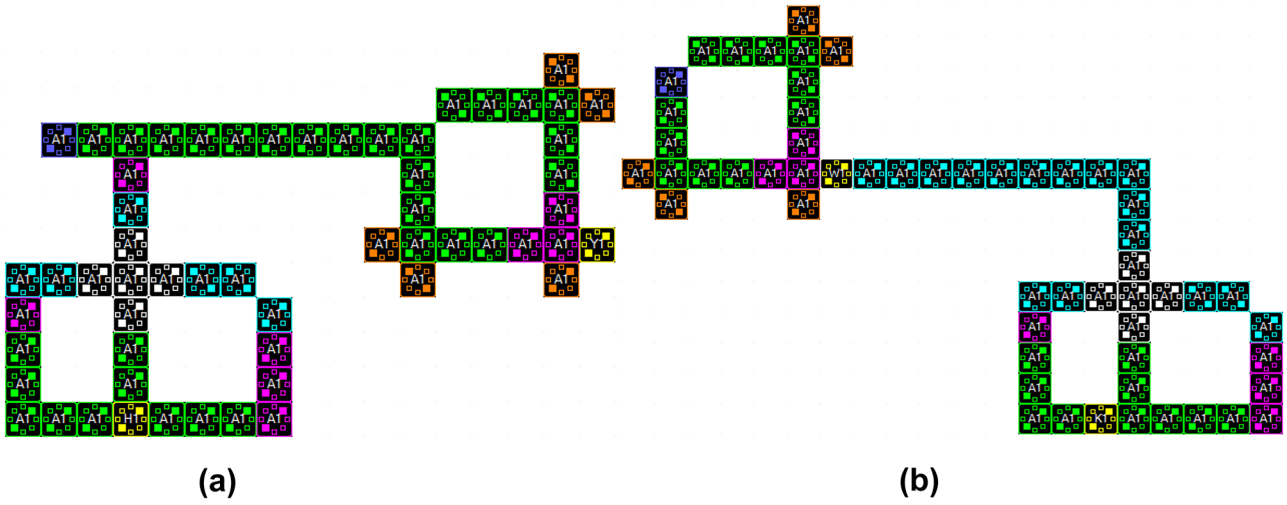


Fig. 8 Proposed ternary models for the novel basic PIM cell; **a** T1 and **b** T2

The first part of the novel basic PIM cell is a circuit to which the inputs are connected and is responsible for the operation of the switches in the Akers model. The second part is a QCA flip-flop. The first binary model named B1 is shown in Fig. 7a and the first ternary model named T1 is shown in Fig. 8a; B1 and T1 are responsible for storing the input data, and then, the calculations are performed in the next step. Figure 7b shows the second binary model named B2 and Fig. 8b shows the second ternary model named T2; B2 and T2 can store the calculation result and transfer them to the output.

The inputs, 'X' and 'Y', are '0' and '1' in binary logic, and 'A' and 'B' in ternary logic. This is useful for designing larger circuits and generating the Akers arrays of logic gates so that the circuit can properly open and close the Akers logic array switches. When the select line 'Z' is '1' (or 'B' in ternary logic), 'Y' is transferred to the output, otherwise 'X' is transferred to the output (Figs. 9 and 10). In Fig. 7a, 'F1' is the output of the Akers cell, and 'aa' is the memory output. In Fig. 7b, 'F1' is the output of the Akers cell, and 'FF1' is the memory output (DFF output), which has saved the output value. Similar outputs are shown in the ternary

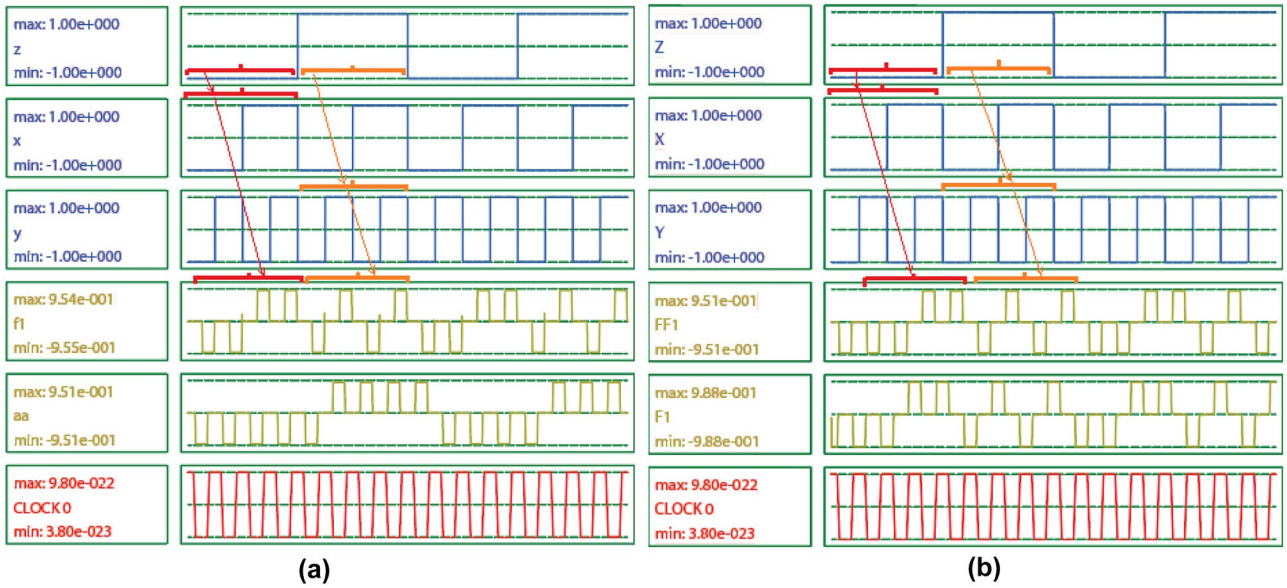


Fig. 9 Simulation results for two proposed binary basic PIM cells; **a** B1 and **b** B2

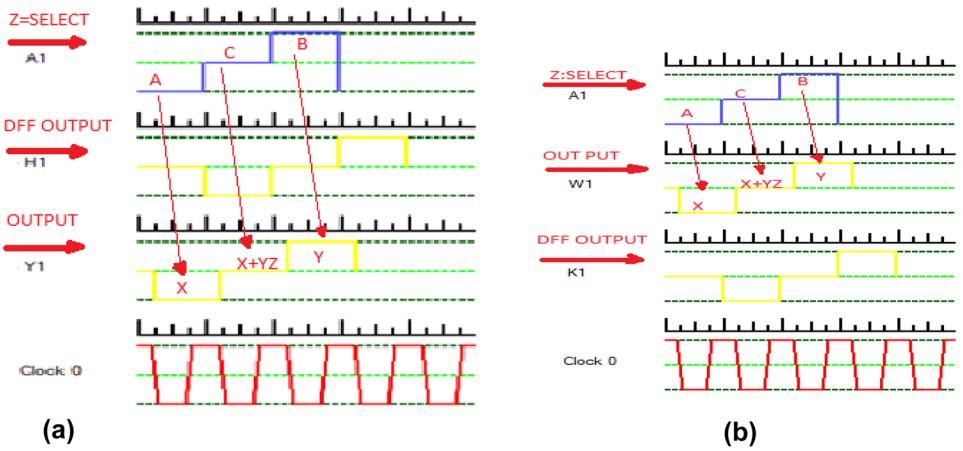


Fig. 10 Simulation results for two proposed ternary basic PIM cells; **a** T1 and **b** T2

structures. For more clarity two outputs are displayed. One of them is the output of the memory loop and the other is the main output (Figs. 9 and 10). Figure 11 shows that the operations of both switches are regulated by two AND gates. This is the case when the clock 'Z' is set to '1' (or to 'B' in ternary logic), and the AND1 gate that is connected to

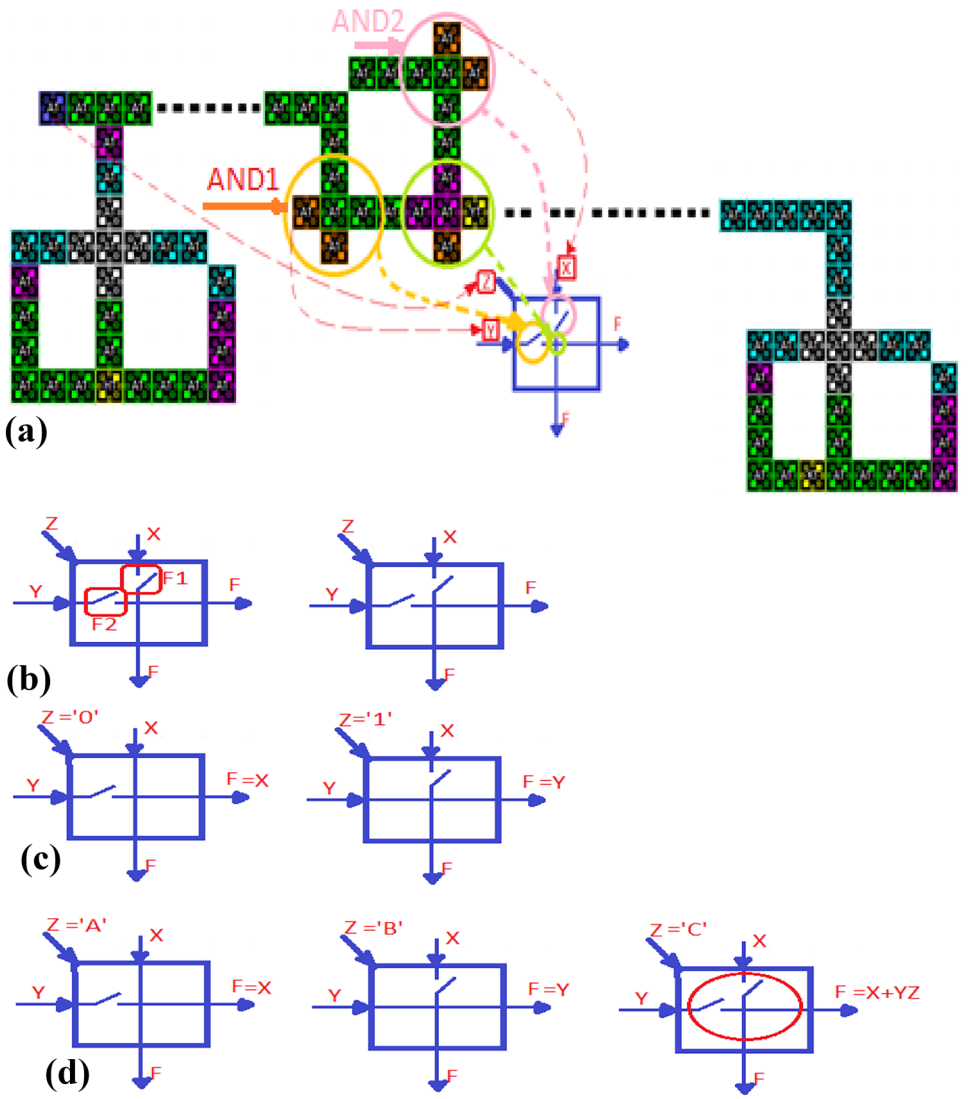


Fig. 11 Operation principle of switches in **a** novel basic cell, **b** Akers cell, **c** binary cell, and **d** ternary cell

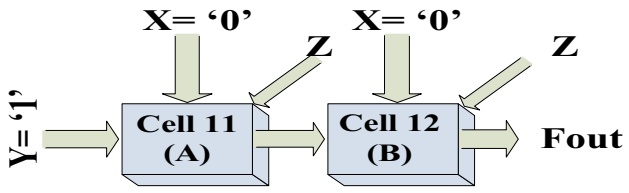


Fig. 12 Structure of AND Akers gate

it acts as a closed switch (Fig. 11c and d). When the clock 'Z' has a value of '0' (or ternary 'A'), the AND1 gate that is connected to it acts as an open switch, and the AND2 gate that is connected to the inverting 'Z' acts as a closed switch.

In the ternary design in Fig. 11-d, an additional mode is considered for the switch; i.e., when the value of 'Z' is C, both the AND1 and AND2 gates (both switches) are shared as denoted by X and Y in Eq. (1). In this case, it is not possible to clearly show the open or closed states of the switches in the figures. It can only be stated that the third case occurs when the output of the cell depends on both inputs X and Y. Therefore, the cell operates in three states in the ternary cell structure.

The proposed novel basic binary logic in Fig. 7a (model B1) comprises 59 BQCA cells with an occupied area of 0.11 µm2, while in Fig. 7b (model B2) it comprises 48 BQCA cells with an occupied area of 0.08 µm2. The latency in both models is 0.5 clock cycles.

The proposed basic ternary logic in Fig. 8a (model T1) includes 56 TQCA cells with an occupied area of 0.013392 µm2, while in Fig. 8b (model T2) it contains 57 TQCA cells and the occupied area is 0.02008575 µm2. The latency of both models is 0.75 clock cycles to the cell output.

4 Proposed Gates with PIM Structure in Binary and Ternary QCA

As mentioned, primary PIM cells are used to design larger circuits. In this part of the study, the design of logic gates (AND, OR, and XOR) with processing in memory capability is shown. These regular Akers structures can be used in future works. The XOR structure is an example of larger structures which is presented below.

4.1 Proposed AND Gate with PIM Structure in Binary and Ternary QCA

The proposed AND gate based on binary (ANDB1 and ANDB2) and ternary (ANDT1 and ANDT2) QCA-Akers for the proposed basic cell models are shown in Figs. 12 and 13. This structure consists of two Akers cells connected horizontally (Fig. 14). When A and B are '0' and '0', the output F2 is '0', and when A and B are '0' and '1', or vice versa, F2 is '0' (Fig. 15). The output F2 is '1' only when both A and B have values of '1' (Fig. 15a and b). The output values 'aa' and 'bb' are the same as 'A' and 'B' in first model, while 'FF1 and 'FF2' are equal to output values 'F1' and 'F2' in second model. For more clarity, two outputs are shown. One of them is the output of the memory loop and the other is the main output. The main output for binary structures is F2, and the main output for ternary structures is Q1. Other outputs are only displayed in the simulation and can be replaced with normal cells.

In ternary: X AND Y = X.Y = MAJ ('A', X, Y), 'A' is a constant state (2).

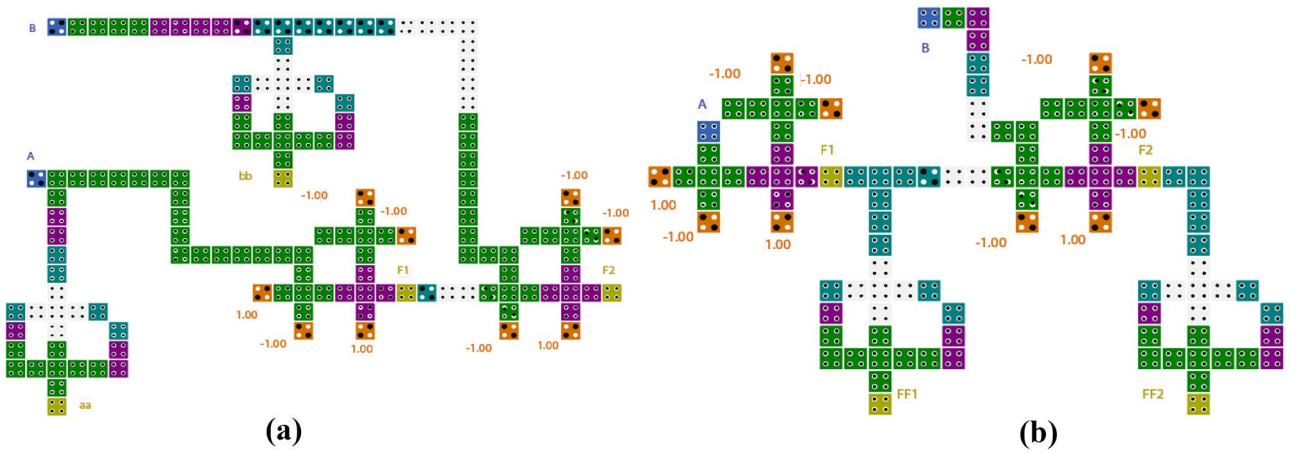


Fig. 13 Proposed binary two-input AND gate with the Akers structure for **a** ANDB1 and **b** ANDB2

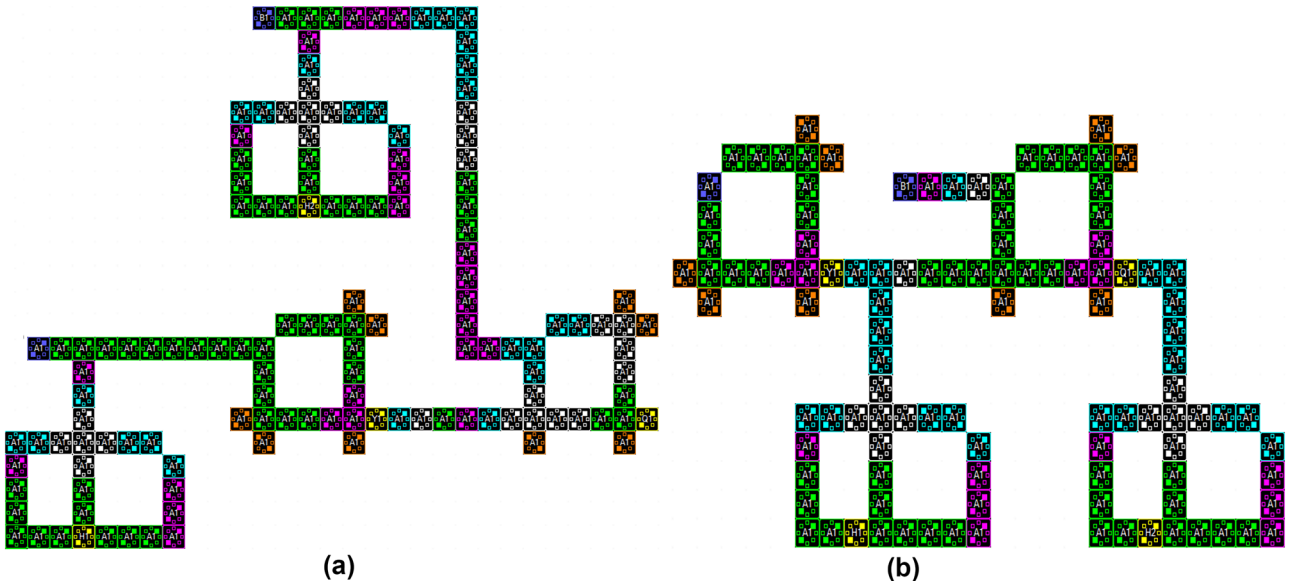


Fig. 14 Proposed ternary two-input AND gate with the Akers structure for **a** ANDT1 and **b** ANDT2

In Fig. 16a and b, when the inputs A1 and B1 are 'A' and 'A', X is transferred from the upper switch in the second cell to the output and the output Q1 becomes 'A'. When the inputs A1 and B1 are 'A' and 'B', the upper switch is closed in the first cell, while in the second cell, the value of input Y, which is the same as the output of the previous cell, is transferred to the output. If the inputs A1 and B1 are 'B' and 'A', the operation of the switches in the cells is reversed. When inputs A1 and B1 are 'B' and 'B', the switches connected to Y are closed and the main output Q1 becomes 'B'. When one or both inputs in the AND gate are 'C', the output is calculated by Eq. (1) and the states of the switches cannot be determined (Fig. 16).

Moreover, the values of inputs or outputs of each binary or ternary Akers cell are stored in the flip-flops according to the proposed model.

The first proposed binary model ANDB1 has 145 cells. The occupied area is 0.27 μm2 and the latency is 1.5 clock cycles. The second proposed binary model ANDB2 has 108 cells. The occupied area is 0.19 μm2 and the latency is 1.5 clock cycles.

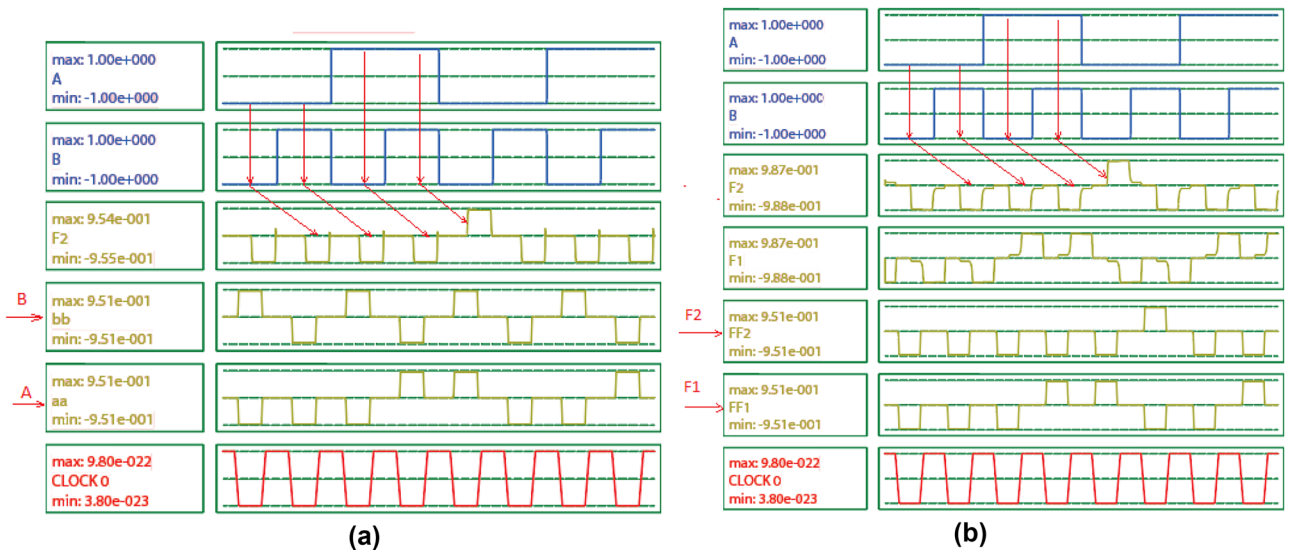


Fig. 15 Simulation results of binary AND gate with Akers structure for **a** ANDB1 and **b** ANDB2

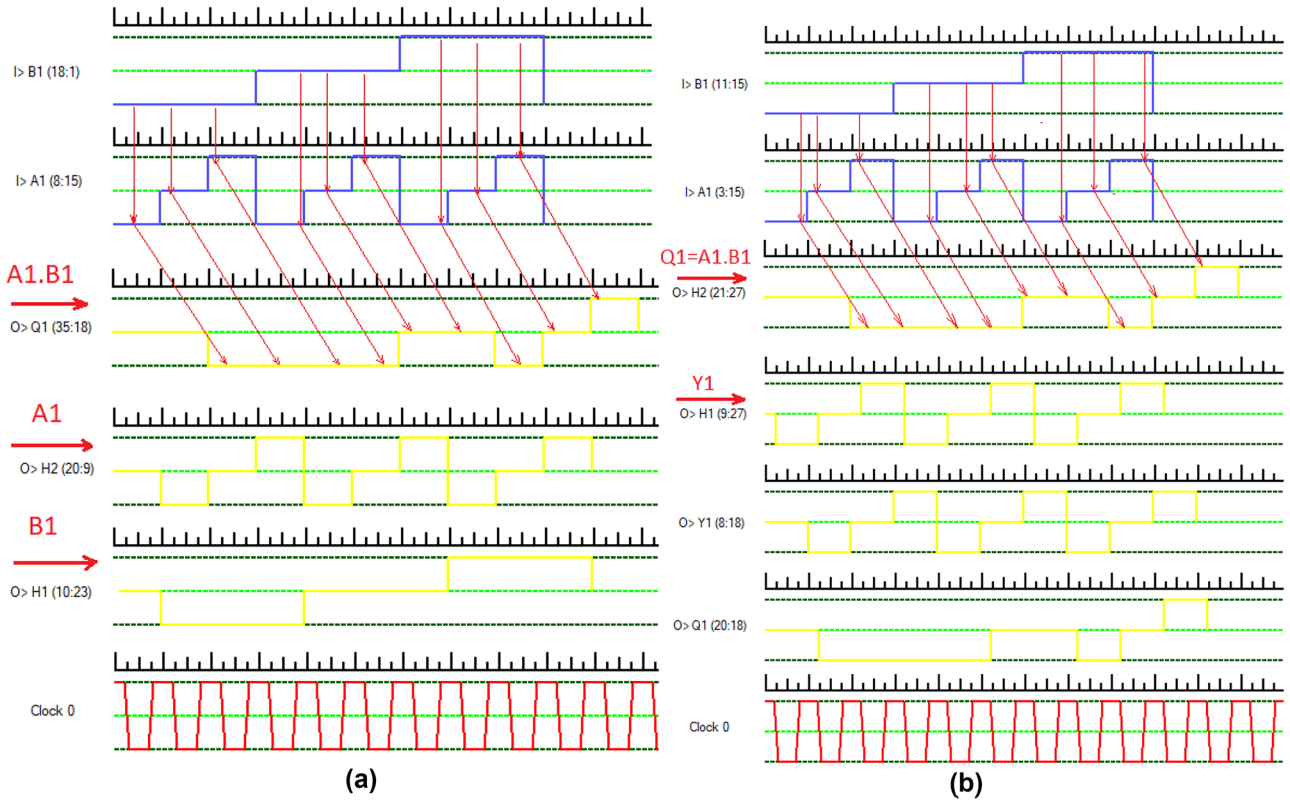


Fig. 16 Simulation results of ternary AND gate with Akers structure for **a** ANDT1 and **b** ANDT2

The first proposed ternary model ANDT1 for Akers structure with AND function has 135 cells. The occupied area and the latency are 0.04797 µm2 and 2.25 clock cycles. The second proposed ternary model ANDT2 for Akers structure with AND function has 109 cells. The occupied area and the latency are 0.026924 µm2 and 1.75 clock cycles.

4.2 Proposed OR Gate with PIM Structure in Binary and Ternary QCA

The proposed OR gate models based on binary (named ORB1 and ORB2) and ternary (named ORT1 and ORT2), which use the novel basic PIM models, are shown in Figs. 17 and 18, respectively. This structure consists of two basic Akers cells connected vertically (Fig. 19). Figure 19 shows the Akers structure for the OR gate design. Figures 20 and 21 show the Akers OR gate simulation results for the BQCA and TQCA structures, respectively.

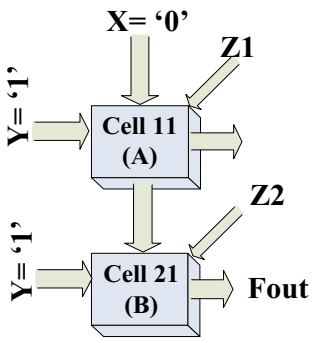


Fig. 17 Two-input OR gate with Akers structure

For both models ORB1 and ORB2 in Fig. 20a and b, when both inputs are '00', the output is '0', and when both inputs are '01' or '10', the output is '1'. When both inputs A and B are '1', the output F2 becomes '1'. For ORB1 in Fig. 20a, the DFF outputs aa and bb are equal to inputs A and B. For ORB2, the DFF outputs FF1 and FF2 are equal to the outputs F1 and F2 of each cell (Fig. 20b). F2 and Y1 are the main outputs of the binary and ternary structures that show the OR gate operation. Other outputs are used only in the simulation (to display the correct operation of the circuit) and can replace with normal cells.

In ternary: X OR Y = X + Y = MAJ ('B', X, Y), 'B' is a constant state.

In Figs. 18 and 21 (for ORT1 and ORT2), when the inputs A1 and B1 are 'A' and 'A' in both cells, the upper switches are closed and X is transferred to the output. Then, X is transferred to the main output and output Y1 becomes 'A' (see Fig. 21a and b). When inputs A1 and B1 are 'A' and 'B', the upper switch is closed in the first cell. In the second cell,

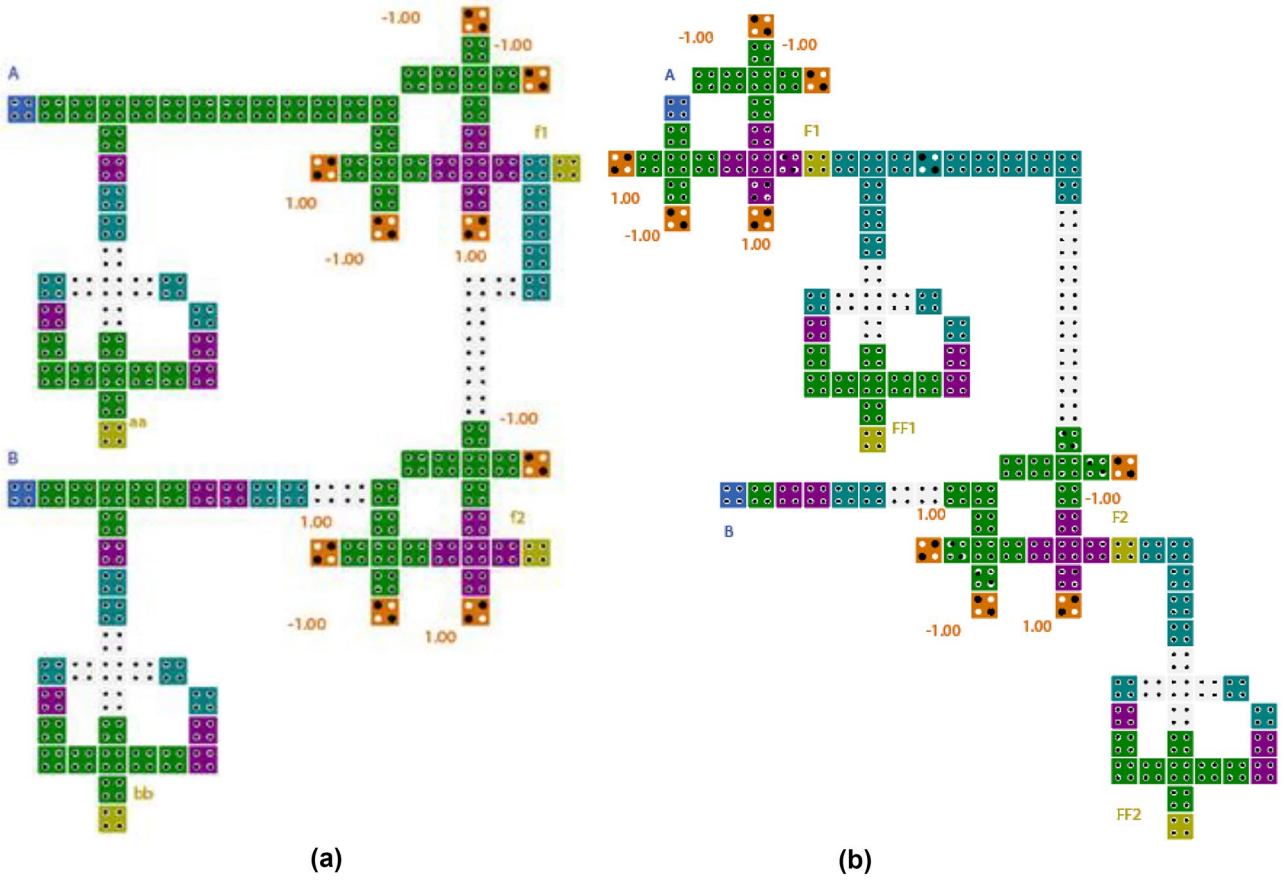


Fig. 18 Proposed binary OR gate with Akers structure for **a** ORB1 and **b** ORB2

Y is transferred to the output and its value becomes 'B'. If the values of inputs A1 and B1 are 'B' and 'A', the operation of the switches is reversed, and finally, 'B' is transferred to the main output Y1 again. When inputs A1 and B1 are 'B' and 'B', the switches connected to them are closed and the values of Y in both cells are transferred to their outputs and the main output Y1 becomes 'B'. For ORT1 in Fig. 21a, the DFF outputs H1 and H2 are equal to inputs A1 and B1. For ORT2 in Fig. 21b, the DFF outputs K1 and K2 are equal to outputs W1 and Y1 of each cell.

According to the values of the outputs based on the inputs, the function of the OR gate is realized correctly in the Akers binary and ternary structures. Moreover, in the first proposed model, the input values are stored in the flip-flops of the circuit, and in the second model, the output value of each Akers cell is stored.

The first proposed binary model ORB1 has 128 cells, and the occupied area and latency are 0.21 µm2 and 1.5 clock cycles. The second binary model ORB2 has 120 cells, and the occupied area and the latency are 0.29 µm2 and 1.5 clock cycles.

The first proposed ternary model ORT1 for the Akers structure with OR function has 122 cells. The occupied area and the latency are 0.02808 µm2 and 1.75 clock cycles. The second proposed ternary model ORT1 for the Akers structure with an OR function has 126 cells; the occupied area and latency are 0.0429975 um2 and 1.75 clock cycles.

4.3 Proposed XOR Gate with PIM Structure in Binary and Ternary QCA

The XOR gate structure is designed using the first proposed basic PIM cell in BQCA (B-XOR) and TQCA (T-XOR). The diagram of the XOR gate based on the Akers array is shown in Fig. 22.

The Akers array is used to implement the XOR gate. In this structure, there are two rows and two columns. One memory is shared for each row and four multiplexers are used in the gate structure. The value of X is fixed and equal to "-1" in BQCA (logic 0(. The outputs of the cells in the first row, which control the value of X, are inserted to the second row. The value of Y is equal to "1" in BQCA (logic

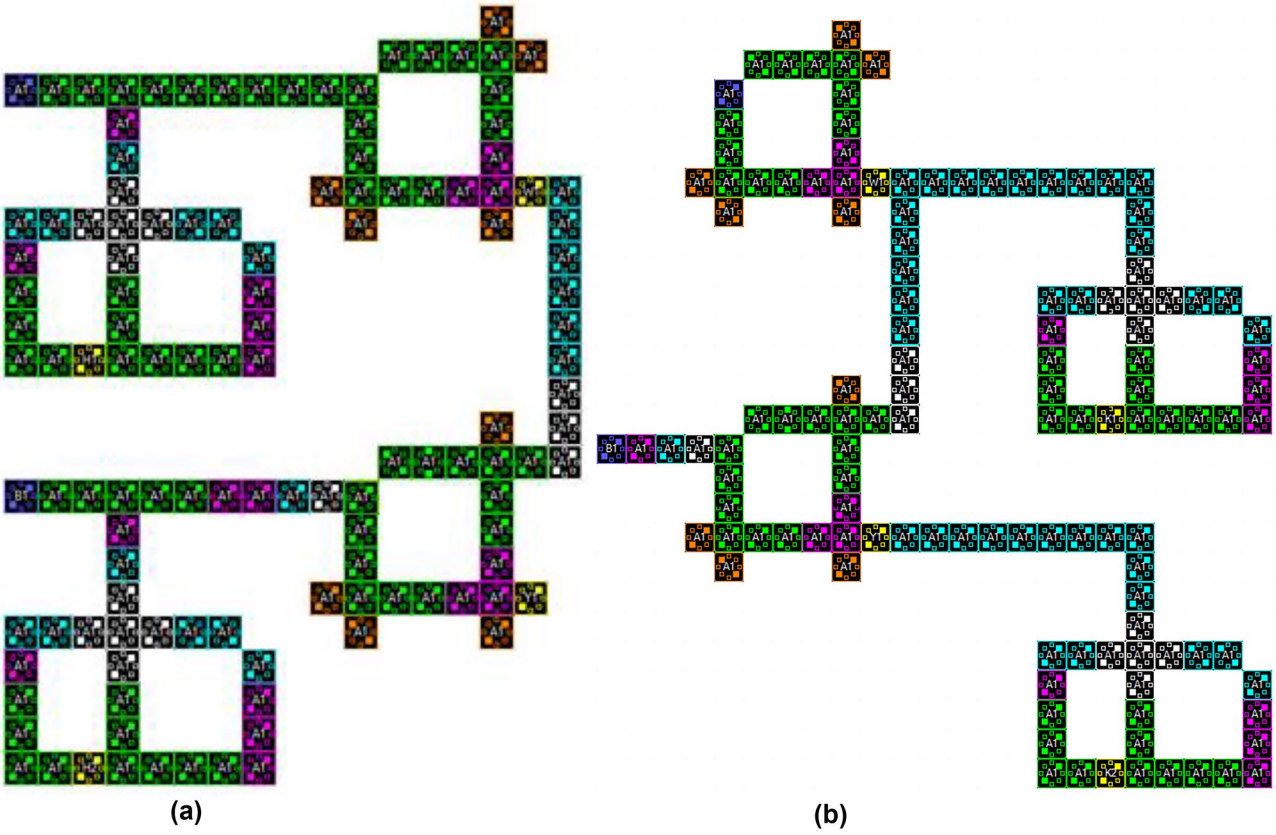


Fig. 19 Proposed ternary two-input OR gate with Akers structure for **a** ORT1 and **b** ORT2

1(. The output is '1' when one of the two inputs is equal to '1', but when both inputs are '1' or '0', the output is equal to '0' (Fig. 23).

The ternary structure of the XOR gate is shown in Fig. 24. In this structure, there are three levels in the input, so instead of two values, three values are applied to the inputs. In this

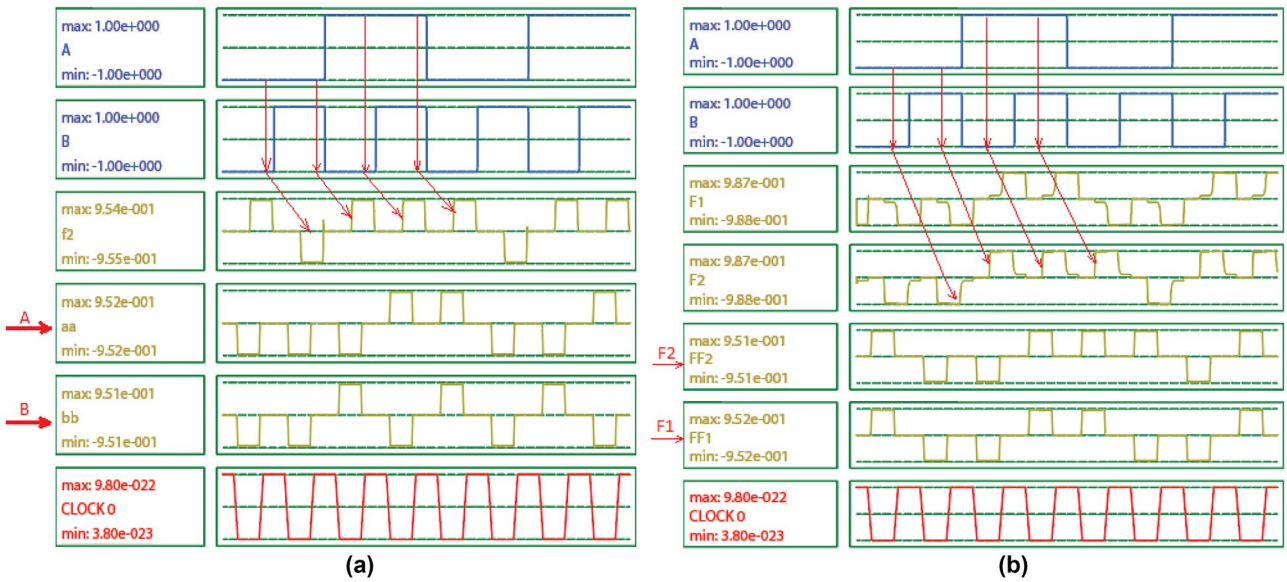


Fig. 20 Simulation results of binary two-input OR gate with Akers structure; **a** ORB1 and **b** ORB2

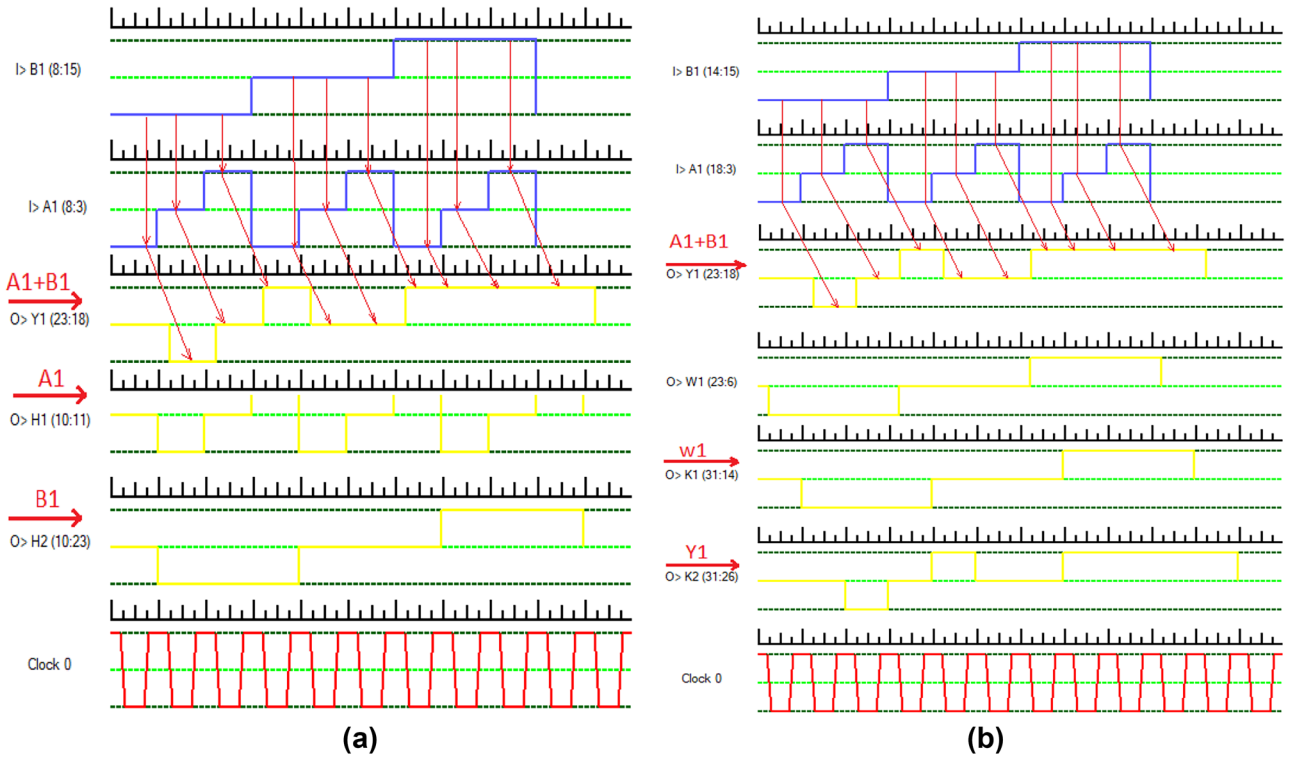


Fig. 21 Simulation results of OR gate with Akers structure; **a** ORT1 and **b** ORT2

situation, the density of stored and processed data increases. The Akers array is also used to design this structure. The values of X and Y in the first row and column are constant and equal to 'A' and 'B'.

The simulation results of XOR are shown in Fig. 25. The simulation results of the ternary XOR structure in QCA Sim-Ternary Edition software version 1/0/11/1 are shown in Fig. 26. As can be seen, when one of the inputs is equal to 'C', the output is equal to 'C'. If the inputs are 'A' or 'B', the output is 'A', and only if both inputs are different and equal to 'A' and 'B', the output is 'B'. Two outputs H1 and H2 store the inputs and are equal to the values of inputs A1 and B1 (Fig. 25). In fact, the XOR gate with ternary PIM structure can store and process more information in smaller occupied area, compared to the binary structure. Accordingly, the output diagram confirms the correct operation of the XOR gate. F and F4 are the main outputs in binary and ternary XOR. For more clarity, another outputs are also shown. The proposed binary XOR circuit occupies 0.35 µm2 of area, consists of 266 cells, and has a latency of 2.5 clock cycles. The proposed ternary XOR circuit consists of 281 cells and the occupied area is equal to 77745.5 nm2 or 0.0777455 µm2 and the latency is equal to 4 clock cycles.

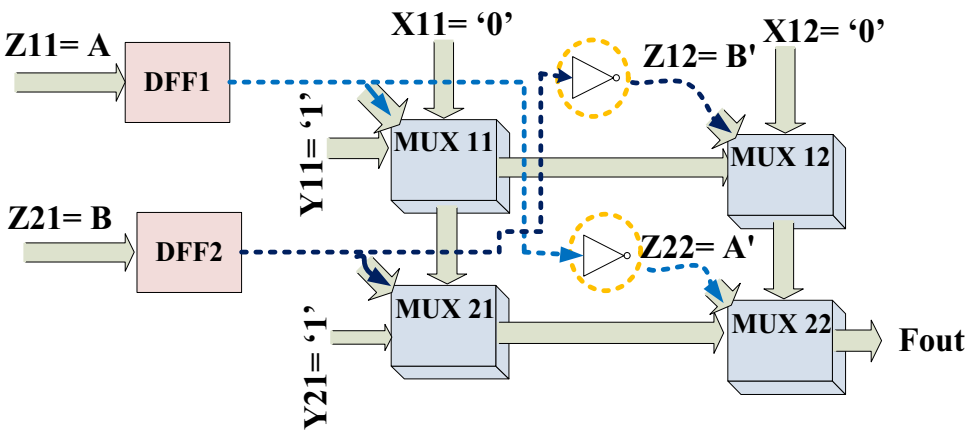


Fig. 22 Akers structure of two-input XOR gate

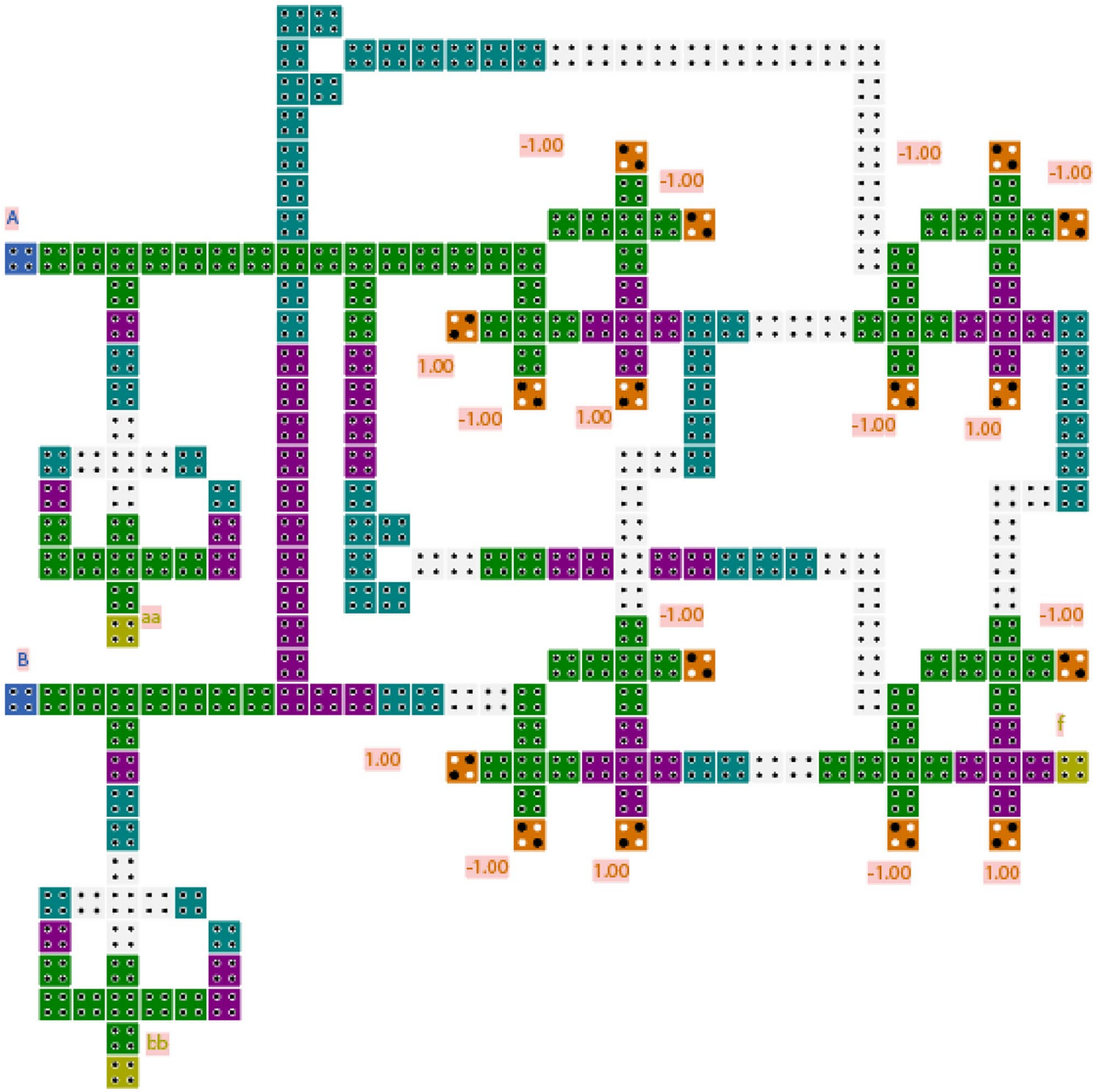


Fig. 23 Proposed binary two-input XOR (B-XOR) gate with Akers structure and the first proposed basic cell model

A comparison of the XOR structures indicates that the proposed ternary XOR is better than other design [19] in terms of latency and occupied area. The structures are not comparable in terms of cell count because the model presented in [19] does not include a memory section. The ternary structure can store and process more information. Moreover, in terms of cost, which is defined as the ratio of occupied area to cell count, the ternary structure is more efficient than both binary structures. A comparison of the proposed binary basic PIM cell and other designs is presented in Table 2.

5 Effect of Fault

To investigate the cell omission defect, we remove cells sequentially and compare the output waveform with the correct waveform. According to Table 3, by removing 12 cells, the output is still correct and total cells are 51 (Fig. 27a). According to Eq. (2), the FT of cell omission (missing cells) is 23.52%.

$$FT\ for\ BI\ (cell\ omission) = \frac{12}{51} \times 100 = 23.52\%$$

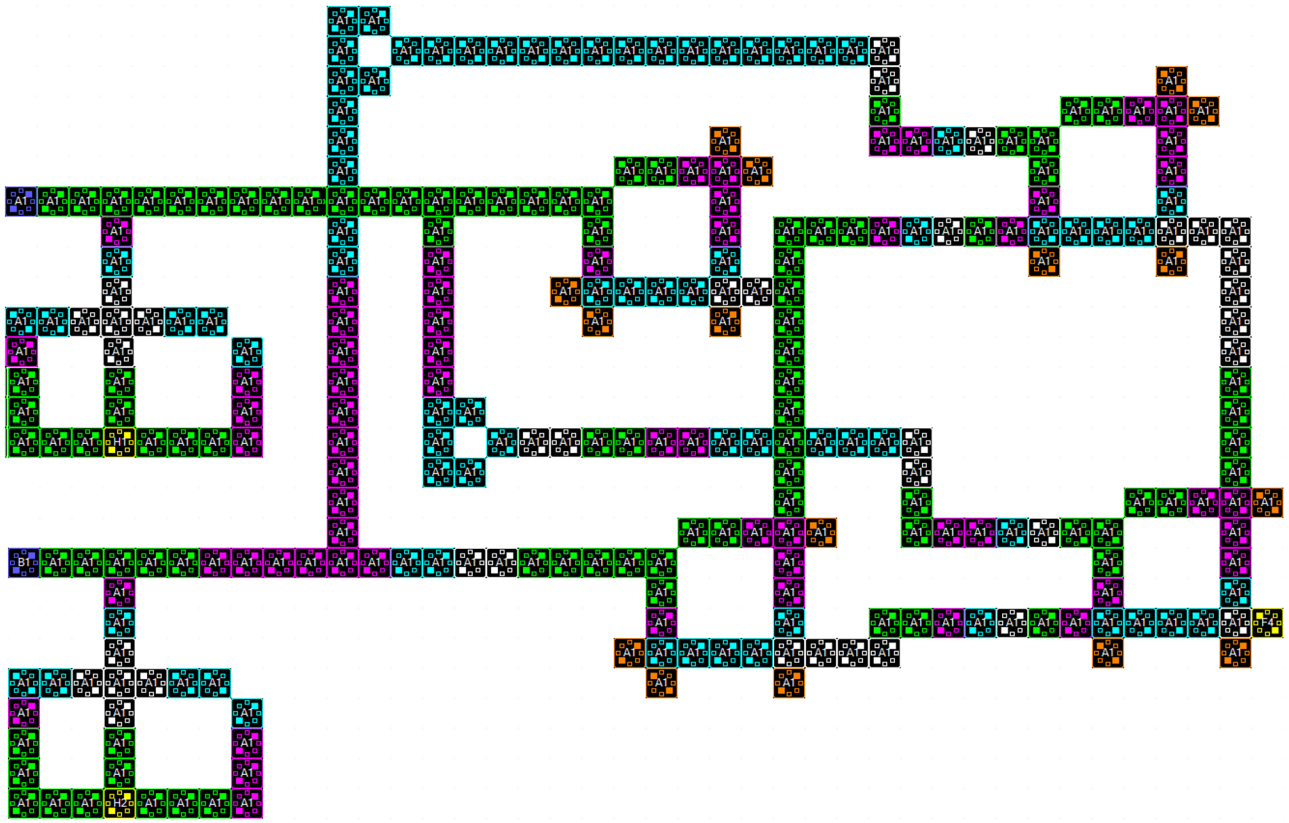


Fig. 24 Proposed ternary two-input XOR (T-XOR) gate with Akers structure and the first proposed basic cell model

Cells A1-A10 are added to the empty spaces of the structure and the effect of adding each cell on the output is evaluated (Table 4). Adding four cells from a total of 10 cells results in correct output. By inserting these values into Eq. (2), the FT of extra cell defect is equal to 40%.

$$FT\ for\ BI\ (extra\ omission) = \frac{4}{10} \times 100 = 40\%$$

For B1, an acceptable result is obtained in terms of FT against single-cell omission and extra cell defect.

Figure 27b shows the numbering of B2. Moreover, cells A1-A10 are added to examine the extra cell deposition defect. After removing each cell, the output waveform is examined for all input modes and the results are shown in Table 5. As indicated in this table, 22 cells have correct output from a total of 38 cells. According to Eq. (2), the value of FT is 57.89%.

$$FT\ for\ B2\ (cell\ omission) = \frac{22}{38} \times 100 = 57.89\%$$

To investigate the extra cell deposition defect, cells A1-A10 are added to the empty spaces of the proposed structure. According to Table 6, 10 cells are added and the correct output is obtained by adding 8 cells. Therefore, the FT of the extra cell deposition defect is 80%.

$$FT\ for\ B2\ (extra\ omission) = \frac{8}{10} \times 100 = 50\%$$

This structure, especially the memory part and its multiplexer, is very similar to B1, except that the memory is located at the end of the circuit. Despite many similarities between the two structures, it should be asked "why has FT increased for B2?" To answer this question, we compare the circuit configuration and cell count in both structures. In both structures, the number of majority and inverse gates are equal (five majority gates and two NOT gates) and the clocks are the same. In other words, these parameters cannot be considered as the basis for comparing the gates. Therefore, we examine the communication routes of the gates. In B1, there is a 9-cell gap between the main input and the memory input, and 13-cell gap between the main input and the multiplexer input. However, in B2, the main input is connected directly to the multiplexer input and the main output is connected to the memory through only 6 cells. Therefore, it can be concluded that the fault-effects may be more pronounced because of the existence

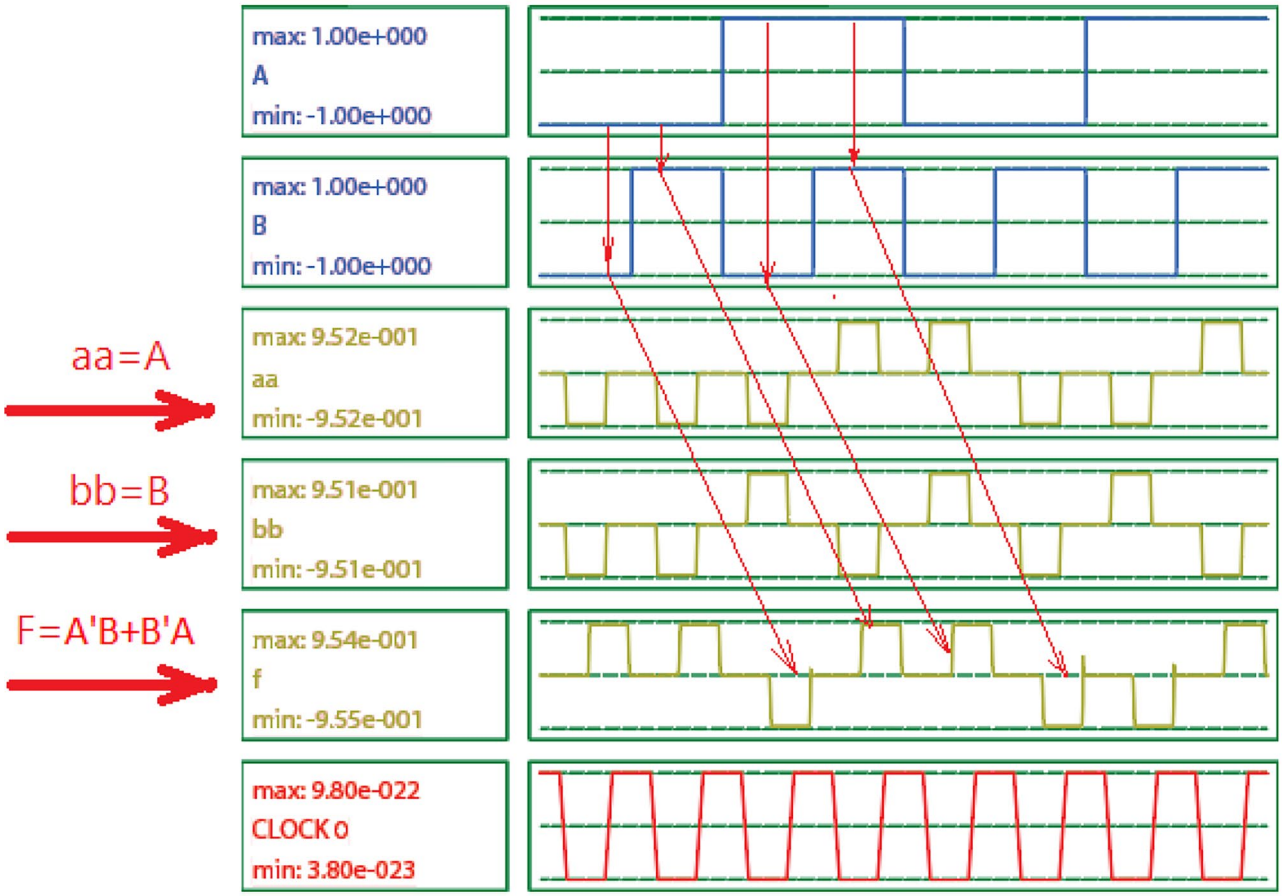


Fig. 25 Simulation results of two-input binary XOR gate with Akers structure and the first proposed model

of longer distance between applied signals (inputs) and those to the memory and multiplexer in B1. This large distance changes the electrostatic effect between the cells when a fault occurs and the signal is not transmitted properly to neighboring cells.

Figure 28a shows the numbering of ternary cells. This structure is based on the binary structure proposed for B1 and the memory is located on the input side.

After removing each cell, the output waveform is examined and the results are shown in Table 7. As indicated in this table, 26 cells creates correct output from a total of 50 examined cells. According to Eq. (2), the value of FT is 52%.

$$FT\ for\ T1\ (cell\ omission) = \frac{26}{50} \times 100 = 52\%$$

Cells A1-A24 are added to the empty spaces of the structure, and then, for different input modes, the output is evaluated (Table 8). Adding 22 cells from a total of 24 cells results in no change in the output waveform. Using Eq. (2), the FT of extra cell deposition defect is equal to 91.6%.

$$FT\ for\ T1\ (cell\ omission) = \frac{22}{24} \times 100 = 91.6\%$$

Figure 28b shows the numbering of T2, which is based on the binary scheme B2 in the three-valued structure. A total

Table 2 Comparison of the proposed binary PIM basic cell and other designs

Circuit	Latency (clock cycles)	Occupied area (μm2)	Complexity (cell count)	Costa-$c = \frac{occupiedarea(nm)}{complexity}$	Ternary/ Binary (T/B)	Technology (nm)
XOR presented in [19]	4.75	0.23	184	1.25	BINARY	18
Proposed binary-PIM-XOR	2.5	0.35	266	1.315	BINARY	18
Proposed ternary-PIM-XOR	4	0.077	281	0.27	BINARY	8

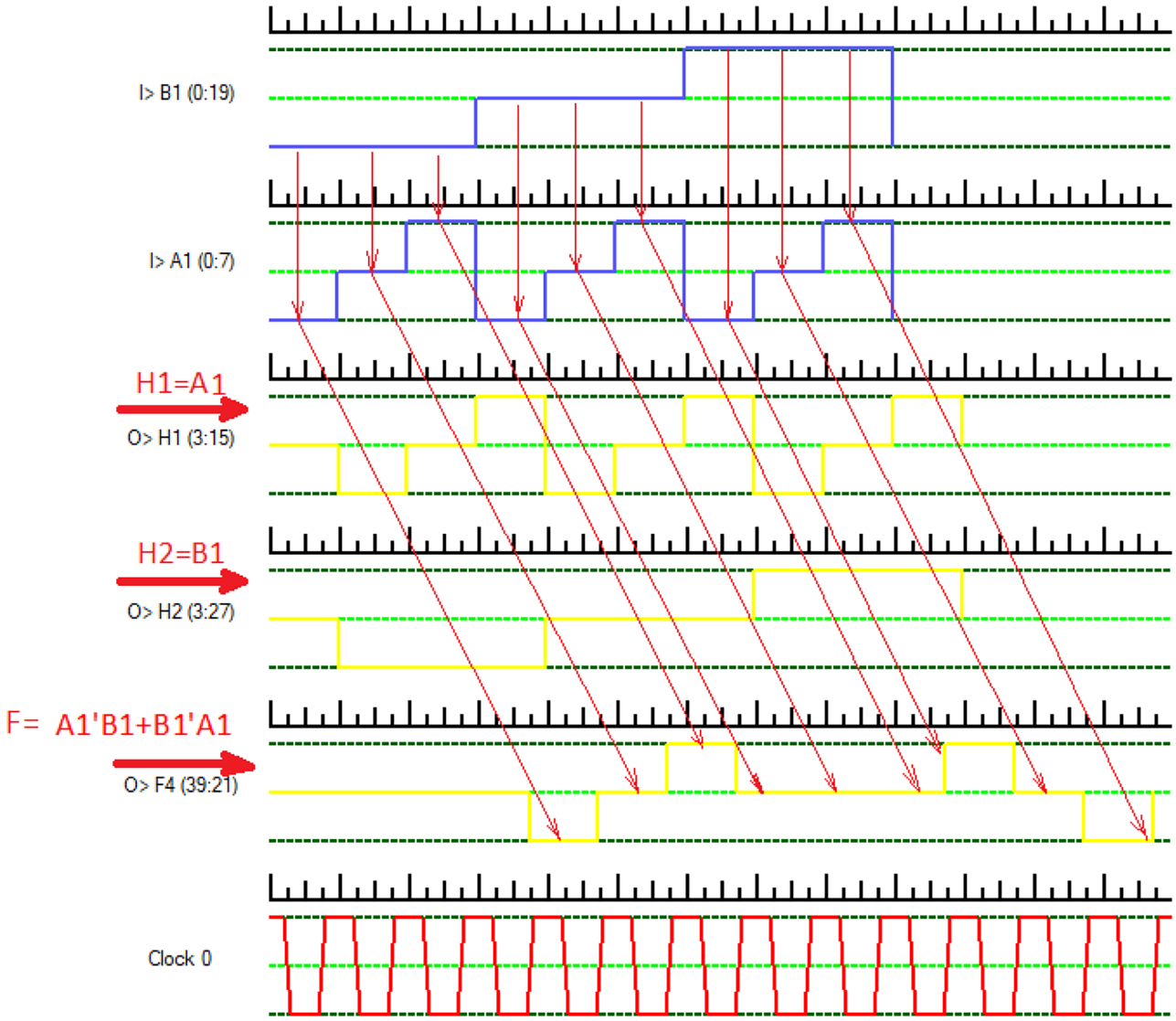


Fig. 26 Simulation results of two-input ternary XOR gate with Akers structure and the first proposed model

Table 3 Investigating cell omission fault for B1

Impact on output	Cell number	Impact on output	Cell number	Impact on output	Cell number	Impact on output	Cell number	Impact on output	Cell number
Yes	45	No	34	Yes	23	Yes	12	Yes	1
Yes	46	No	35	Yes	24	Yes	13	Yes	2
Yes	47	Yes	36	No	25	Yes	14	Yes	3
No	48	No	37	No	26	Yes	15	Yes	4
No	49	No	38	Yes	27	Yes	16	Yes	5
No	50	Yes	39	Yes	28	Yes	17	Yes	6
Yes	51	No	40	Yes	29	Yes	18	Yes	7
		Yes	41	Yes	30	Yes	19	Yes	8
		Yes	42	Yes	31	Yes	20	Yes	9
		Yes	43	Yes	32	Yes	21	Yes	10
		No	44	No	33	Yes	22	Yes	11

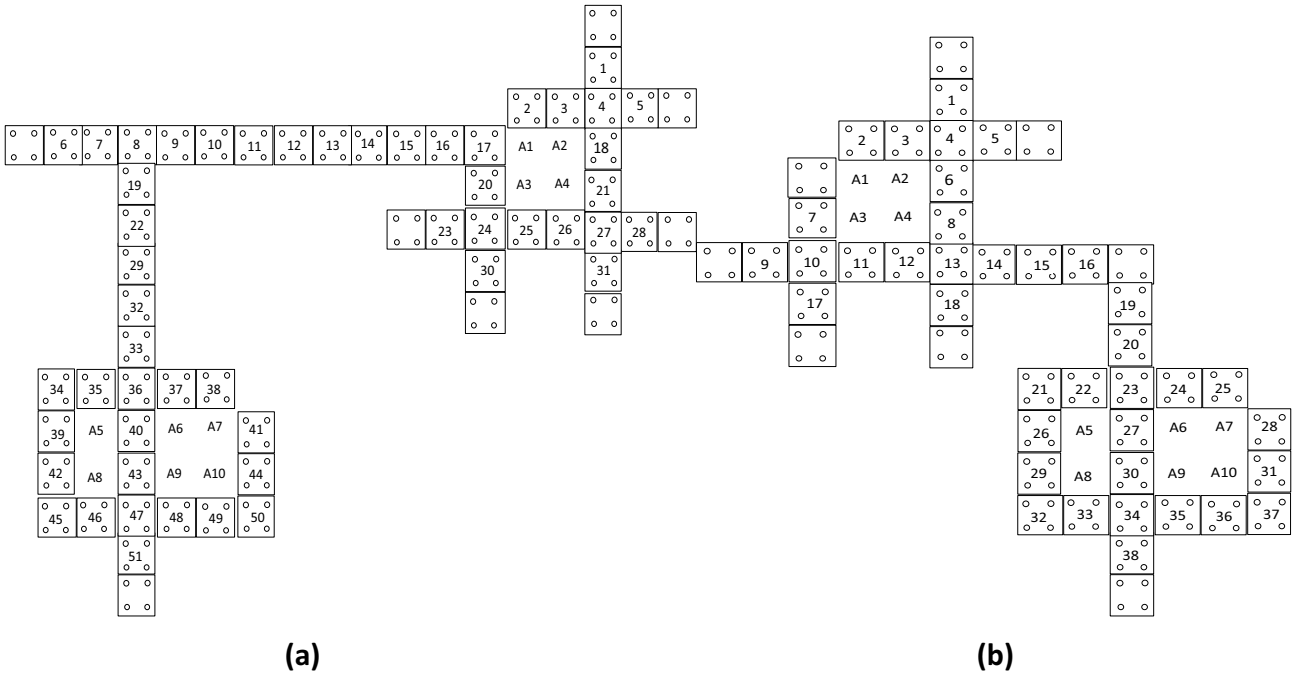


Fig. 27 Numbering QCA cells; **a** B1 and **b** B2

of 49 cells are evaluated and 25 cells have no effect on the output (Table 9). The value of FT is obtained by inserting these values into Eq. (2).

To evaluate the extra cell deposition defect, we add cells A1-A24 to the empty spaces of the circuit, respectively. A total of 24 cells are evaluated and 22 cells have no effect on the output waveform (Table 10). By inserting these values into Eq. (2), FT is equal to 91.66%.

$$FT\ for\ T2\ (cell\ omission) = \frac{25}{49} \times 100 = 51.02\%$$

$$FT\ for\ T2\ (extra\ omission) = \frac{22}{24} \times 100 = 91.66\%$$

The structures T1 and T2 are optimized compared to B1 and B2 in terms of FT and occupied area. The FTs of T1 and T2 are the same, which can be attributed to the equality of the number of empty space cells and structures. However, the question is "why has FT (for extra cell) increased compared to B2?".

This question can be answered as follows: The dimension of a ternary cell (8 nm) is smaller than that of a binary cell (18 nm). So, for ternary structure, the cells are closer, so, less error occurs. We study and analyze the profile of external electrostatic energy in order to justify the fact the ternary structures admit improved fault tolerance compared to the binary one. First, we consider a wire with three cells in each of the structures. Then, we assume that the middle cell is removed. The external electrostatic energy must travel a distance of 18 nm, in the binary structure, because its polarization can transfer from the first cell to the third cell. In the ternary structure, this distance is reduced to 8 nm. Therefore, the probability of the occurrence of faults in the ternary structure is less than that for the binary architecture, because the electrostatic effect between two neighboring cells in ternary QCA, is stronger than that in binary one.

In the transformation of structures from binary to ternary, the occupied area is also reduced. According to the literature, the FT is reduced when the number of cells increases, and as a result, the occupied area increases. However, our proposed method can simultaneously reduce the occupied area and improve FT.

Table 4 Investigating extra cell defect for B1

Impact on output	Cell number	Impact on output	Cell number
No	6	Yes	1
Yes	7	Yes	2
No	8	Yes	3
No	9	Yes	4
No	10	Yes	5

Table 5 Results of cell omission defect for B2

Impact on output	Cell number	Impact on output	Cell number	Impact on output	Cell number	Impact on output	Cell number
No	34	No	23	No	12	Yes	1
No	35	No	24	Yes	13	Yes	2
No	36	No	25	No	14	Yes	3
Yes	37	Yes	26	No	15	Yes	4
Yes	38	No	27	No	16	Yes	5
		No	28	Yes	17	Yes	6
		No	29	Yes	18	Yes	7
		No	30	No	19	Yes	8
		No	31	No	20	No	9
		No	32	No	21	Yes	10
		Yes	33	No	22	No	11

6 Power Estimation

The QCA-Pro software is used to perform energy calculations in QCA. The proposed binary basic PIM cells are evaluated for tunneling energies of 1.5, 1, and 0.5 Ek at 2 °K (Fig. 29). Darker color cells dissipate higher power. Table 11 shows the switching and leakage energies.

For a better comparison between ternary and binary structures, we calculate the external electrostatic energy transfer between two binary cells and between two ternary cells. The amount of external electrostatic transfer energy between two binary cells is equal to $0.033 \times 10\text{-}20$j and between two ternary cells is equal to $0.196 \times 10\text{-}20$j, according to Eq. (3). The external electrostatic energy transfer between the two ternary cells is more than that between the binary ones. Therefore, the structures designed with ternary cells has more fault tolerance because the electrostatic energy interacts over long range and less affected by cell deletion or addition.

$$E_{ij} = \frac{1}{4\pi\varepsilon_0\varepsilon_r} \sum_{i=0}^{m} \sum_{j=0}^{n} \frac{q_i q_j}{d_{ij}} \tag{3}$$

As can be seen, the second binary basic PIM cell model (B2) consumes less energy than the first one (B1). Moreover, B2 consumes less total energy compared to other architectures and models.

Table 6 Results of extra cell deposition defect for B2

Impact on output	Cell number	Impact on output	Cell number
No	6	Yes	1
Yes	7	No	2
No	8	No	3
No	9	No	4
No	10	No	5

A comparison of different PIM and RAM structures is shown in Table 12. It is observed that the binary and ternary basic PIM cell structures have an acceptable occupied area and complexity compared to other structures. The cost function, which is the ratio of occupied area to the number of cells, is much more efficient for the ternary structure than for the binary structure.

The ternary structure carries more information and has an acceptable complexity and occupied area. Moreover, the ternary structure is more desirable and similar to fuzzy and real systems.

Considering that the dimensions of the ternary cells are 8 nm, the AND and OR gates designed with the second basic ternary model (T2) occupy less area and have lower latency and complexity compared to other structures. Ternary structures have more FT than binary structures (Table 13). The fault tolerance for extra cell deposition in ternary structures is increased to 91.6%. The main reasons can be summarized as the reduction of dimensions and the increase of external electrostatic energy. As you can see, we calculate the cost value for some of articles. It is observed that the cost is much more efficient for the ternary structure than for the binary one.

Figures 30 and 31 compare the occupied area of the proposed ternary AND and OR gates with their similar binary counterparts. It is observed that the first proposed ternary model for AND gate (ANDT1) and the second proposed ternary model for OR gate (ORT2) have better performance in terms of area occupation.

In Ref. [7], if the inverting gate is removed from the end of NAND and NOR gates to obtain AND and OR gates, the number of cells and latency become 139 and 1.75 clock cycles (we calculate for Ref. [7]), respectively (Table 13). Therefore, the design in Ref. [7] can be compared with the proposed structures.

By comparing the structure in Ref. [7] and the proposed binary and ternary structures in the present study, it can be seen that both binary and ternary models proposed for AND

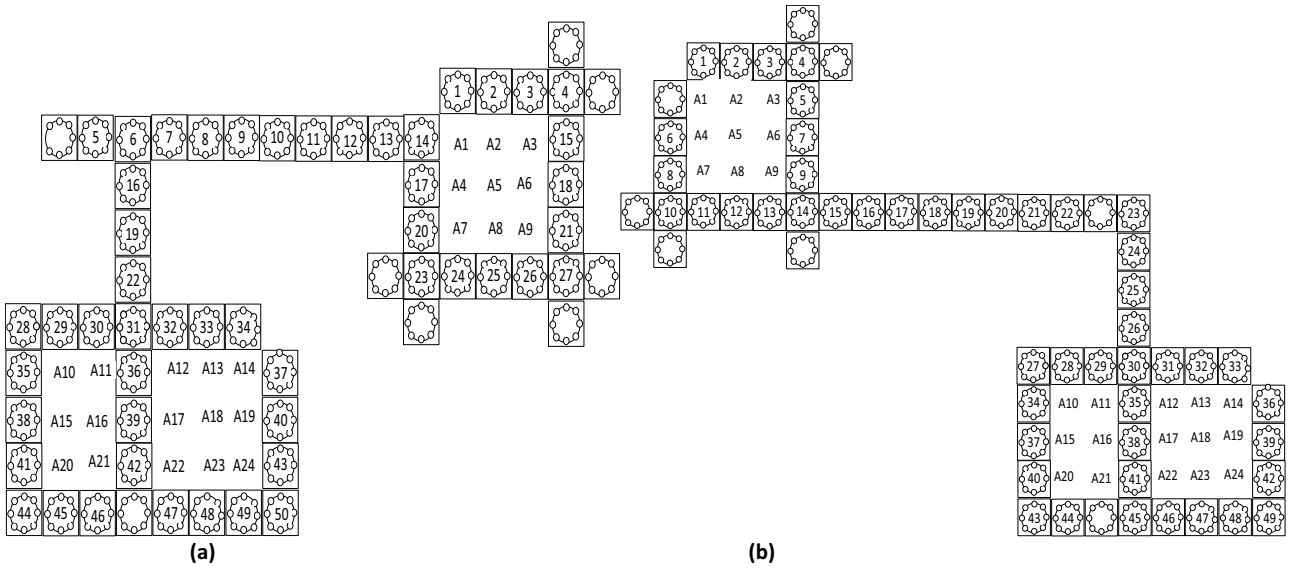


Fig. 28 Numbering QCA cells; **a** T1 and **b** T2

Table 7 Investigating cell omission defect for T1

Cell number	Impact on output	Cell number	Impact on output	Cell number	Impact on output	Cell number	Impact on output	Cell number	Impact on output
NO	45	NO	34	YES	23	YES	12	NO	1
NO	46	NO	35	YES	24	YES	13	NO	2
NO	47	YES	36	YES	25	YES	14	NO	3
NO	48	NO	37	YES	26	NO	15	YES	4
NO	49	NO	38	YES	27	YES	16	YES	5
NO	50	YES	39	NO	28	YES	17	YES	6
		NO	40	NO	29	NO	18	YES	7
		NO	41	NO	30	YES	19	YES	8
		YES	42	NO	31	YES	20	YES	9
		NO	43	NO	32	NO	21	YES	10
		NO	44	NO	33	YES	22	YES	11

Table 8 Investigating extra cell deposition defect for T1

Impact on output	Cell number	Impact on output	Cell number	Impact on output	Cell number	Impact on output	Cell number	Impact on output	Cell number
NO	21	NO	16	NO	11	NO	6	NO	1
NO	22	NO	17	NO	12	NO	7	NO	2
NO	23	NO	18	NO	13	YES	8	YES	3
NO	24	NO	19	NO	14	NO	9	NO	4
		NO	20	NO	15	NO	10	NO	5

Table 9 Investigating cell omission defect for T2

Cell number	Impact on output	Cell number	Impact on output	Cell number	Impact on output	Cell number	Impact on output	Cell number	Impact on output
YES	45	NO	34	YES	23	YES	12	NO	1
NO	46	YES	35	YES	24	YES	13	NO	2
NO	47	NO	36	YES	25	YES	14	NO	3
NO	48	NO	37	YES	26	YES	15	YES	4
NO	49	YES	38	NO	27	YES	16	NO	5
		NO	39	NO	28	YES	17	YES	6
		NO	40	NO	29	YES	18	NO	7
		YES	41	NO	30	YES	19	YES	8
		NO	42	NO	31	YES	20	NO	9
		NO	43	NO	32	YES	21	YES	10
		NO	44	NO	33	YES	22	YES	11

Table 10 Investigating extra cell deposition defect for T2

Cell number	Impact on output	Cell number	Impact on output	Cell number	Impact on output	Cell number	Impact on output	Cell number	Impact on output
NO	21	NO	16	NO	11	NO	6	NO	1
NO	22	NO	17	NO	12	NO	7	NO	2
NO	23	NO	18	NO	13	YES	8	YES	3
NO	24	NO	19	NO	14	NO	9	NO	4
		NO	20	NO	15	NO	10	NO	5

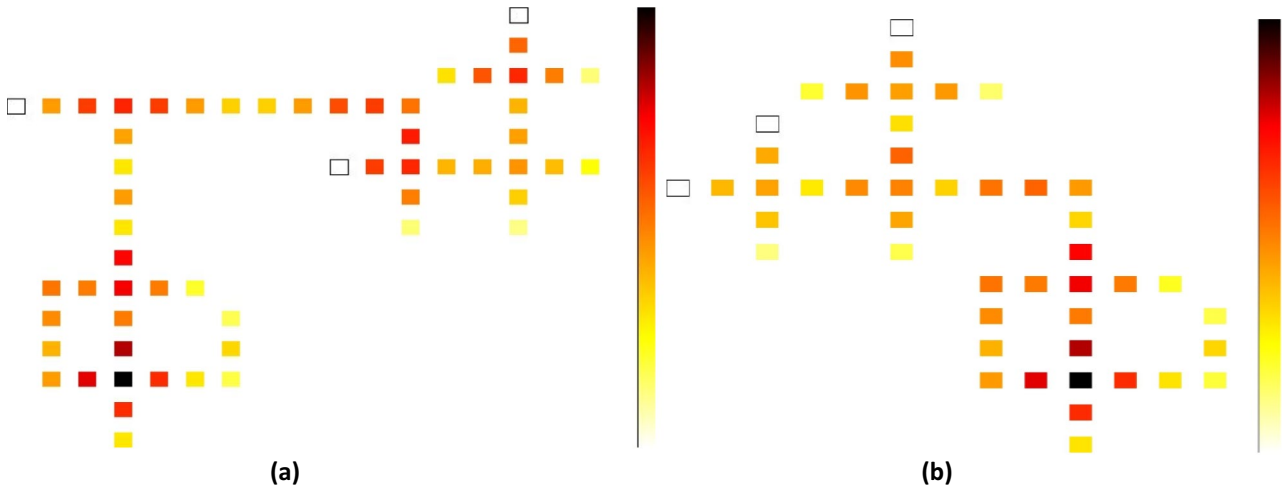


Fig. 29 Power dissipation map for the proposed binary PIM with 0.5 Ek; **a** B1 and **b** B2

Table 11 Power analysis result of proposed binary PIM basic cell and a comparative study of different QCA based memory and other architectures

Circuit	Technology (nm)	Avg. leakage energy dissipation (eV)			Avg. switching energy dissipation (eV)			Total energy consumption (eV)		
		0.5Ek	1EK	1.5EK	0.5EK	1EK	1.5EK	0.5EK	1EK	1.5EK
FinFET SRAM cell [32]	22	-	-	-	-	-	-	average energy:$3.72(MeV(\times 10^3 ev)/0.595(pJ(\times 10^{-12} J))$		
FinFET SRAM cell [33]	22	-	-	-	-	-	-	average energy:$16.875(MeV(\times 10^3 ev)/2.7(pJ(\times 10^{-12} J))$		
Presented RAM cell in [34]	18	0.02	0.06	0.1	0.09	0.08	0.07	0.11	0.14	0.17
Presented RAM cell in [35]	18	0.02	0.07	0.13	0.1	0.09	0.08	0.12	0.16	0.21
Presented basic PIM cell [36]	18	0.01443	0.04421	0.07858	0.05440	0.04611	0.03859	-	-	-
Proposed binary PIM basic cell (model1: B1)	18	0.01649	0.05025	0.09059	0.10054	0.08861	0.07666	0.11703	0.13887	0.16725
Proposed binary PIM basic cell (model2: B2)	18	0.01414	0.04142	0.07329	0.06675	0.05835	0.05023	0.08090	0.09977	0.12351

and OR gates are optimized in terms of cell count. However, the latency of the proposed binary structure is better than the latency in Ref. [7], and the latency of the proposed ternary structure is identical to the latency obtained in Ref. [7].

Additionally, the ternary structure can carry more information (three values) than the binary (two values) structure. This feature is an advantage of the ternary structure.

Figure 32 compares the proposed binary and ternary basic cells with the cell presented in Ref. [7]. It is observed that the occupied area of the first ternary model (T1) is optimized by 91.88% compared to the structure in Ref. [7], while in terms of the cell count, it has an acceptable performance just behind the second proposed binary structure. The first and second ternary models (T1 and T2) and the corresponding model in Ref. [7] are the same in terms of latency, while the proposed binary structures are 33.3% more efficient.

To summarize, the proposed ternary structure transfers more information, occupies less area, and needs fewer cells compared to the previously published binary designs. Therefore, the proposed ternary structure can improve the performance of the circuits.

Table 12 Comparison of the proposed basic PIM cells and previous designs

SRAM structure	Technology (nm)	Ternary/Binary (T/B)	Coplanar wire crossing	Complexity (cell count)	Occupied area (μm2)	Latency (clock cycles)	$\text{Cost}_{a\text{-}c} = \frac{occupiedarea(nm)}{complexity}$
RAM cell presented in [37]	18	Binary	yes	158	0.16	2×10^{-12} s	1.0126
RAM cell presented in [38]	18	Binary	NO	109	0.13	1.75×10^{-12}s	1.192
FinFET SRAM cell presented in [32]	22	Binary	-	9-Transistor	0.17	$\times10^{-9}$ s	18.88
PIM cell presented in [7]	18	Binary	NO	73	0.16	0.75×10^{-12}s	2.191
Proposed binary PIM cell (model1: B1)	18	Binary	NO	59	0.11	0.5×10^{-12}s	1.864
Proposed binary PIM cell (model2: B2)	18	Binary	NO	48	0.08	0.5×10^{-12}s	1.666
Proposed ternary PIM cell (model1: T1)	8	Ternary	NO	56	0.013392	0.75×10^{-12}s	0.2391
Proposed ternary PIM cell (model2: T2)	8	Ternary	NO	57	0.020085	0.75×10^{-12}s	0.352

Table 13 Comparison of the proposed novel PIM structures and previous designs

Model name	Type of structure	Number of cells	Occupied area (μm2)	Latency to main output (clock cycle)	Costa-$c = \frac{occupiedarea(nm)}{complexity}$	Fault tolerance (FT) (cell omission)	Fault tolerance (FT) (extra cell)
Presented in [7]	Basic cell	73	0.16	0.75	2.191		
	NAND	147	0.31	2	2.108		
	NOR	147	0.34	2	2.312		
First binary model	Basic cell(B1)	59	0.11	0.5	1.864	23.52%	40%
	AND(ANDB1)	145	0.27	1.5	1.862		
	OR(ORB1)	128	0.21	1.5	1.64		
Second binary model	Basic cell(B2)	48	0.087	0.5	1.812	57.89%	80%
	AND(ANDB2)	108	0.197	1.5	1.824		
	OR(ORB2)	120	0.29	1.5	2.416		
First ternary model	Basic cell(T1)	56	0.013392	0.75	0.239	52%	91.6%
	AND(ANDT1)	135	0.04797	2.25	0.355		
	OR(ORT1)	122	0.02808	1.75	0.23		
Second ternary model	Basic cell (T2)	57	0.02008	0.75	0.35	51.02%	91.66%
	AND (ANDT2)	109	0.026	1.75	0.247		
	OR (ORT2)	126	0.042	1.75	0.341		

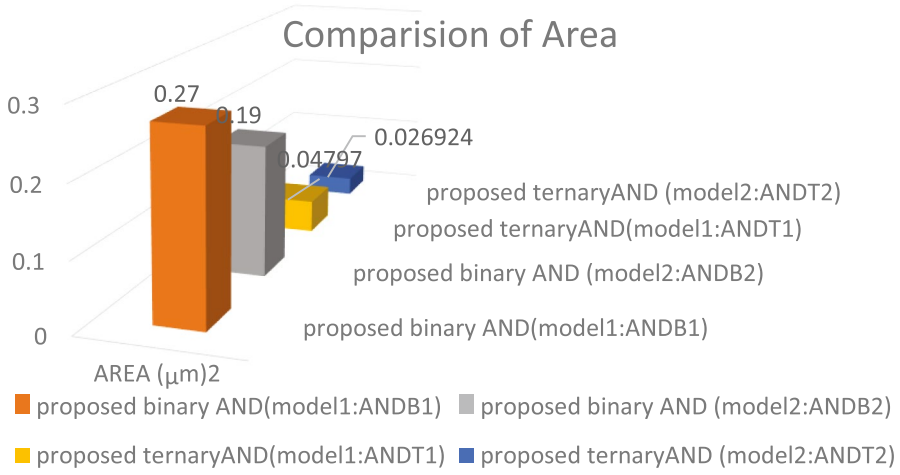


Fig. 30 Comparison of occupied areas of the proposed binary and ternary AND gates with Akers structure

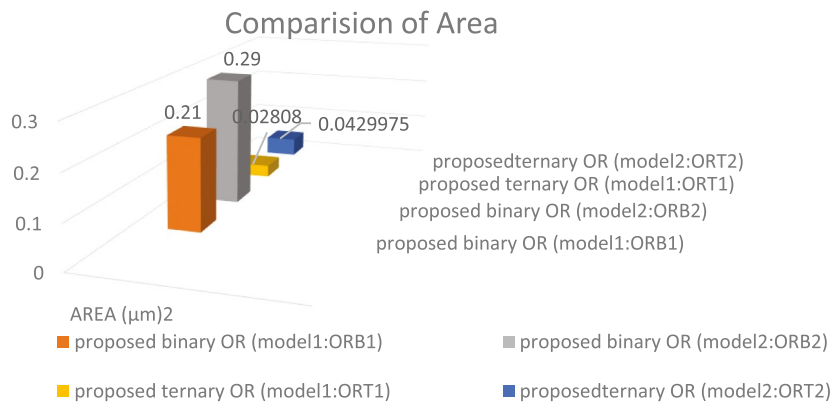
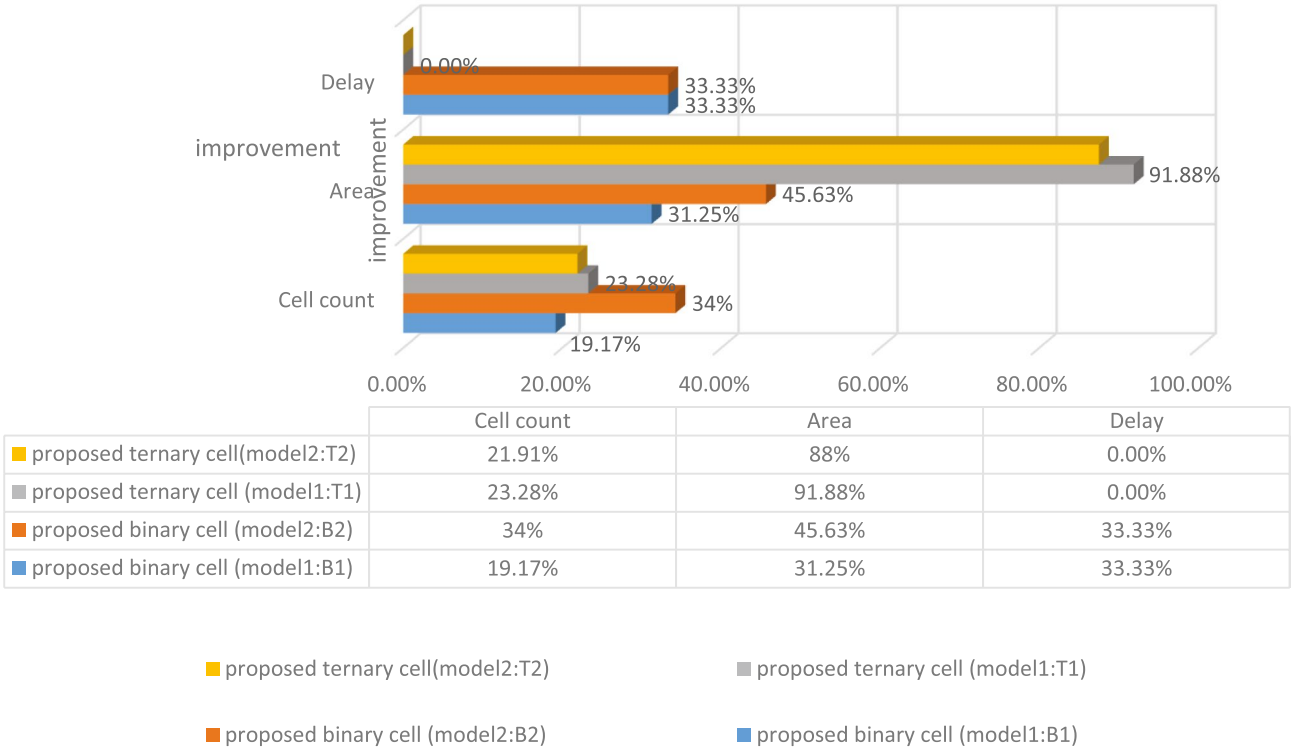


Fig. 31 Comparison of occupied areas of the proposed binary and ternary OR gates with Akers structure



	Cell count	Area	Delay
proposed ternary cell(model2:T2)	21.91%	88%	0.00%
proposed ternary cell (model1:T1)	23.28%	91.88%	0.00%
proposed binary cell (model2:B2)	34%	45.63%	33.33%
proposed binary cell (model1:B1)	19.17%	31.25%	33.33%

Fig. 32 Improvement in the proposed PIM cell structures compared to the results of Ref. [7]

7 Conclusion and Discussion

Many studies have attempted to change the configuration and cell placement of QCA circuits to improve FT, while this usually increases the number of cells and consequently the occupied area. To solve these issues, the present study proposed the use of ternary QCA and the obtained results confirm the correctness of the proposed scheme. Another novelty of this paper is the implementation of PIM architecture in ternary QCA. Moreover, the effect of fault on the PIM architecture and ternary QCA has not been investigated to date, so we investigated this effect in the present study. Although the effects of various faults in some binary QCA gates and simple circuits had been investigated earlier, no study was carried out so far for ternary QCA architectures. Accordingly, some ternary gates were designed and simulated using the proposed ternary PIM cell. Then, we compared the proposed ternary structures with their binary counterparts and the designs presented in other articles. The comparison of the results showed that the proposed ternary structures have better performance than similar structures and binary RAMs in terms of latency, occupied area, FT, and cost function (defined by the ratio of occupied area to the number of cells). Additionally, in terms of FT, the ternary structure performs better than the binary one due to its smaller dimensions. The shorter distance between ternary cells allows the transmission of the intercellular electrostatic effect from one cell to neighboring cells. Moreover, by deleting or adding a cell, fault occurrence is less likely. This has been confirmed by external electrostatic energy calculations. The results of comparing two proposed ternary structures showed that the first ternary structure, with the memory placed at the beginning of the circuit, has more optimal area, cost, FT and complexity than other structures. Moreover, AND and OR gates are universal gates, so other logic structures can be designed based on these gates. The energy consumption of some binary structures was simulated using QCA-Pro software. The results of energy analysis showed that the proposed binary basic cells (B1 and B2 models) are optimized by 8.3% and 33.33% (at 0.5 EK) and by 18.75% and 43.75% (at 1.5 EK) in terms of energy consumption. Subsequently, the XOR gate was designed using the Akers array and TQCA. The proposed ternary structure uses two common flip-flops for each input, and four multiplexers are used for the Akers array switches. The proposed structure was compared with the binary structure presented in [19] and the results showed an acceptable performance. Moreover, the result of comparison indicated that the proposed ternary structure is more optimal in terms of latency, occupied area, cost, and FT compared to the binary structures and has higher speed of processing and storing information. According to Table 13, the proposed ternary basic cell (T1)

improves area consumption by 91.875% compared to other previous designs. The second proposed ternary model for AND (ANDT2) improves area consumption by 91.322% compared to the results of other studies. The first proposed ternary model for OR (ORT1) optimizes area consumption by 91.76% compared to other studies. Moreover, the number of cells is reduced and TQCA can transfer more information. Therefore, the memory size is reduced, meanwhile, operations can be performed much faster with less cost, more information, and better fault tolerance. In future work, larger logical circuits can be designed in TQCA using these structures.

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Data Availability My manuscript has no associated data.

Declarations

Conflict of Interest All authors certify that they have no affiliations with or involvement in any organization or entity with any financial interest or non-financial interest in the subject matter or materials discussed in this manuscript.

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