Journal of Electronic Testing (2022) 38:371–379
https://doi.org/10.1007/s10836-022-06011-0

Efficient Design of Rounding Based Static Segment Imprecise Multipliers for Error Tolerance Application

D. Tilak Raju[1] · Y. Srinivasa Rao[2]

Received: 25 January 2022 / Accepted: 19 June 2022 / Published online: 4 July 2022

Abstract
Error-Tolerant applications regularly accomplish more data adaption. Approximate computing is one of the optimum strategies for data manipulation in several Error-Tolerant applications. It depletes circuit complexity and enhances area, power, and latency design parameters. Moreover, multiplication is a vital operation in Error-Tolerant applications. Existing Exact Multipliers are used in the approximate computing approach to expand the design parameters with fewer accuracy parameters in the present scenario. Hence, in this paper, new Rounding Based Static Segment Imprecise Multipliers (RBSSIM0, RBSSIM1) with and without Estimator Logic Circuit (ELC) are proposed to ameliorate the design and accuracy parameters. ELC removes lower-order important information in the input of bit length. Imprecise multiplication is executed using a rounding unit and barrel shifter in the proposed RBSSIM designs. These multipliers are synthesized and simulated using Cadence RTL compiler, Xilinx Vivado, and MATLAB with input bit sizes ranging from 8-bit to 32-bit. The results evidenced RBSSIM depletion area, delay, power, and energy by an average of 61.1%, 29.8%, 54.9%, and 64.2%, respectively, compared to existing imprecise multipliers. In addition to that, the proposed RBSSIM has better performance in terms of accuracy parameters. RBSSIM has improved NED, MRED, MED, and WCE on an average of 14.12%, 39.1%, 42.12%, and 24.21%, respectively. As a final point, RBSSIM provides higher SSIM and PSNR over the existing imprecise multipliers after including in the Error-Tolerant applications.

Keywords Rounding · Approximate Computing · Estimator Logic Circuit · Static Segment Method

1 Introduction

Digital Signal Processing (DSP) applications are required to perform Very Large Scale Integration (VLSI) architectures. High-performance modules are added to DSP designs to enhance the accuracy of such applications, which ameliorates overall performance related to general-purpose processors using the equivalent CMOS technology [2, 8].

The crucial purpose of filters in DSP architecture is in the composition of multipliers and adders. The filter performance is degraded if multipliers and adders are too deliberate or consume too much energy or if they exhibit poor accuracy or area overhead. A filter design based on a stochastic scientific model is applied to whittle the noise in the data. This mathematical paradigm's computation error tolerance has been employed to trade precision for energy consumption [17].

In DSP design, imprecise multiplication and addition have been successfully stayed out to get speed, power, and area benefits at the sacrifice of accuracy. Many studies were done in the multiplier design to achieve energy efficiency by trading accuracy in VLSI design using extreme voltage scaling, shorter least significant bit lengths, and the use of faulty building blocks [3, 5–7, 9–11, 16, 19]. Most recent developments in DSP design focused on adding and multiplying circuits with unbiased performance. Next, Tilak Raju and Srinivasa Rao [15] have analyzed fifty recent imprecise multipliers and finally concluded that there is no

Responsible Editor: S. T. Chakradhar

✉ D. Tilak Raju
tilakraju55@gmail.com

Y. Srinivasa Rao
srinniwasarau@gmail.com

[1] Department of Electronics and Communication Engineering, Vignan's Institute of Engineering for Women, Visakhapatnam, Andhra Pradesh, India

[2] Department of Instrument Technology, Andhra University, Visakhapatnam, Andhra Pradesh, India

one recent Imprecise Multiplier that provides better design, error, and quality parameters. Energy efficiency, space efficiency, high computational accuracy, and fast speed are four important design criteria for unbiased performance. The stable design structure is critical in reducing error in high-performance error-tolerance applications.

The conversion approach exhibits the efficiency of DSP applications through computational accuracy. For core arithmetic modules, high-precision algorithms are developed before including in the processor architectures. These restrictions are taken into account, efficient design of balanced architectural RBSSIM0 and RBSSIM1 are presented, and it is applied in Image Smoothing (IS), Gaussian Filter (GF), and Edge Detection (EDN) in error tolerance applications.

The k-bit segment in this proposed RBSSIM0 architecture may begin at 'n' or 'n-k' bit position of the n-bit input bit length, where k equals n/2. The Leading One Bit (LOB), which is positioned in higher or lower order segments, determines the k-bit static segment. Each segment output is applied to the rounding block, and the barrel shifter accomplishes multiplication. The k-bit segment in the proposed RBSSIM1 architecture may begin at 'n' or 'n-k' bit position of the n-bit input bit length, where k equals n/2. The LOB, which is positioned in a higher or lower order segment, is used to identify the k-bit static segment. The ELC ameliorates accuracy by refusing the lower order k-bit segment of input bit length if the high order k-bit segment is selected. One segment output is applied to the rounding block, and the barrel shifter accomplishes multiplication. This method outperforms earlier imprecise multipliers in terms of computational accuracy and design parameters. Further, analysis of accuracy parameters [1, 12] is completed in Error Distance (ED), Worst Case of Error (WCE), Normalized ED (NED), Mean Relative ED (MRED), and Mean ED (MED) for both the proposed RBSSIM0 and RBSSIM1 and existing imprecise multipliers. In addition, in this paper, IS [13], GF [7], and EDN [14] are incorporated with the proposed RBSSIM0 and RBSSIM1. Present imprecise multipliers are established and verified with six standard images [4] to examine the equivalent quality parameters [18] in terms of Structural Similarity Index (SSIM) and Peak Signal o Noise Ratio (PSNR).

The rest of the paper is organized as follows: a detailed discussion on imprecise multipliers in the second section. The proposed rounding static segment imprecise multiplier designs in the third section. The examination of results and applications in the fourth section. Finally, the conclusion is in the fifth section.

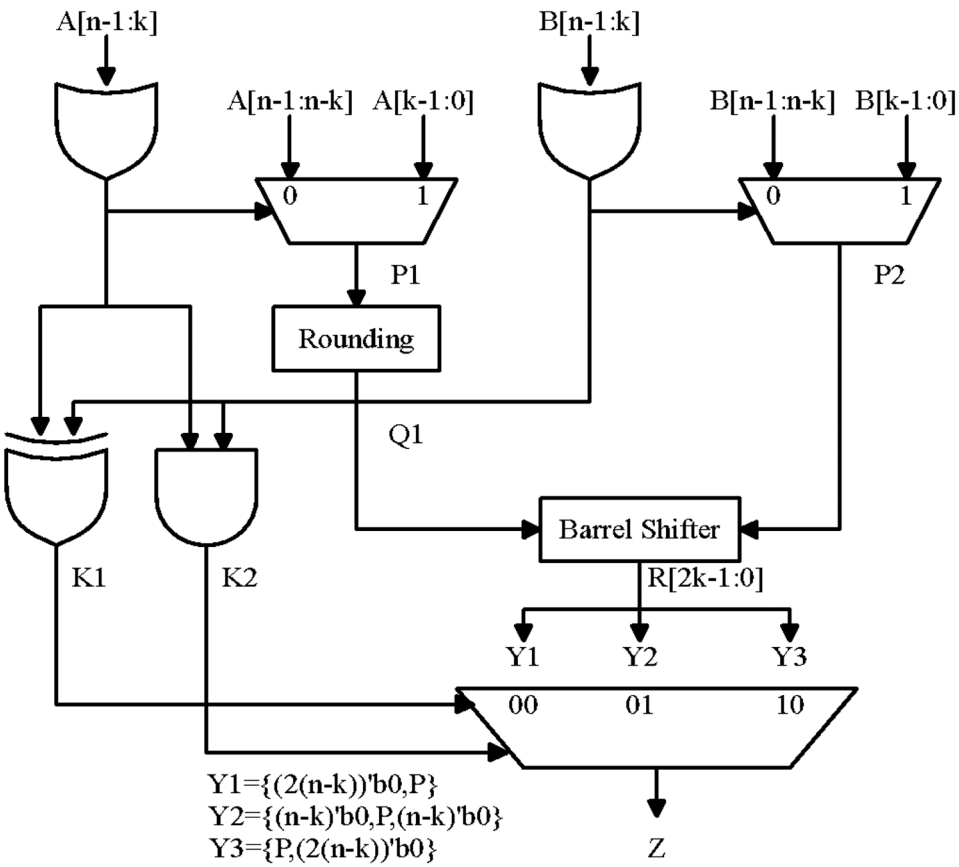

Fig. 1 Architecture of proposed RMSSIM0

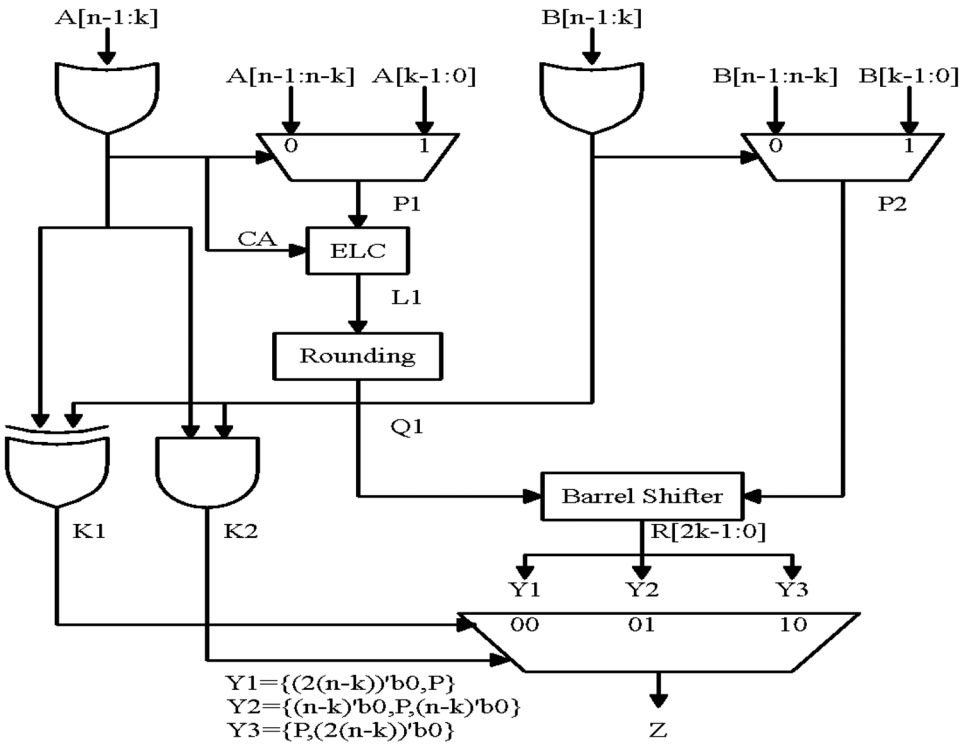

Fig. 2 Architecture of proposed RBSSIM1

2 State-of-the-Art Imprecise Multipliers

Kyaw et al. introduced an imprecise multiplier whose inputs bit length is split into exact and inexact sections, including a few MSBs and remainder LSBs accordingly [10]. Garg and Sharma introduced an imprecise multiplier by calculating inexact product AND-OR circuitry for limited LSBs [5]. Kulkarni et al. developed an accuracy customizable imprecise multiplier that includes the multiplier with EDC logic to produce inexact products with high accuracy without significant performance overhead [11]. Furthermore, when the error generated by the truncation approach for moving the MRED is pushed to zero, the LSB of the truncated input is set to one in the Dynamic Range Unbiased Imprecise Multiplier (DRUIM) [6]. Jothin and Vasanthanayaki designed Modified Static Segment Imprecise Multiplier (MSSIM) to ameliorate accuracy by denying lower-order important information of input bit length utilizing significance ELC [9]. Garg et al. have designed a LOB-based Imprecise Multiplier (LIM). It generated a final imprecise product that chooses m-bits from the n-bit input bit length based on LOB logic [7]. It improved accuracy parameters by precisely picking k-bits depending on LOB position logically. Garg and Patel designed Rounding Based imprecise Multiplier (RBIM), first rounding input bit length to the nearest power of two values and then accomplishing imprecise multiplication using a few shifters and adders [3]. The proposed RBIM multipliers significantly shrink the execution complexity and ameliorate energy competence but more error. Vahdat et al. have designed energy-efficient imprecise multipliers

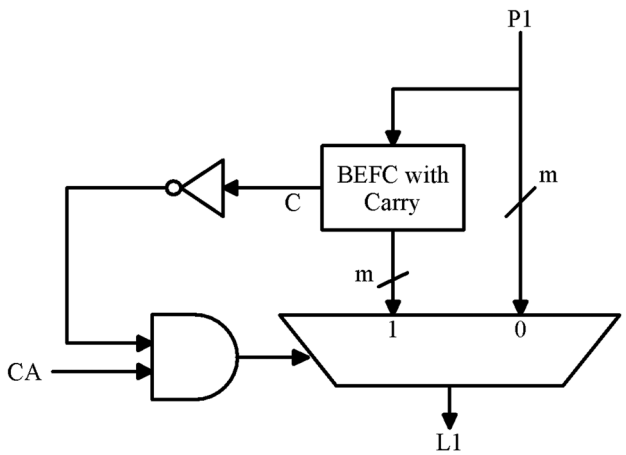

Fig. 3 Architecture of ELC

Table 1 Truth table of ELC

CA	P1 < 2^k-1 (C = Carry Output)	Output L1
0	×	P1
1	×	P1
1	0	P1 + 4
1	1	P1

Table 2 Hardware parameters of imprecise multipliers at 90 nm PDK

Bit-Width	Parameters	DRUIM [6]	MSSIM [9]	LIM [7]	RBIM [3]	RBSSIM0	RBSSIM1
8 bit	Area (μm^2)	1820	576	1247	1461	210	211
	Power (mW)	0.09	0.05	0.02	0.09	0.02	0.01
	Delay (ns)	4.25	3.11	5.24	6.54	1.49	1.48
	Energy (fJ)	382	155	104	588	298	149
16-bit	Area (μm^2)	3012	1939	3417	6739	572.97	572.97
	Power (mW)	31.12	180.1	190.4	30.12	25.65	25.64
	Delay (ns)	5.18	7.19	4.69	8.54	3.49	3.50
	Energy (fJ)	6781	1294	892	1281	895	897
32-bit	Area (μm^2)	5146	5730	8931	19,865	1563	1563
	Power (mW)	82.13	794.36	631.1	82.4	70.69	70.70
	Delay (ns)	5.54	13.99	6.99	12.41	5.45	5.44
	Energy (fJ)	45,000	11,113	44,113	10,225	3852	3846

utilizing the rounding and truncation method. It enhances accuracy and design parameters, but errors increase with the input bit length [16]. The literature review observed that present approximation multipliers endow with improved design parameters but not improved accuracy parameters.

3 Proposed RBSSIM Architectures

This section discusses two RBSSIM architectures procedures and the subsequently proposed architecture.

3.1 Proposed RBSSIM Algorithm

The procedure of the Proposed RMSSIM0 algorithm of two n-bit input bit lengths is given below:

(i) The higher-order or lower-order LOB k-bit segment output is selected for each n-bit input bit length.
(ii) One of the k-bit segment outputs is applied to the rounding block.
(iii) The barrel shifter is done by multiplying the k-bit segment and rounding output.
(iv) The final 2n-bit imprecise product is achieved by extension of the 2 k-bit.

The procedure of the Proposed RMSSIM1 algorithm of two n-bit input bit lengths is given below.

(i) The higher-order or lower-order LOB k-bit segment output is chosen for each n-bit input bit length.
(ii) One of the k-bit segment outputs is applied to the ELC block.

Table 3 Accuracy parameters of imprecise multipliers

Bit-Width	Parameters	DRUIM [6]	MSSIM [9]	LIM [7]	RBIM [3]	RBSSIM0	RBSSIM0
8-bit	MED	1.59e+04	1088.8	1.26e+04	5.01e+03	4.02e+03	4023.2
	MRED	6.07e-05	1.02e-06	2.36e-05	5.16e-06	5.36e-06	5.36e-08
	NED	0.25	0.23	0.21	0.08	0.09	0.08
	WCE	65,378	48,248	62,158	62,950	46,162	46,162
	ED	1.03e+09	70,798,444	823,636,708	325,889,758	261,606,432	261,606,432
16-bit	MED	4.96e+02	2.74e+03	5.08e+05	6.57e+06	2.04e+04	20,434
	MRED	1.22e-07	7.85e-07	3.70e-06	3.80e-06	6.38e-04	0.0006375
	NED	0.15	0.13	1.18e-04	0.18	0.48	0.49
	WCE	53,520	22,418	4.29e+09	3.75e+09	41,630	41,630
	ED	130,116,224	718,644,558	1.33e+11	1.72e+12	1.33e+09	1.33e+09
32-bit	MED	1.01e+04	2.66e+06	6.81e+05	1.27e+07	9.33E+03	9.33E+03
	MRED	2.79e-05	3.79e-06	3.80e-06	3.81e-05	2.27E-05	2.27E-05
	NED	0.21	6.20e-04	1.58e-04	0.29	0.23	0.22
	WCE	47,950	4.31e+09	4.42e+09	4.39e+08	42,036	42,036
	ED	2.62e+09	6.98e+11	1.78e+11	3.34e+12	606,751,018	606,751,018

Table 4 IS quality parameters of the imprecise multipliers

Parameters	DRUIM [6]	MSSIM [9]	LIM [7]	RBIM [3]	RBSSIM0	RBSSIM0
PSNR	28.8	28.7	27.9	27.8	29.1	29.8
SSIM	0.7371	0.7123	0.7122	0.7112	0.7912	0.8121

(iii) The output of ELC is applied to the rounding block.
(iv) The barrel shifter is done by multiplying the k-bit segment and ELC output.
(v) The final 2n-bit imprecise product is achieved by extension of the 2 k-bit.

3.2 Proposed RMSSIMs

The RMSSIM architectures improved the accuracy for all available input bit length combinations. On the other hand, the circuit complexity is reduced for the n-bit multiplier into the k-bit multiplier.

Figure 1 depicts the proposed n-bit RMSSIM0 architecture. The k-bit segment for each input bit length is picked from two available segments. One of the segment values is applied to the rounding block, and the output of the rounding block is the nearest power of two, and the rounding procedure is fully explained in [19]. Final 2 k-bit multiplication is done using a barrel shifter with the k-bit segment and rounding value. When both segments of input operands are from the lower m-bit segments, the multiplexer chooses Y1 when two segments are from the higher and lower ones of input operands or vice versa. When both segments of input operands are from the upper ones, the multiplexer chooses Y3. The 2 k-bit product generated by the multiplier may be expanded to a 2n-bit output by adding zeros. Proposed RMSSIM0 is decreased the circuit complexity, power, and delay.

The architecture of the proposed RBSSIM1 is illustrated in Fig. 2. The proposed RBSSIM1 is identical to RBSSIM0. The only change is one of the upper segment values applied to the ELC block before the rounding block. It is noted that the proposed RBSSIM1 enhanced accuracy and design parameters as well.

3.2.1 Algorithm for ELC

The ELC is depicted in Fig. 3, and the logic function is described in Table 1. The method explicates that the output function of the ELC is either P1 or Binary to Excess Four Code (BEFC) with output P1 + 4, which is determined by the control signals.

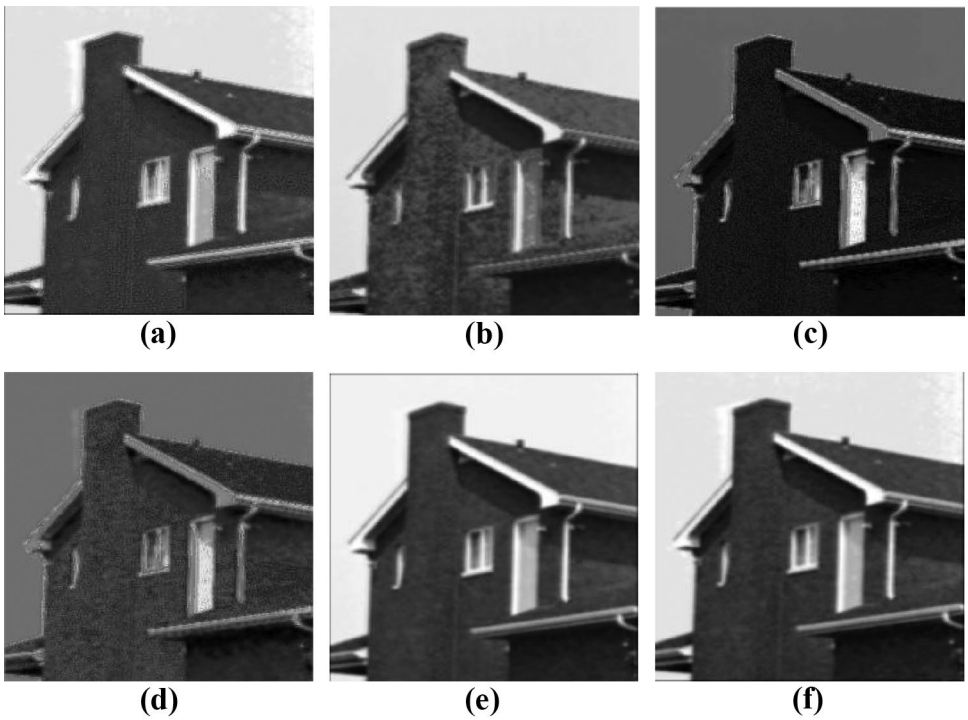

Fig. 4 House image by IS incorporated with: **a** DRUIM [6], **b** MSSIM [9], **c** LIM [7], **d** RBIM [3], **e** RBSSIM0, and **f** RBSSIM1

Table 5 GF quality parameters of the imprecise multipliers

Parameters	DRUIM [6]	MSSIM [9]	LIM [7]	RBIM [3]	RBSSIM0	RBSSIM0
PSNR	27.1	27.9	27.2	27.4	28.2	28.4
SSIM	0.7212	0.7102	0.7125	0.7224	0.7991	0.8001

4 Results and Discussion

This section begins with a hardware analysis, concluding with comparing the proposed and existing multipliers in terms of accuracy and quality.

4.1 Hardware Analysis

Hardware analysis of the proposed RBSSIM0 and RBSSIM1 with existing imprecise multipliers [3, 6, 7, 9] (DRUIM, MSSIM, LIM, and RBIM) with input bit lengths ranging from 8-bit to 32-bit are shown. The truncation length in the DRUIM architecture is six of the input bit length. The MSSIM truncation length, LAM, is half the input bit length, and the RBIM multiplier type is an unsigned RBIM multiplier. Imprecise multipliers are designed in Verilog and subsequently synthesized using Cadence RTL Compiler with 90 nm Process Design Kit (PDK) for hardware analysis.

Table 2 provides hardware parameters with respect to area, delay, power, and energy. From Table 1, it is shown that the proposed 8-bit RBSSIM0 and RBSSIM1 use limited energy compared to DRUIM, MSSIM, LIM, and RBIM. Further, the proposed 8-bit RBSSIM0 and RBSSIM1 are improved area, delay, and power on an average of 72.2%, 34.3%, and 52.4%, respectively, over DRUIM, MSSIM, LIM, and RBIM.

Furthermore, from Table 2, it is apparent that the proposed 16-bit RBSSIM0 and RBSSIM1 have minimized energy and also improved area, delay, and power on an average of 62.1%, 31.8%, and 61.8%, respectively, compared to DRUIM, MSSIM, LIM, and RBIM.

Similarly, it is shown that the proposed 32-bit RBSSIM0 and RBSSIM1 consume lesser energy and achieve a decrease in area, delay, and power on an average of 66.25%, 23.5%, and 45% compared to DRUIM, MSSIM, LIM, and RBIM.

4.2 Accuracy/Quality Analysis

This section shows the accuracy analysis in terms of MRED, MED, NED, WCE, and ED of the proposed RBSSIM0 and RBSSIM1. Furthermore, an evaluation of the proposed RBSSIM0 and RBSSIM1 and the existing imprecise multipliers on the accuracy parameters are discussed in [1, 12]. Finally, quality parameters analysis is completed in SSIM

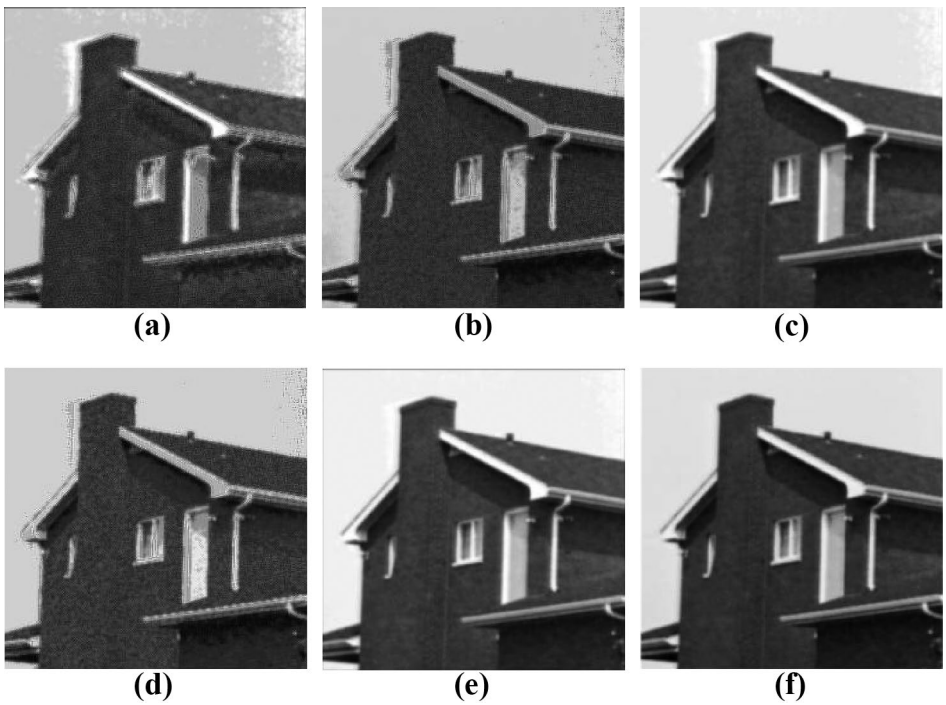

Fig. 5 House image by GF incorporated with: **a** DRUIM [6], **b** MSSIM [9], **c** LIM [7], **d** RBIM [3], **e** RBSSIM0, and **f** RBSSIM1

Table 6 EDN quality parameters of the imprecise multipliers

Parameters	DRUIM [16]	MSSIM [16]	LIM [19]	RBIM [15]	MRSSAM	MRSSM1
PSNR	20.1	20.4	21.2	20.1	24.2	24.3
SSIM	0.4122	0.4120	0.4201	0.4011	0.5122	0.5128

and PSNR by incorporating the proposed RBSSIM0 and RBSSIM1 and existing imprecise multipliers in the IS, GF, and EDN applications.

4.2.1 Accuracy Analysis

The accuracy of the proposed RBSSIM0 and RBSSIM1 is evaluated using accuracy parameters, and the associated accuracy parameters are compared with the existing imprecise multipliers. The imprecise multipliers are modeled in Verilog code simulated with one Lakh random input patterns, and accuracy parameters are generated in MATLAB. The simulation technique of generating the accuracy parameters is thoroughly explained in [16].

The accuracy parameters are computed and provided in Table 3 for the proposed RBSSIM0 and RBSSIM1 and existing imprecise multipliers. The simulation results show that the proposed RBSSIM0 and RBSSIM1 are minimized ED in the range of 32.25%—45.23% compared to DRUIM, MSSIM, LIM, and RBIM. From Table 3, it is also revealed that the proposed RBSSIM0 and RBSSIM1 are improved MRED, NED,WCE, and MED in the range of 74.1%—23.12%, 22.12%—11.09%, 52.21%—22.1%, and 82.12%—11.24%, respectively, compared to DRUIM, MSSIM, LIM, and RBIM.

5 Quality Analysis of IS/GF/EDN

In this section, IS, GF, and EDN are also simulated and compared to standard images for quality parameters analysis in terms of PSNR and SSIM. The pixel is produced in IS, GF, and EDN by performing convolution between the input image sub-matrix and the standard mask [7, 14, 16]. The efficiency of IS, GF, and EDN incorporated with the proposed RBSSIM0 and RBSSIM1 and existing imprecise multipliers is examined using the quality parameters.

The efficiency of IS, GF, and EDN incorporated RBSSIM0 and RBSSIM1, and existing imprecise multipliers are evaluated using the quality parameters. IS, GF, and EDN incorporated with these imprecise multipliers are analyzed and simulated using six standard images. The simulation method of quality parameters is fully explained in [16].

Table 4 illustrates the extracted quality parameters of IS incorporated with proposed and present imprecise multipliers. The simulation results show that IS incorporated with

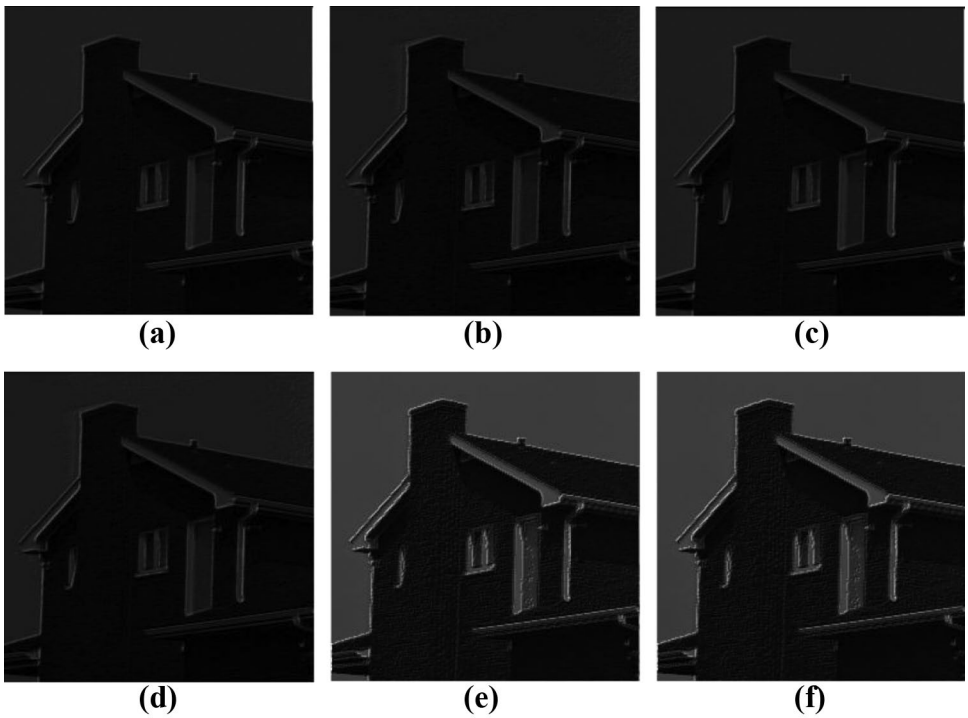

Fig. 6 House image by EDN incorporated with: **a** DRUAM [6], **b** MSSAM [9], **c** LAM [7], **d** RBAM [3], **e** RBSSIM0, and **f** RBSSIM1

the proposed RBSSIM0 and RBSSIM1 are improved SSIM and PSNR in the range of (9.2%—12.4%) and (3.4%—6.7%) over the IS incorporated with existing DRUIM, MSSIM, LIM, and RBIM. House images of the IS incorporated with different imprecise multipliers are shown in Fig. 4. The IS incorporated with proposed RBSSIM0 and RBSSIM1 gives higher image quality over the IS incorporated with the existing DRUIM, MSSIM, LIM, and RBIM.

Table 5 illustrates the retrieved quality parameters of GF incorporated with proposed and existing multipliers. The simulation results show that GF incorporated with the proposed RBSSIM0 and RBSSIM1 are improved SSIM and PSNR in the range of 0.2%—10.9% and1.7%—4.5%over the GF incorporated with existing DRUIM, MSSIM, LIM, and RBIM. House images of the GF incorporated with various imprecise multipliers are shown in Fig. 5. The GF incorporated with proposed RBSSIM0 and RBSSIM1 gives higher image quality over the GF incorporated with the existing DRUIM, MSSIM, LIM, and RBIM.

Table 6 represents the extracted quality parameters of EDN incorporated with proposed and existing imprecise multipliers. The simulation results show that EDN incorporated with the proposed RBSSIM0 and RBSSIM1 are improved SSIM and PSNR in the range of 18.1%—21.8%, and 12.8%- 17.3% over the EDN incorporated with existing DRUIM, MSSIM, LIM, and RBIM. House images of the EDN incorporated with various imprecise multipliers are shown in Fig. 6. The EDN incorporated with proposed RBSSIM0 and RBSSIM1 improves image quality over the EDN incorporated with the existing DRUIM, MSSIM, LIM, and RBIM.

6 Conclusion

This paper proposes two rounding-based static segment approximation multipliers (RBSSIM0, RBSSIM1). In RBSSIM0, the k-bit static segment is identified based on the LOB position, and one k-bit static output is applied to the rounding block and multiplication done by the barrel shifter. The final product is the multiplexer selected. Similarly, RBSSIM1 performs a multiplier function but adds one block as the ELC block, and the remaining operation is similar to RBSSIM0. The proposed RBSSIM0 and RBSSIM1 improved the area, delay, power, and accuracy parameters compared to prior approximation multipliers. Finally, IS, GF, and EDN are incorporated with the proposed RBSSIM0, and RBSSIM1 has experimented with quality parameters. It is shown through the simulation results that the IS, GF, and EDN incorporated with the proposed RBSSIM0 and RBSSIM1 achieved better quality parameters than the IS, GF, and EDN incorporated with recent multipliers.

Data Availability Data sharing is irrelevant to this article since no data sets are generated or analyzed throughout the small proposed and existing Imprecise Multipliers.

Declarations

Conflict of Interest I certify no actual or potential conflict of interest about this article.

Competing Interests The authors declare that they have no known competing financial interests or personal relationships that could influence the work reported in this paper.

References

1. Akbari O, Kamal M, Afzali-Kusha A, Pedram M (2018) CLA: A reconfigurable approximate carry look-ahead adder. IEEE Trans Circuits Syst II Express 65(8):1089–1093
2. Botella G, García C, Meyer-Bäse U (2013) Hardware implementation of machine vision systems: image and video processing. EURASIP J Adv Signal Process 152:1–4
3. Garg B, Patel S (2021) Reconfigurable rounding based approximate multiplier for energy efficient multimedia applications. Wireless Pers Commun 118(4):1–8
4. Garg B, Sharma G (2016) A quality-aware energy-scalable Gaussian smoothing filter for image processing applications. Microprocess Microsyst J 45:1–9
5. Garg B, Sharma G (2016) Low power signal processing via approximate multiplier for error-resilient applications. In Proc. of 11th International Conference on Industrial and Information Systems (ICIIS), IEEE, p 546–551
6. Garg B, Sharma G (2017) ACM: An energy-efficient accuracy configurable multiplier for error-resilient applications. J Electron Test 33(4):479–489
7. Garg B, Patel SK, Dutt S (2020) LoBA: a leading one bit based imprecise multiplier for efficient image processing. J Electron Test 36:429–437
8. Han J, Orshansky M (2013) Approximate computing: An emerging paradigm for energy-efficient design. In Proceeding of 18th IEEE European Test Symposium (ETS), IEEE European, p 1–6
9. Jothin R, Vasanthanayaki C (2018) High performance modified static segment approximate multiplier based on significance probability. J Electron Test 5:1–8
10. Kyaw KY, Goh W-L, Yeo K-S (2010) Low-power high-speed multiplier for error-tolerant application. In Proc. of IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC), IEEE, p 1–4
11. Kulkarni P, Gupta P, Ercegovac M (2011) Trading accuracy for power with an under designed multiplier architecture. In Proc. of 24th International Conference on VLSI Design, IEEE, p 346–351
12. Liang J, Han J, Lombardi F (2013) New metrics for the reliability of approximate and probabilistic adders. IEEE Trans Comp 62(9):1760–1771
13. Myler HR, Weeks AR (2009) The pocket handbook of image processing algorithms in C. Englewood Cliffs, NJ, and USA: Prentice-Hall
14. Strollo AGM, Napoli E, De Caro D, Petra N, Meo GD (2020) Comparison and extension of approximate 4–2 compressors for low-power approximate multipliers. IEEE Trans Circuits Syst I Regul Pap 67(9):3021–3034
15. Tilak Raju D, Srinivasa Rao Y (2021) Investigation of error-tolerant approximate multipliers for image processing applications. In Proc. of 3rd International Conference on Communication and Intelligent Systems (ICCIS 2021), Springer, p 1–14

16. Vahdat S, Kamal M, Afzali-Kusha A, Pedram M (2019) TOSAM: An energy-efficient truncation-and rounding-based scalable approximate multiplier. IEEE Trans Very Large Scale Integr VLSI Syst 27(5):1161–1173
17. Vasudevan M, Chakrabarti C (2014) Image processing using approximate Datapath units. In Proc. of IEEE International Symposium on Circuits and Systems (ISCAS), IEEE, p 1544–1547
18. Wang Z, Bovik A, Sheikh H, Simoncelli E (2004) Image quality assessment: from error visibility to structural similarity. IEEE Trans Image Process 13(4):600–612
19. Zendegani R, Kamal M, Bahadori M, Afzali-Kusha A, Pedram M (2017) RoBa multiplier: A rounding-based approximate multiplier for high-speed yet energy-efficient digital signal processing. IEEE Trans Very Large Scale Integr VLSI Syst 25(2):393–401

D. Tilak Raju received his B.E degrees in Electronics and Instrumentation Engineering from Andhra University, Visakhapatnam, India, in 2006 and M.E degrees in Electronics and Communication Engineering from Andhra University, Visakhapatnam, India, in 2009. He is a Research scholar at Andhra University. His areas of research include Approximate Multipliers, and Efficient design of Arithmetic elements. He has 10 years of teaching experience. He has supervised and guided various projects at undergraduate and postgraduate levels.

Y. Srinivasa Rao received his Ph.D. in Electrical Communication Engineering from Indian Institute of Science, Bangalore in 1998. At present, he is a UGC – PDF Research Fellow and also Professor and BOS Member in Instrument Technology Department, AU College of Engineering (A), Andhra University, Visakhapatnam, AP, India. He has more than 15 years of teaching and research experience and has published more than 102 research papers in the International Journals and also presented some of them in International Conferences. He was in Eritrean Institute of Technology, Asmara, N.E. Africa for one year on academic assignment. He was a Visiting Researcher, EEE Department, Nanyang Technological University, Singapore in 2013. He was a Visiting Research Scholar at I Shou University, Kaohsiung City, Taiwan in 2013-2014. He received the SAARC Award in 2013, ''Research Award'' in 2012 from University Grants Commission, India, ''Outstanding Paper Award'' at the Emerald Literati Network Awards for Excellence 2008, England (UK), Five ''Best Paper Awards'' at International Conferences (2012, 2011 and 2007), ''Vignan Pratibha Award – 2006'' for Research from Andhra University, ''Science Researcher for Asia – Pacific Region'' Award in 2005 by UNESCO and Australian Expert Group in Industry Studies (AEGIS) at the University of Western Sydney (UWS), and ''Young Scientist Award'' from Department of Science and Technology, Government of India in 2002.