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Editorial

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This issue has seven articles. The topics discussed are memrister technology, failure probability, hardware security. wafer-level test, software test and verification, and approximate circuits for error-tolerant application.

Memristor was first described by Leon Chua in 1971 as fourth circuit element besides resistor, capacitor, and inductor. Lately, it has been receiving renewed interest. The first two papers in this issue discuss memristor devices.

The first paper gives the design of an op-amp using memristor. Authors examine various performance characteristics and compare with conventional designs. Contributors of this work are Parlar and Almali from Van Yuzuncu Yil University, Van, Turkey.

The second paper examines the use of memristor-based random access memory (RAM) for neuromorphic computing circuits, showing economy of power and delay over the conventional alternatives. The authors are Yadav, Chakraborty and Sengupta from Indian Institute of Technology Kharagpur, India, Thangkhiew from Indian Institute of Information Technology Guwahati, India, and Datta and Drechsler from Deutsches Forschungszentrum für Künstliche Intelligenz (DFKI) Bremen, Germany.

The third paper analyzes the failure probability of circuit (FPC) caused by faults. Accuracy requires that signal correlations due to reconverging fanouts be considered, which increases the computation cost. This work supplies various tradeoffs between accuracy and cost. The authors are Cai, He, Wu, J. Wang, W. Wang and Yu from Changsha University of Science and Technology, Changsha, China.

Next is a hardware security paper. Sivabalan and Murugan from Kalasalingam Academy of Research and Education, Srivilliputtur, Tamil Nadu, India, propose an FPGA-based architecture of advanced encryption standard (AES) for data security. Keys are obtained from efficient pseudorandom number generators (EPRNG). The security architecture is analyzed under hazards like side channel attacks, denial of service, offline password guessing attack, and others.

In the fifth paper, wafer-level testing is addressed by Huang,Dai, Dou, Wu and Li from Central South University, Changsha, China, and J. Liu, Y. Liu and Chen from 43rd Research Institute China Electronics Technology Group Corporation, Hefei, China. Their work shows that a flexible loading device can effectively limit radial rotation of the loading process and ensure a stable loading of wafers into the test system. They supply mathematical models for stable pressure and mechanical performance characteristics of the system.

Most electronic systems today consist of hardware and software, and software test is an integral part of the system testing. However, the two subsystems follow different test methodologies. Software test resembles hardware design verification. In the past, *JETTA* has focused on hardware test. Nevertheless, we believe that a segment of our readers would have a need for, as well as an interest in, the software aspects of testing. Therefore, we should not neglect the software aspect.

The sixth paper in this issue provides a method for software test generation. Like hardware, test complexity can be a problem. But unlike hardware, there are no accepted fault models. The emphasis in this paper is to cover paths in the program under test, or verification. Contributors of this work are Arasteh and Hosseini from Istinye University, Istanbul, Turkey. Interestingly, they call their test generation system Traxtor, the name of a popular football team in the historical city of Tabriz.

The final contribution of this issue comes from Chandaka of Vignan's Institute of Information Technology, Andhra Pradesh, India, and Narayanam from Jawaharlal Nehru Technological University, Kakinada, India. Here, in

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the design of an approximate computing circuit, which is a multiplier, the quest for reducing area, power and delay continues. Of course, the application of image processing allows relaxation from absolute accuracy. This latest design of a modified Wallace tree multiplier can save up to 28-percent on power, while further extensions for real time image processing are also proposed in the paper.