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Design of Power Gated SRAM Cell for Reducing the NBTI Effect and Leakage Power Dissipation During the Hold Operation

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Abstract
Along with the advancement of technology, Negative bias temperature instability (NBTI) has now been considered a severe reliability threat in modern processors causing the device to deteriorate over time. SRAM-based architectures within the memory array are very much prone to the NBTI effect. Since SRAM cells are composed of cross-coupled inverters, one of the PMOS transistors will always be under constant stress and heavily degraded by NBTI, resulting in an increase in threshold voltage and degradation of SNM and performance of SRAM. Similarly, as one the PMOS transistor is always ON, so there will be a leakage power from V_{DD} to the ground. In this paper, we have proposed a power gated SRAM architecture to reduce the NBTI effect and standby leakage power of a 4×4 SRAM array. The proposed gated logic is introduced during the hold state of the SRAM operation. So both the PMOS of the SRAM cell will be OFF during this period and will get sufficient time to relax from NBTI stress. The simulation result shows using our proposed approach overall, 30.41% NBTI-related V_{th} degradation can be saved and considering only the standby mode, 96.24% NBTI-related degradation can be minimized compared to the conventional SRAM design. Moreover, 79.10% leakage power can be reduced over the conventional design using the proposed approach.

Keywords NBTI · SRAM · Reliability · Power gating · SNM

1 Introduction

NBTI effect has become a serious reliability issue in current times with the constant scaling of transistor feature sizes, affecting the PMOS device's lifetime [1]. NBTI arises whenever a negative gate voltage ($V_{gs} = -V_{DD}$) is applied to the gate of the PMOS device [2, 3]. Due to this negative gate voltage, some traps are created at the Si/SiO2 interface. Because of these trap charges, the threshold voltage increases, and the drain current reduces [4]. The performance of the device degrades as the threshold voltage increases and finally leading the circuit to fail. However, when logic '1' is applied, a few interface traps can be eliminated, and NBTI stress is partially recovered [5, 6]. This put the device into recovery mode. NBTI poses a significant challenge on the memory arrays, especially SRAM-based architectures [7]. Since SRAM cells are made of cross-coupled inverters, each memory cell always stores either '0' or '1' all the time. Therefore, one of the PMOS transistors will be always ON. In other words, we can say one of the PMOS transistors will be always under constant stress and heavily affected due to NBTI. Due to the constant stress, the threshold voltage (V_{th}) of the PMOS transistor degrades over time which eventually causes degradation in the SRAM cell stability, static noise margin (SNM), performance, as well as the possibility of functional failure over the lifetime of the circuit [8]. In SRAM, such degradation can be very much significant, whereas MOSFET's relative strengths determine device stability. With time the stability degradation becomes even more critical as a result of the decreased guard-banding with the process variations under the worst-case scenario. As

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all modern processor cores are made up of multiple SRAM-based architectures, it is very significant to minimize the NBTI effect on such architectures to increase their lifetime.

Different work has been done to minimize the NBTI related degradations in SRAM-based circuits [7, 8]. Previously, the recovery boosting technique was suggested to mitigate the impact of NBTI on SRAM by putting both of the PMOS transistors into recovery mode [9]. The fundamental concept behind the recovery boosting is to increase the memory node voltages to bring all the PMOS transistors into the recovery state. It is possible to do this by increasing the ground and bitline voltages to V_{DD}. But recovery boosting technique is only applicable in recovery boost mode. In this paper, a power gated SRAM architecture is proposed to compensate the NBTI degradation of a 4×4 SRAM array during the entire hold operation by gating the V_{DD} in the hold operation. During the hold operation, SRAM stores either '1' or '0' for a long amount of time. So, one of the PMOS transistors will always be under constant NBTI stress. Similarly, as one of the PMOS transistors is always ON, there will be a leakage power from V_{DD} to the ground. In our proposed design, we have controlled the row decoder of SRAM so, during hold operation, when the word line is turned OFF, we can power gated the V_{DD} for the entire row of the SRAM architecture. By using this technique, we can control eight SRAM cells at a time. As a result of this, both of the PMOS transistors will be OFF during the entire hold operation. So, NBTI stress can be reduced, and degradation of SNM can be improved. One advantage of our proposed approach compared to the recovery boosting technique is that recovery boosting can't be applied on normal SRAM operations is only applicable on recovery boost mode, whereas, using the proposed approach entire hold operation may be utilized to minimize the NBTI effect. And using our approach, the leakage power flowing from V_{DD} to the ground during the hold operation can also be minimized. Simulation is performed in UMC 28nm technology [10].

The following summarized the contribution of the work:

- In this paper, a power gated SRAM architecture is presented to reduce the NBTI degradation and leakage power of a 4×4 SRAM array by power gating the V_{DD} during the hold operation. Using this approach, eight SRAM cells will be power gated at a time. So, for a significant amount of time, both of the PMOS of eight SRAM cells will be in the recovery state. The simulation result show, overall 30.41% NBTI-induced Vth degradation can be reduced using the proposed approach over the conventional design.
- However, considering only the standby time, using the proposed approach, near about 96.24% NBTI-related V_{th} degradation can be minimized.
- Using the proposed approach, the degradation rate of the read SNM is reduced by 28.74% compared to the conventional design.
- Moreover, the leakage power flowing from V_{DD} to ground in the hold operation can also minimize using the proposed approach. The simulation result shows near about 79.10% leakage power can be saved using the proposed power gating approach.
- In terms of area overhead, the proposed design consumes a little more area, i.e. 1.78% more area than the normal SRAM design.
- In the proposed design, SRAM will perform read and write operations similar to the conventional SRAM. Whereas in the case of hold operation, SRAM will be power gated, and output Q and Q_B will be '0' at that time, and after the hold operation, previous values will be restored in the memory. So the logic and functionality will be unaffected.

The remaining sections of the paper are arranged as follows. In Sect. 2, related work is described. Section 3 represents the NBTI effect and its impact on the SRAM cell. A detailed description of our proposed approach is presented in Sect. 4. Section 5 contains simulation, results, and associated discussions. Finally, Sect. 6 summarizes the conclusion of the proposed work.

2 Related Work

Previously different work has been proposed to alleviate the NBTI effect in the SRAM-based architectures. In Siddiqua et al. [9] the author has proposed the recovery boasting technique to reduce the impact of NBTI on the SRAM array. Using the recovery boasting, both of the PMOS transistors can be placed into the recovery state, so these are less affected by NBTI stress. They have shown using the recovery boasting technique, 56% improvement can be observed in terms of static noise margin while the structure has imposed little power and area overhead. However, this approach is only applicable to the recovery boosting mode. So for a small amount of time, the transistors will be in the recovery state. In Faraji et al. [11] author has addressed the long-term BTI aging effect that degrades SRAM stability and proposes an adaptive body biasing technique (ABB) that mitigates the BTI effect and enhances stability and performance of SRAM with low area overhead. They have shown using their proposed ABB technique, read SNM degradation, hold SNM degradation, write margin degradation, write delay and read delay are reduced by 12.24%, 6.85%, 2.16%, 32.61%, 28.68% respectively. Moreover, along with the reduction of the BTI effect using this approach, a considerable amount of

leakage power is also saved. However, the design imposes some extra area overhead. In Shah et al. [12], the author has suggested an on-chip body biasing circuit to mitigate the degradation caused by NBTI. Using this approach, a significant amount of NBTI-related performance degradation in the SRAM can be minimized, and the figure of merit (FOM) of the SRAM cell is improved by 17.96%. However, this analysis has not reported the power consumption and area estimation.

In Kumar et al. [13] the author has discussed the significance of the NBTI degradation on the read stability of the SRAM. They have also used the data flipping approach to combat the NBTI effect by periodically changing the contents of SRAM, thus assuring the PMOS transistors are susceptible to alternative stress and relaxation that allows the threshold voltage to have the dynamical recovery. Using their technique, 30% read stability in terms of SNM can be restored. Though the author has shown hardware implementation of their proposed cell flipping in the SRAM cells and discussed the data read and write operations in the cell flipping cache, the estimation of area and power consumption were not presented in the paper. In Ahmed et al. [14] the author has presented an on-chip NBTI degradation monitoring scheme in SRAM to predict the NBTI-induced cell failures. Using this approach, the gradual degradation of PMOS transistors in individual SRAM can be controlled without affecting its performance in normal operation. Therefore, under NBTI degradation, the error in limited noise immunity can be prevented. Hence, using this approach, cell failure can be identified before occurrence so the SRAM can operate correctly. In Bansal et al. [15] the author has presented an analysis of the impact of PBTI and NBTI on the stability of SRAM during the write and read operations under worst-case conditions. They have analyzed the trade-off between short-term and long-term stability to obtain the optimal six-sigma confidence in functionality. They have shown depending on technology, higher V_{DD} might be required to accomplish the necessary stability during the lifetime of IC. In Chenouf et al. [16], the author has suggested a transistor sizing approach to reduce the NBTI degradation in the 6-T SRAM circuit. In this approach, initially, the access transistors are sized for improving the hold stability and later sizing the other transistors based upon the cell-ratio and pullup ratio to mitigate the NBTI degradation and improve the read stability and write-ability. However, sizing the transistors can increase the power consumption of the SRAM cell. In [17], an aging monitoring scheme was presented to periodically detect the over-aging in the SRAM memory cell and the sense amplifier module. In their approach, a simple, low-cost differential ring oscillator is utilized to monitor the degradation of transistors. So, the over-aged transistors are identified, and proper reliable operation is maintained. Moreover, the normal operations of the memory cell are not altered. However, using this approach, there will be some increment of power consumption and total area overhead.

3 NBTI Effect and Impact on SRAM Cell

3.1 Overview of NBTI

In recent times NBTI effect has emerged as a serious aging concern [18]. It's been a research topic for more than 40 years, and it has received a lot of coverage in the recent decade because of the difficulties it faces with new semiconductor technologies [19, 20]. Whenever a negative bias (logic '0') is fed to the PMOS transistor, Si-H bonds break, forming interface traps at the interface [21, 22]. As a result of these traps, the device's threshold voltage (V_{th}) rise over time, reducing the device's speed. However, when the positive voltage (logic '1') is applied to the PMOS transistor's gate, some of the interface traps are annealed [23, 24]. Therefore, the stress phase ends, and the threshold voltage (V_{th}) decreases. If a PMOS transistor experiences constant stress, referred to as static NBTI. When both the stress and recovery phase exists during the active period, referred to as dynamic NBTI [25, 26]. The physics behind the interface traps generation due to the effect of NBTI is described in the reaction-diffusion (R-D) model [27].

$$\begin{aligned} Static\ :\ \Delta V_{th} &= A\left((1+\delta)t_{ox} + \sqrt{C\left(t-t_0\right)}\right)^{2n} \\ Dynamic\ :\ \Delta V_{th} &= \left(\sqrt{K_V^2 T_{clk}\alpha}/\left(1-\beta_t^{1/2n}\right)\right)^{2n} \end{aligned} \tag{1}$$

Based on the reaction-diffusion (R-D) mechanism, a real-time NBTI model was presented in Bhardwaj et al. [28], with static and dynamic terms defined by the Eq. (1), where A, β_t, and K_v are functions of stress time, temperature, voltage, and signal probability. Table 1 shows their respective values. Here, α denotes the proportion of time that a PMOS transistor is stressed. t_e refers to the effective oxide thickness. ϵ_{ox} refers permittivity of the semiconductor, which is $4 \times 8.854e^{-21}$ F/nm in silicon. The time duration of the stress signal is represented by T_{clk}. ξ_1 and ξ_2 represent back diffusion constants. Their respective values are 0.95 and 0.5. The value of K is $8 \times 10^4 C^{-0.5} nm^{-2}$. The value of activation energy, E_a, is 0.49

Table 1 Parameters for static and dynamic NBTI model

K_V	$\left(\frac{qt_{ox}}{\epsilon_{ox}}\right)^3 K^2 C_{ox}(V_{gs}-V_{th})\sqrt{C}exp\left(\frac{2E_{ox}}{E_0}\right)$
A	$\left(\frac{qt_{ox}}{\epsilon_{ox}}\right)^{1/2n}\sqrt{K^2 C_{ox}(V_{gs}-V_{th})\left(exp\left(\frac{E_{ox}}{E_0}\right)\right)^2}$
β_t	$1-\frac{2\xi_1 t_e + \sqrt{\xi_2 C(1-\alpha)T_{clk}}}{(1+\delta)t_{ox}+\sqrt{Ct}}$
C	$T_0^{-1} exp\left(\frac{-E_a}{KT}\right)$

eV. The value of the variable T_0 is $10e^{-8}s.nm^{-2}$. The value of n is 1/6 and 1/4 for H_2 diffusion-based model and H-based model, respectively. The lateral electric field, denoted by E_0, has a value of 0.335 V/nm. The value of the variable δ is 0.5.

3.2 Impact of NBTI on SRAM Cell

SRAM-based architectures are very susceptible to the NBTI effect [7, 9]. Since the SRAM cells are made up of cross-coupled inverters, so at a time one of the PMOS transistors has an input value '0' at the gate. As a result, one of the PMOS transistors is constantly under stress and severely degraded by NBTI. Fig. 1 shows because of the cross-coupled configuration of the SRAM when Q becomes '0', the M2 transistor is under NBTI stress, and when Q becomes '1', the M1 transistor is under NBTI stress. NBTI causes a shift of threshold voltage (V_{th}) of the PMOS transistor. This shift in threshold voltage (V_{th}) deteriorates the performance of the SRAM and shifts the VTC curve, which results in the degradation of SNM. The SNM refers to the stability indicator of SRAM and is defined as the maximum amount of voltage noise that can be allowed until the contents of the memory are flipped [11]. In the case of SNM, the threshold voltage shift could result in an increase in the time needed for writing and reading the contents of the cell. Since an SRAM cell might store the same content for a long interval of time, there could be asymmetric FET degradation [12]. So, if the voltage applied to the PMOS gate is switched on a regular basis, dynamic recovery of the threshold voltage (V_{th}) can occur, saving a considerable amount of performance.

NBTI affects normal SRAM operations namely, hold, read, and write.

3.2.1 Hold

During the hold operation, data is stored in the feedback inverter pairs. At that time, WL=0 and the SRAM cells are isolated from bit lines. During this period, one of the pull-up transistors (M1 or M2) experiences NBTI stress. Since data were kept for a long time, these transistors are heavily degraded due to NBTI, and the SNM degrades.

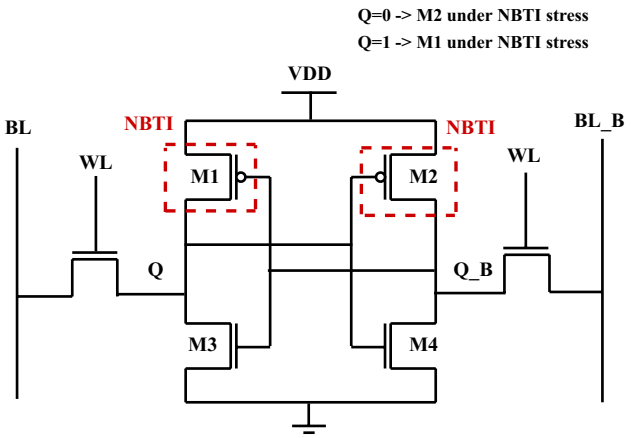

Fig. 1 Schematic of 6T-SRAM cell illustrating the degradation in M1, M2 transistors because of NBTI stress

3.2.2 Read

For the read operation, bit lines (BL, BL_B) are acting as output. Here, stored data is collected from memory and transferred to the bit lines via access transistors. The sense amplifier is attached to the bit lines and acts as a comparator. The sense amplifier output determines which data ('0' or '1') is stored in the memory. A worst-case scenario in the read operation might be occurred due to static stress. If the data kept the same value for a long time, it would result in NBTI induced V_{th} shift on pull-up transistors. As a result of NBTI stress, the pull-up transistors become weak, and it affects the read stability of SRAM. As a result of the increase in threshold voltage the read access time, and read SNM degrades.

3.2.3 Write

During the write operation, bit lines act as input. Here, data is written into the memory with the help of write enable from the write driver circuit. For a successful write operation, the memory node should switch in the time when word line and write enable is high. But due to the NBTI stress on PMOS transistors, the threshold voltage increases over time which affects the write access time of SRAM. However, different studies have found that write margin is marginally improved due to NBTI.

3.2.4 Static Noise Margin (SNM)

The main concern of NBTI on SRAM cells is that it degrades the SNM of SRAM [12, 29]. SNM is represented by the minimum amount of dc noise available at the nodes to change the phase of the cell is a measure of the SRAM cell's stability. SNM is calculated as the side of a maximum square that can be embedded within the VTC curves of cross-coupled inverters. In SRAM, SNM can be studied mainly in two modes, read SNM and hold SRAM. According to the various studies, read SNM degradation due to NBTI effect is more significant in SRAM cells than hold SNM degradation [11, 13, 15]. In our analysis, we are focusing on the read SNM degradation due to the NBTI effect. Different NBTI models on SNM have been proposed previously. In [30], an analytical model is presented for the read SNM calculation as a function of the shift in NBTI-induced threshold voltage (ΔV_{th}).

$$SNM(\Delta V_{th}) = SNM(Initial) + c \times \Delta V_{th} \quad (2)$$

This model is presented in Eq. (2), where SNM(ΔV_{th}) is the degraded SNM due to the NBTI-induced change in Vth,

SNM (Initial) is the initial SNM of the SRAM. c is the fitting constant; its value is -0.2893. And ΔV_{th} represents the change in threshold voltage caused by NBTI. In this work, we have used this analytical model to analyze the read SNM degradation due to the change in V_{th}.

4 Design of the Proposed NBTI-Aware Low Leakage Power Gating Design of 4 × 4 SRAM Array

The proposed methodology is based on power gating the supply voltage (V_{DD}) during the hold operation in order to mitigate NBTI degradation and also minimizes the standby leakage power. During the hold operation of the SRAM cell, either '0' or '1' is stored in the memory, so that means at a time, one of the two PMOS transistors will be ON. And if the hold operation lasts a long period of time, these PMOS transistors will be under constant stress and will be heavily degraded due to NBTI. As a result of these NBTI stress, threshold voltage (V_{th}) increases over time, which finally results in degradation in static noise margin (SNM) and the performance of SRAM. Similarly, during the hold operation, as one of the PMOS transistors is always ON, So, there will be a constant leakage power flowing from V_{DD} to GND. In our proposed design, when the SRAM performs hold operation, the supply voltage (V_{DD}) will be power gated; as a result, both of the PMOS transistors will be OFF during the hold operation. That means these PMOS transistors will undergo the recovery state and will get sufficient time to relax from NBTI degradation. In this design, SRAM performs the write and read operations like the conventional SRAM, and when the WL becomes '1', the previous value has been restored in the memory. Using this approach, NBTI oriented threshold voltage (V_{th}) degradation can be minimized, and also SNM and performance of the SRAM can be saved. Moreover, as both of the PMOS transistors are OFF throughout the hold operation, a significant amount of leakage power can be saved. And these characteristics make this approach superior compared to many other SRAM designs. In this paper, we have used an array of 4 × 4 SRAM cells for simulation. Figure 2 presents the block diagram of a normal 4 × 4 SRAM array.

Figure 3 represents the block diagram of the proposed power gated design in the array of 4 × 4 SRAM cells. The

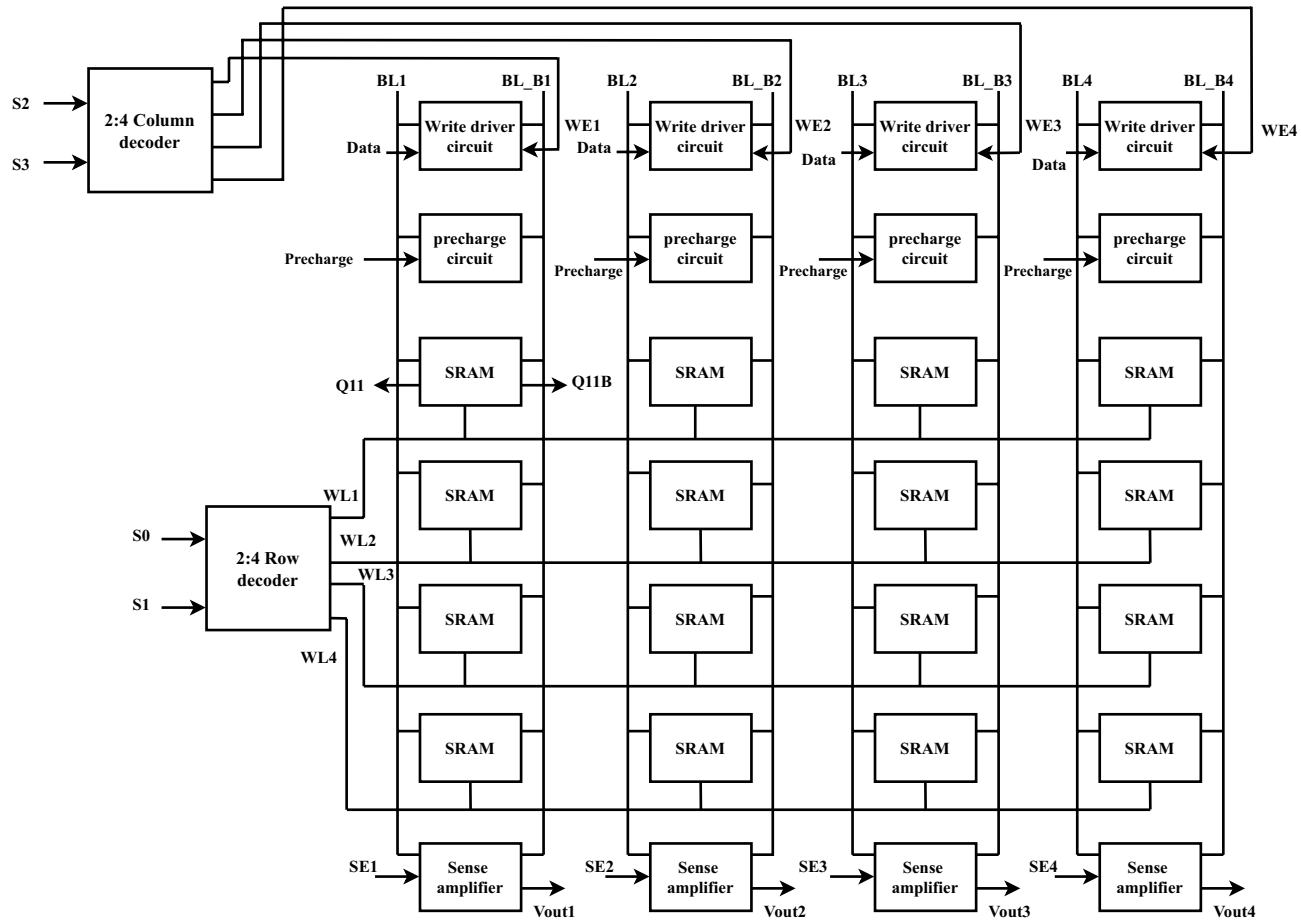

Fig. 2 Block diagram of normal 4 × 4 SRAM array

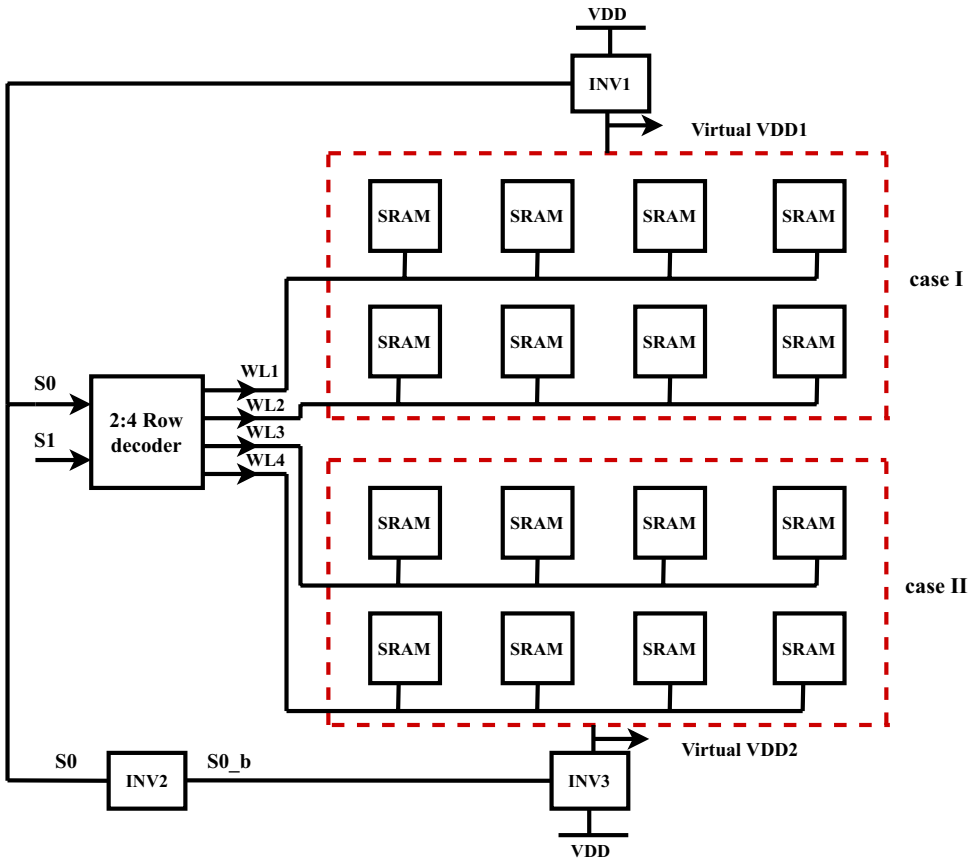

Fig. 3 Block diagram of proposed power gated design in the array of 4 × 4 SRAM cells

word lines for the array of 4 × 4 SRAM cells are the output of the 2:4 row decoder. So, the inputs of the row decoder, namely S0 and S1, decide which word line (WL) is to be asserted ON at a particular time. Table 2 shows the selection of word lines. From Table 2, it may be observed that if S0 becomes '0', then at that particular time, word lines WL3 and WL4 (case II) are OFF (Hold state). That means the associated eight SRAM cells are isolated from the bit lines. Similarly, if S0 becomes '1', then on that period, word line WL1, WL2 (case I) will be OFF. And the associated eight SRAM cells will be in the hold condition. In our proposed design, we have used three inverters to implement the power gating for the array of 4 × 4 SRAM cells. The operation of the proposed power gating design of SRAM is shown in Table 3.

Table 2 Selection of word line

S0	S1	Word line selection
0	0	WL1
0	1	WL2
1	0	WL3
1	1	WL4

The detailed functionality of our proposed SRAM design is described below.

4.1 Read and Write Operation

During the read and write operation, the word line is asserted high (WL= '1'), and the bit lines, i.e. BL, BL_B, are acting as output and input, respectively. Word line activates both of the access transistors that connect the cell to and from bit lines. When the input of the row decoder S0 is '0', then either word line WL1 or WL2 activates. In that condition output of INV1, virtual V_{DD1} becomes V_{DD}. And the associated SRAM cells can perform write and read operations. Similarly, when S0 is '1', then either WL3 or WL4 activates. Then, S0_b becomes '0', and the output of INV3, virtual V_{DD2} becomes V_{DD}. And the associate SRAM cells can execute write and read operations similar to the conventional SRAM.

4.2 Standby Mode or Hold Operation

The word line is asserted low (WL='0') during the hold operation, and the access transistors separate the cell from the bit lines. When the input of row decoder S0 is '0', then

Table 3 Proposed SRAM cell operation

Virtual V_{DD}	WL	BL	BL_B	Q	Q_B	operation
1 (VDD)	1	1	1	0/1	1/0	Read
1 (VDD)	1	1	0	1	0	Write '1'
1 (VDD)	1	0	1	0	1	Write '0'
0 (GND)	0	X	X	0	0	Hold

WL3 and WL4 are OFF. Therefore, the eight SRAM cells connected with the WL3, WL4 (case II) are in the hold condition. In our proposed design, when S0 becomes '0', then the output of the INV3, Virtual V_{DD2} becomes '0'. So, during this condition, the SRAM cells connected with word lines- WL3 and WL4 will be power gated. After that, when S0 becomes '1', then word lines- WL1 and WL2 (case I) will be OFF. In that condition, the output of INV1, virtual V_{DD1} becomes '0'. Therefore, the SRAM cells connected with word lines- WL1 and WL2 will be power gated for that particular time duration. Using our proposed design, at a time, eight SRAM cells are power gated. That means both PMOS transistors of the eight SRAM cells are in recovery condition during the hold period. So, these transistors get sufficient time to relax from the NBTI degradation, and the performance, SNM, and lifetime of SRAM improve significantly using our proposed design. Moreover, as SRAM cells are power gated during the hold operation, a significant amount of leakage power can be saved using our approach.

Figure 4 represents the block diagram of the $4 \times N$ SRAM cells based on the proposed power gating design. In our design, the 4×4 SRAM array is considered for simulation. Our proposed approach can be further extended to any higher array of SRAM cells if we consider a 4×N array structure, where N represents the number of the column. If we consider N=8, then at a time, 16 SRAM cells will be power gated using our approach. As a result, power reduction will keep increasing as we keep increasing the number of N. Moreover, using this approach, more transistors will

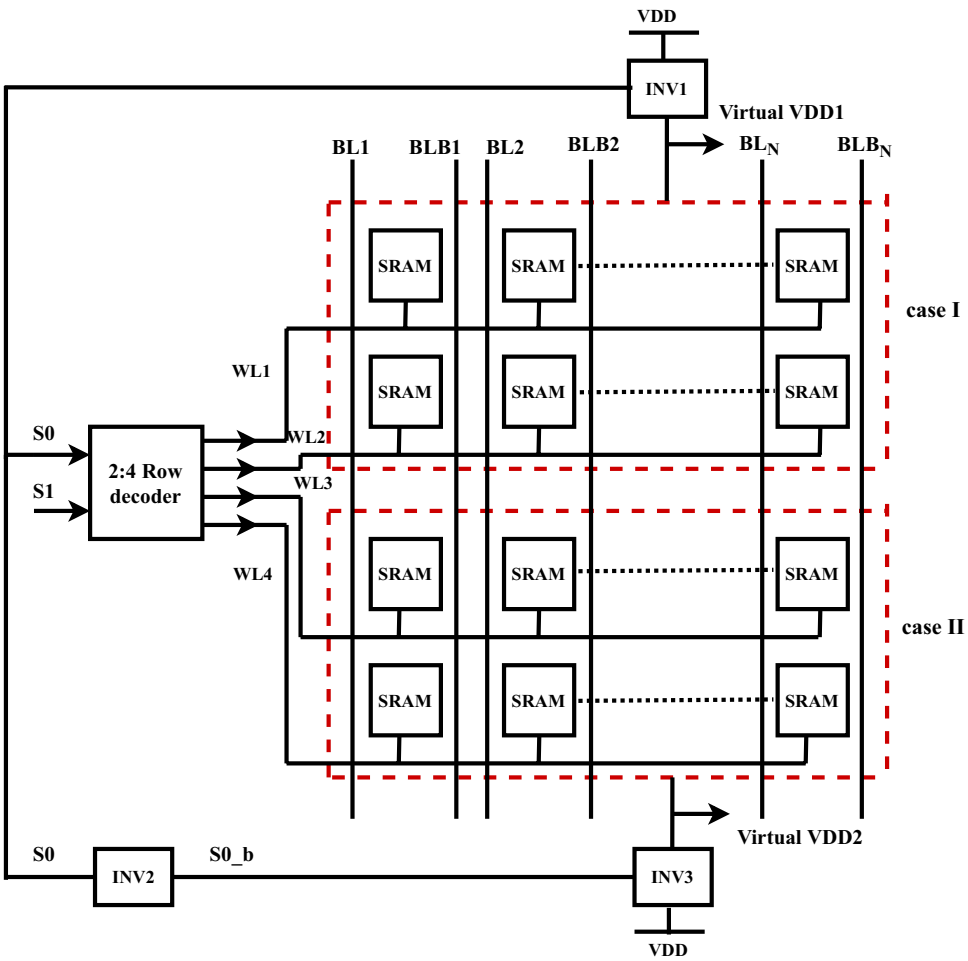

Fig. 4 Block diagram of the 4×N SRAM cells based on the proposed power gating design

be in the recovery state during the hold period. On the other hand, the access area required for implementing the logic remains the same even for the higher number of N, as the same word line will control any number of SRAM cells in a particular row. As a result, the area overhead will keep decreasing as we increase the number of N.

5 Simulation Result & Related Discussion

This section investigates the effectiveness of the proposed NBTI-aware low leakage power gating design for a 4×4 SRAM array. All the simulations are performed in Cadence Virtuoso using UMC 28nm CMOS technology. The transistors we have used from UMC 28nm library are 1.8V T-G (Thick gate) devices having a channel length of 150nm [31]. The simulation for NBTI degradation is performed using Cadence Relxpert at the worst-case temperature of 125^0C for 10 years of operation [16, 32]. We have used the supply voltage of 1.8V for the simulation. First of all, we have designed a 4×4 SRAM array which includes 6-T SRAM cells, write driver circuits, pre-charge circuits, sense amplifiers, row decoder (for word line), and column decoder (for write enable). We have calculated all the necessary parameters like leakage power, read access time, write access time, and NBTI-induced V_{th} degradation for a normal 4×4 SRAM cell array. After that, we have designed our proposed NBTI aware low leakage power gating design for a 4×4 SRAM array. From this also, we have calculated necessary information like leakage power, read access time, write access time, wake up time, SNM, and NBTI-induced degradations. Finally, we have compared the proposed design with the conventional SRAM design.

Figure 5 represents the transient response of the proposed power gated design of the 4×4 SRAM array. From Fig. 5, it may be seen that when S0 is '0', then virtual V_{DD1} becomes '1' and virtual V_{DD2} becomes '0'. During this time, WL1 is asserted high, and the values of Q and Q_B are '1' and '0', respectively. When S0 becomes '1', at that time, WL1 becomes '0', and virtual V_{DD1} also becomes '0'. At that moment, both Q and Q_B become '0', as both PMOS transistors of that SRAM cell are OFF. After some time, when S0 is again become '0', virtual V_{DD1} becomes '1', and the previous values of Q and Q_B are restored (Q=1 and Q_B=0). Here, when the power gating technique is applied, the stored values (Q, Q_B) become '0'. But, the value of Q_B will be in strong '0', whereas Q will be in weak '0'. This is because the stored charge of Q was not fully discharged. So, whenever power gating is removed, the bit having weak '0', i.e., Q becomes '1' instantly. So the logic and functionality will be unaffected. Similarly, the write '0'/ read '0' operation of the proposed design is also presented in Fig. 5. Here, we can see that the word line is asserted high during the write and read operation. After data changes from '1' to '0', and write enable (WE1) becomes high, Q becomes '0' and Q_B becomes '1'. After this, when sense enable (SE1) becomes high, the sense amplifier output (Vout1) becomes '0'. And logic '0' is written into and read from the SRAM memory. The same logic is applicable for the write '1' and read '1' operations.

5.1 Delay and Performance Analysis

Table 4 compares the performance and delay analysis of the proposed SRAM design with the conventional SRAM design. From Table 4, we can see the write access time for write '1' and write '0' operation of normal 4×4 SRAM design are 107 ps and 51 ps, respectively. Whereas in the case of our proposed design, the write access time for write '1' and write '0' operation are 114 ps and 54 ps, respectively. Although the power gating technique is used, we have

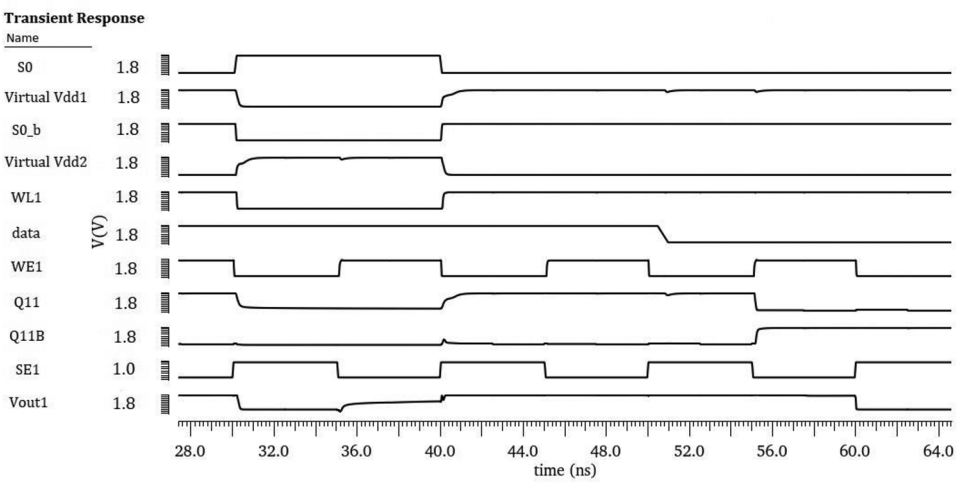

Fig. 5 Transient response of the proposed power gating design for 4×4 SRAM array

Table 4 Performance and delay analysis of the proposed design compared to the conventional design

Circuits	Write access time (ps)		Read access time (ps)		Static Noise Margin (mV)			Wakeup time (ps)
	Write '1'	Write '0'	Read '1'	Read '0'	Hold SNM	Read SNM	Write margin	
Normal 4×4 SRAM design	107	51	58.9	40.4	460	190	552	
Proposed SRAM design	114	54	48	29	432	185	520	117.5

a very negligible increase in delay for write access time in our proposed design. For the read delay analysis, the read access time for the read '1' and '0' operation of normal 4×4 SRAM design is 58.9 ps and 40.4 ps, respectively. Whereas using the proposed design, the read access times for the read '1' and '0' operations are 48 ps and 29 ps, respectively. Here for the read delay, the performance of the proposed design is better. In terms of the static noise margin (SNM), the hold SNM, read SNM and the write margin for normal SRAM are 460 mV, 190 mV, and 552 mV, respectively. And in the case of the proposed power gating SRAM design, the hold SNM, read SNM, write margin values are 432 mV, 185 mV, 520 mV, respectively. In the proposed design, the initial values of the SNM are degraded a little bit compared to the normal SRAM design. However, using the proposed design, the rate of degradation of read SNM improves considerably compared to the normal SRAM design, which has been discussed in the next subsection. The wakeup time for our proposed power gating design is 117.5 ps which means the proposed SRAM design can operate at an 8.51 GHz clock frequency. Figure 6 represents the hold SNM and read SNM of the proposed power gated design.

5.2 NBTI-Induced Degradation Analysis

Table 5 represents the NBTI-related V_{th} degradation of the proposed SRAM design compared to the normal SRAM design. For the normal ×4 SRAM design, the degradation

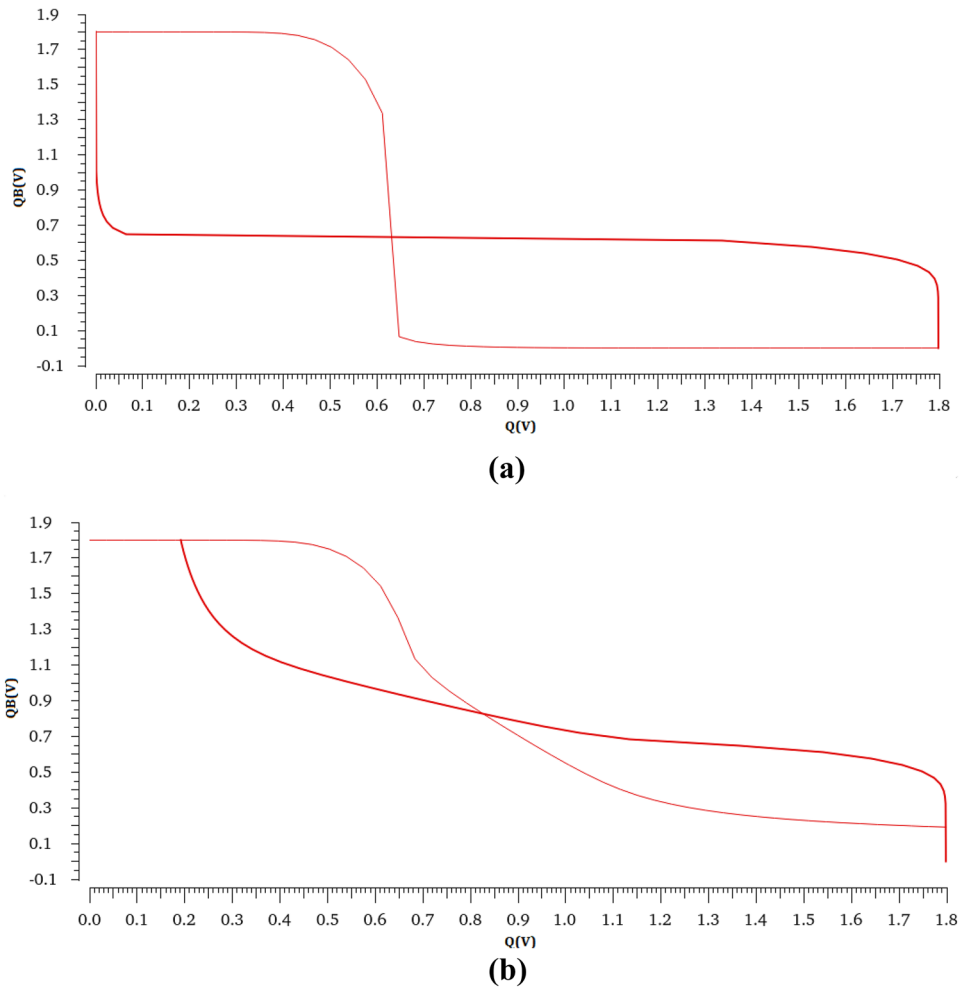

Fig. 6 Static Noise Margin of the proposed power gated SRAM design for (**a**) Hold SNM and (**b**) Read SNM

Table 5 Comparison of NBTI-induced V_{th} degradation in SRAM (T=125^{0}C)

Parameter	Normal 4×4 SRAM design	Proposed design considering all modes	Proposed design considering standby mode
Threshold voltage degradation (ΔV_{th})(mV)	33.80	23.52	1.27
% Improvement		30.41	96.24

of threshold voltage (V_{th}) is 33.80mV at 125^{0}C temperature and 10 years of aging. Whereas, using the proposed design, NBTI-induced V_{th} degradation is 23.52mV considering all the modes. So, using our proposed approach, overall 30.41% threshold voltage degradation can be reduced. However, as the proposed approach is based on power gating the supply voltage during the hold operation, considering only the standby mode NBTI-related V_{th} degradation is 1.27mV. So, considering only the standby mode 96.24% NBTI-related V_{th} degradation can be minimized.

Table 6 illustrates the comparison of the percentage saving of SNM degradation due to NBTI by our proposed approach over the normal SRAM design. In this paper, we are mainly focusing on reducing the rate of degradation due to the NBTI effect. Though in the proposed SRAM design, the initial value of the read SNM degrades compared to the normal SRAM design, the rate of degradation due to NBTI is reduced considerably in our proposed design. We have calculated the SNM degradation by Eq. (2) as a function of NBTI-induced threshold voltage change. Due to NBTI, the read SNM degrades from 190mV to 180.22mV in the normal SRAM design after 10 years of operation, which is near equal to 5.15% degradation. Whereas, in the proposed design, the read SNM degrades from 185mV to 178.19mV, which means 3.67% degradation after 10 years of stress time. Therefore, it may be considered that using the proposed approach, the rate of degradation of read SNM can be improved by 28.74% compared to the conventional SRAM design.

The degradations of read SNM for different stress times and temperatures of the normal SRAM design and the proposed design are illustrated in Fig. 7. Initially, the read SNM of the normal SRAM was 190mV. Due to the NBTI aging, after 10 years of stress, the read SNM has been degraded to 180.22mV (Fig. 7a). Similarly, the read SNM of the proposed design was 185mV initially, and after 10 years of NBTI stress, the read SNM becomes 178.18mV (Fig. 7b). Similarly, in Fig. 7c, the read SNM of the normal SRAM degrades from 187.67mV to 180.2mV from 27^{0}C temperature to 125^{0}C temperature. Whereas, in the case of the proposed design, read SNM degrades from 183.3mV to 178.19mV at 27^{0}C to 125^{0}C temperature. Using the proposed approach, a considerable percentage of the degradation rate of read SNM can be minimized.

Table 6 Comparison of the SNM degradation due to NBTI

Parameter	Normal SRAM design	Proposed SRAM design
Read SNM degradation (%)	5.15	3.67
% Saving		28.74

Figure 8 shows the comparison of percentage change of different parameters caused by NBTI for normal SRAM design and the proposed power gated design after 10 years of NBTI stress. The parameter degradations are calculated using Cadence RelXpert. For normal SRAM design, the trans-conductance (G_m) is degraded by 1.447%, where, for the proposed design, the degradation of trans-conductance is 1.009%. Similarly, in terms of the linear current degradation (I_{dlin}), the normal SRAM design is degraded by 2.716%, whereas, for the proposed design, the degradation is 1.89%. In the same way, for normal SRAM design, the degradations of saturation current (I_{dsat}) and drain-source conductance (G_{ds}) are 4.279% and 2.78%, respectively. Whereas, using the proposed design, the degradations of saturation current and drain-source conductance are 2.98% and 1.94%, respectively. Based on the above discussion, we can conclude that using the proposed power gating design NBTI-induced parameter degradations in SRAM cells can be reduced significantly.

Table 7 compares the change of threshold voltage of PMOS for the normal SRAM design and the proposed SRAM design under different stress times due to the NBTI effect. Here, the stress time is varied from 0 to 10 years. Initially, the threshold voltage of the SRAM is 390mV. Due to NBTI aging, the threshold voltage increases over time. For the normal SRAM design, due to NBTI stress after 10 years, threshold voltage increases to 423.8mV. Whereas, using our proposed approach, after 10 years of NBTI stress, threshold voltage increases to 413.54mV. This table shows that the threshold voltage degradation for different stress times can be reduced significantly using the proposed approach. The threshold voltage change with temperature, supply voltage, and stress time of normal SRAM design and the proposed SRAM design is plotted in Fig. 9. Though with the advancement of high-k metal gate technology, the PBTI effect also becomes prominent, the simulation result shows the impact of PBTI is not considerable compared to NBTI. That's why the PBTI results are not included in this analysis.

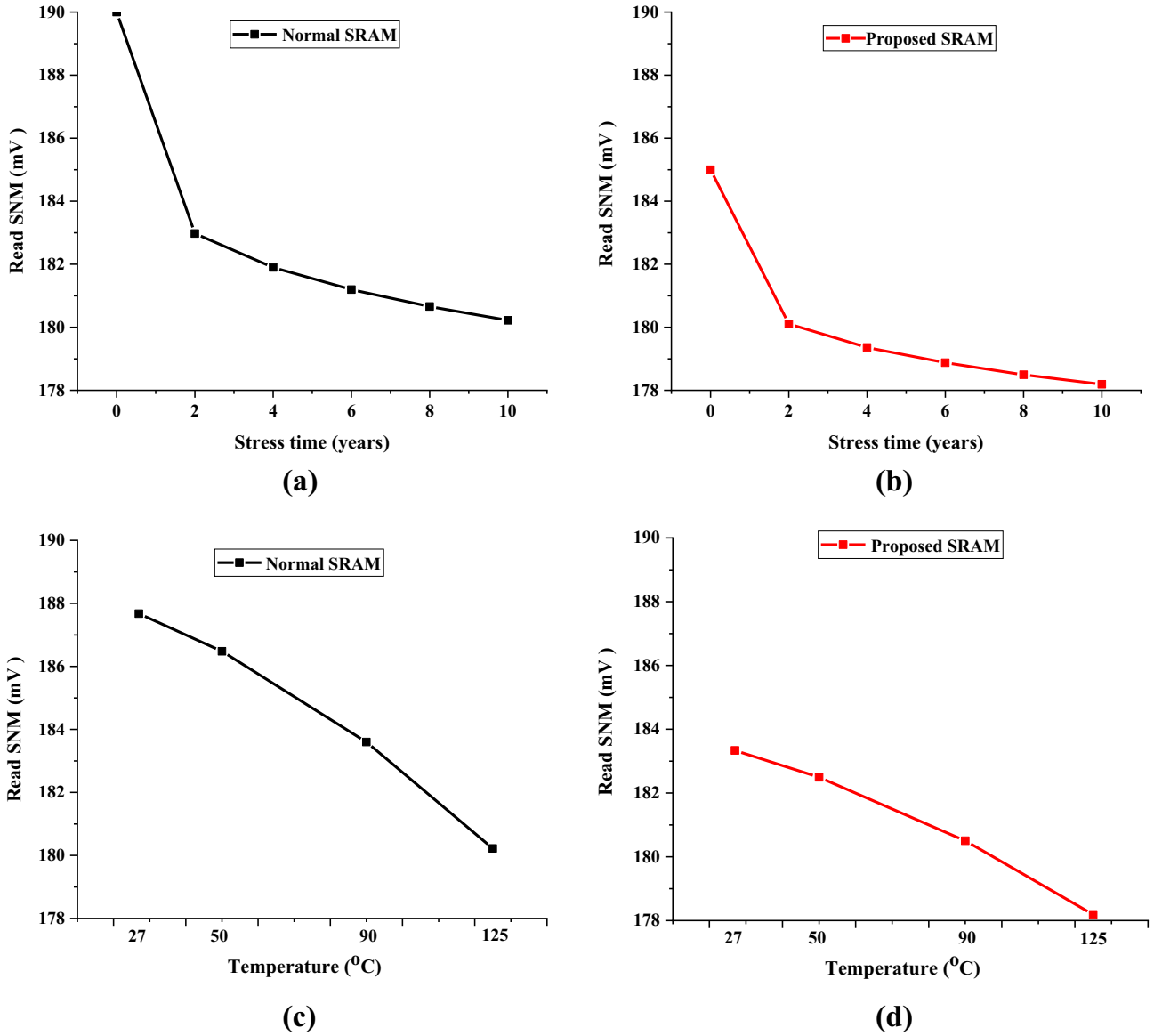

Fig. 7 Degradation of the read SNM under different stress time for (**a**) Normal SRAM and (**b**) proposed SRAM design and under different temperature for (**c**) normal SRAM and (**d**) proposed SRAM design

5.3 Power Analysis

Here, the power consumption report of the normal SRAM design and the proposed SRAM design are presented. With the advancement of the technology node, the leakage power contribution is almost comparable to dynamic power [11, 33]. And as our proposed design is based on a power gating strategy, which mainly focuses on reducing the leakage power consumption, hence we have focused mainly on the calculation of the leakage power and its reduction. Our analysis calculates leakage power when the word line (WL) is not activated ('0'). In our proposed design, eight SRAM cells can be power gated during the hold operation. So, the leakage power estimation is done on eight SRAM

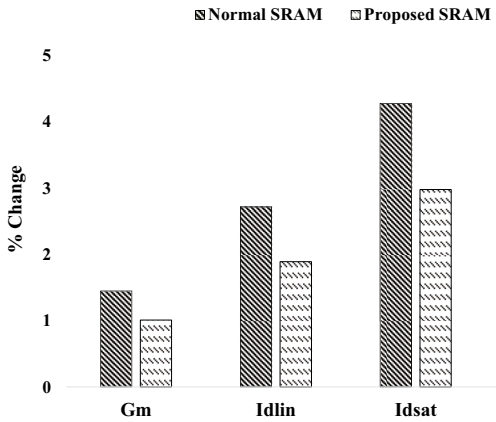

Fig. 8 Percentage change of different parameters of normal SRAM design and proposed power gating design after 10 years of NBTI stress

Table 7 Threshold voltage change of PMOS for normal SRAM and proposed power gated SRAM for different stress times

Stress time (years)	Threshold voltage(mV)	
	Normal SRAM design	Proposed SRAM design
0	390	390
2	414.29	406.9
4	418.01	409.5
6	420.44	411.17
8	422.29	412.49
10	423.8	413.54

cells (either case I or case II) when the word lines (WL1, WL2 for case I or WL3, WL4 for case II) for the respective SRAM cells are OFF. Table 8 compares the leakage power for the proposed power gating design compared to the conventional SRAM array. The leakage power for the conventional SRAM design is 9.226μW, whereas the leakage power for our proposed design is 1.928μW. So, using our proposed power gating approach, 79.10% leakage power can be saved. So, a significant amount of leakage power can be reduced using the proposed power gating approach. Figure 10 shows a bar diagram representing the comparison of power consumption of the normal SRAM design and the proposed design. However, the power reduction will increase if the proposed approach is applied to the 4×N SRAM array

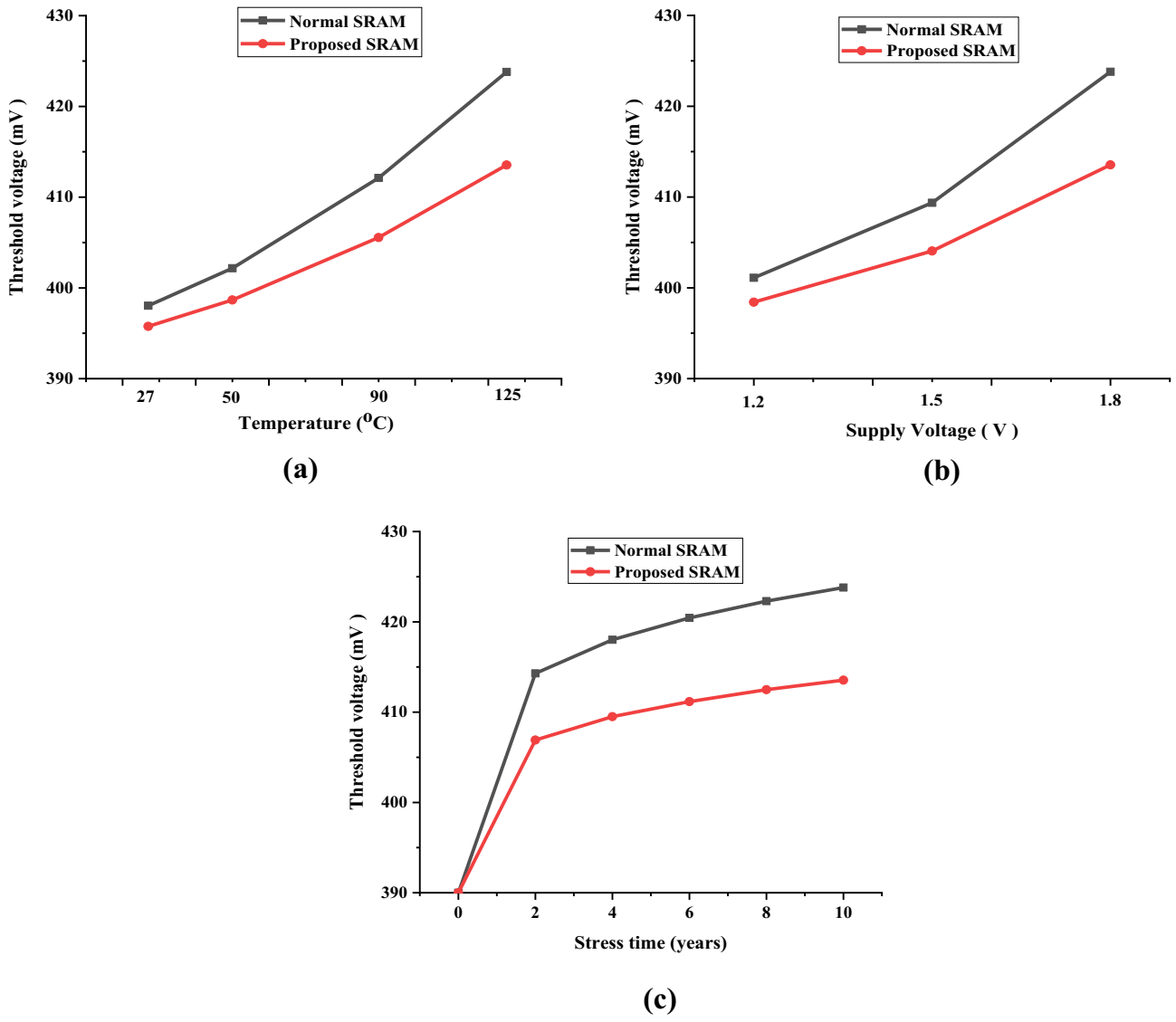

Fig. 9 Change of threshold voltage of PMOS for normal SRAM design and the proposed design for different (**a**) temperature (**b**) supply voltage (**c**) stress time

Table 8 Comparison of leakage power for the proposed design compared to conventional SRAM design

Parameter	Normal SRAM design	Proposed SRAM design
Leakage power (μW)	9.226	1.928
% Improvement of our approach over	79.10	

Table 9 Comparison of area overhead for the proposed design compared to conventional SRAM design

Parameter	Normal 4×4 SRAM	Proposed SRAM design
Total area (λ^2)	$676k$	$688k$
% increment of area overhead of our design over	1.78	

structure presented in Fig. 4. In our approach, we have only considered the 4×4 SRAM array for implementing the proposed approach. If we keep increasing the number of columns (N), more SRAM cells will be power gated at a time. As a result, power reduction will keep increasing with the increase of the number of columns.

5.4 Area Estimation

Table 9 shows the area estimation report of the normal SRAM design and the proposed power gated SRAM design. Here, the area report is estimated using the total width of the transistors in the design. Let's assume k is the width of the minimum width transistor, which is 1μm. So, the area of any transistor in the design which has a width of 3μm will be $3k$. The final area of the architecture is estimated by summation of the widths of the total number of transistors and multiplying it by k. The total area is expressed in terms of 'λ^2', where 'λ' denotes the feature size of a particular technology [34]. The area calculation presented in this paper is based on an estimation approach to compare the total area of the proposed design with respect to conventional SRAM design. Using this approach, the estimated area for normal SRAM design is $676k$, whereas, for the proposed SRAM design, the estimated area is $688k$. As a result, it is therefore observed that using the proposed approach, the total estimated area is increased by 1.78% compared to the normal SRAM design.

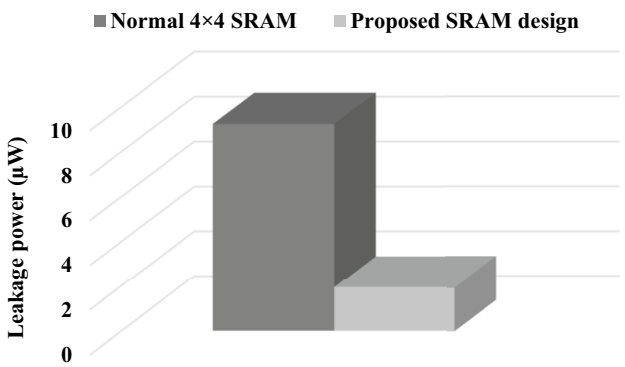

Fig. 10 Comparison of the power consumption of the normal SRAM design and the proposed design

Moreover, this approach can be further extended for the larger number of SRAM arrays. As discussed in Sect. 4, our proposed approach can be implemented on the 4×N array structure, where N represents the number of columns. So, the access area required for implementing the logic remains the same even for the higher number of N. Considering the number of columns (N) is 8, the proposed approach's area overhead will be 0.93%. Therefore, the area overhead will decrease with the increase in the number of columns.

Table 10 presents the comparison of the proposed approach with other related works. Here, the outcomes of the proposed approach are compared with Faraji et al. [11] and Kumar et al. [13]. In Faraji et al. [11], the adaptive body biasing technique (ABB) technique is used. Using their approach, the degradation of read SNM is improved by 21.49%. Also, using their approach, 27.13% leakage power can be saved, while their design requires 2.1% additional area. In Kumar et al. [13], data flipping is used and using their approach, 30% read SNM degradation is minimized. Whereas, in our approach, a power gating strategy is introduced to reduce the NBTI effect and leakage power dissipation by gating the supply voltage (V_{DD}) during the hold operation. Using our approach, overall 30.41% threshold voltage degradation can be minimized. Similarly, the rate of degradation of read SNM is improved by 28.74% using our approach. Moreover, using the proposed approach, 79.10% leakage power dissipation can be saved compared with the normal SRAM design. However, our approach has some extra 1.78% area overhead which is very minimal compared to the gains related. Furthermore, extending the proposed approach to the 4×N SRAM array will increase the leakage power reduction, and area overhead will decrease.

In the proposed power gating design, the initial value of the read SNM degrades a little bit compared to the normal SRAM design. Here, we are mainly focusing on reducing the rate of degradation of the read SNM due to NBTI. In the future, some new approaches can be implemented so that the initial value of the read SNM may not be degraded compared to the normal SRAM design. Moreover, in this paper, the proposed power gating approach is implemented on a 4×4 SRAM architecture. As discussed in Sect. 4, this approach can be further extended to the 4×N SRAM array structure. Also, in the future, a similar kind of power gating

Table 10 Comparison of the proposed approach with other related works

Reference	Technique used	Technology used	% Saving of ΔV_{th}	% Saving of read SNM	% Saving of power	%Area overhead
Faraji et al. [11]	ABB	PTM 32nm	-	21.49	27.13	2.1
Kumar et al. [13]	Data flipping	BPTM 70nm, 100nm	-	30	-	-
Proposed approach	Power gating	UMC 28nm	30.41	28.74	79.10	1.78

architecture might be presented to implement in a larger SRAM array, especially on a 16 × 16 SRAM array.

6 Conclusion

In this paper, a new 4 × 4 SRAM cell architecture is proposed to reduce the NBTI degradation and the standby leakage power. The proposed design is based on power gating the supply voltage of SRAM during the hold operation. As in hold operation, one of the two PMOS transistors of an SRAM cell is always under NBTI stress; using the proposed technique, both PMOS transistors will be in the OFF state and get sufficient time to relax from NBTI degradation. Moreover, using the proposed approach, a significant amount of standby leakage power also can be minimized. Simulation result shows, using the proposed technique, overall 30.41% NBTI related threshold voltage degradation can be saved. Moreover, using the proposed design, 79.10% leakage power can be reduced over the conventional SRAM design.

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Data Availability Data sharing not applicable to this article as no datasets were generated or analysed during the current study.

Declarations

Conflicts of Interest The authors declare that they have no conflict of interest.

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