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# Editorial

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We begin 2022 by welcoming two new editors to the Editorial Board of *JETTA*. Professor Jie Han is with the Department of Electrical and Computer Engineering at the University of Alberta in Canada. His areas of expertise include approximate computing, stochastic computing, brain-inspired learning systems and neural networks, reliability, fault tolerance, nanoelectronics, and novel computational models for nanoscale and biological applications. Dr. Albin Yan is with the School of Computer Science and Technology, Anhui University (AHU), China, where he is the Director of the AHU Institute of Chip Design and Test. His expertise also includes soft error mitigation techniques. The biographies of Professors Jie Han and Albin Yan appear in this issue following this editorial.

Leaving the Editorial Board at the end of 2021 is Professor R. D. (Shawn) Blanton. He has served on the Board since 2011 and decided to step down owing to the additional responsibilities he recently assumed at the Carnegie Mellon University. We have greatly benefited from his expertise and will miss him.

Peer reviewing is an essential part of *JETTA*'s paper selection process. We thank our reviewers of 2021, whose names appear in this issue, for their contribution to the journal and to the profession.

This issue contains seven articles covering the topics of hardware security, analog and radio frequency (RF) circuit testing, reversible circuits, radiation hardening and interference, aging and reliability, and built-in-self-test (BIST).

The first paper proposes high level transformations for hardware security of digital signal processing (DSP) circuits. Transformations are algorithmic and structural but leave the function invariant. The transformed circuit then becomes difficult to reverse engineer for an adversary. The authors are Naveenkumar, Sivamangai and Napolean from Karunya Institute of Technology and Sciences, Coimbatore, India, and Akashraj Nissi from Accenture, Chennai, India.

Next, is a paper on mixed-signal testing, the authors offer an improvement over the histogram method for linearity test of an analog-to-digital converter (ADC). Using especially generated two-tone sine-wave input, they manage to obtain high measurement accuracy at low cost. Contributors of this work are Zhao, Katoh, Kuwana, Katayama, Wei, Kobayashi, Nakatani and Hatayama from Gunma University, Gunma, Japan, and Sato, Ishida, Okamoto and Ichikawa from Rohm Co., Ltd., Yokohama, Japan.

The third paper describes methods for synthesis of reversible logic that would lead to fault-tolerant implementation of quantum computers. Authors are Bu, Yan and Yuan from Guangxi University of Science and Technology, Guangxi, China, and Tang from Jinggangshan University, Jiangxi, China.

Two papers, appearing at fourth and fifth spots, address electromagnetic interference and radiation hardening.

The fourth paper examines signal upsets caused by electromagnetic radiation. These prominently occur due to alpha particles at high altitude near ionosphere but are not completely absent at the ground level either. With continuously shrinking geometries on chips, what started out as single node upset, is now a multiple node situation. The paper gives a design for a latch that prevents triple node upsets. The authors are Lu, Hu, H. Wang, Yao, Liang, Yi and Huang from Hefei University of Technology, Hefei, China, and J. Wang from China Electronics Technology Group Corporation, Chongqing, China.

In the fifth paper, the authors pursue the problem of identifying the electromagnetic interference source (EMIS). Their machine intelligence approach uses convolutional neural network (CNN) with a noise reduction layer (NRL) for improved accuracy. The contributors are Xiao, Zhu, Zhuang and Yang from Southwest Jiaotong University, Chengdu, Sichuan, China.

The sixth paper is about age degradation of static random-access memory (SRAM). Power gating of memory cells reduces the negative bias temperature instability (NBTI)

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effect as well as the static power. The power gating is only applied during the hold state of the memory cell after which the previously written data is restored. Simulated performance shows 30% lower age-related rise in the threshold voltages due to NBTI and 79% leakage power saving. Contributors of this work are Bhattacharjee, Nag, Das and Pradhan from National Institute of Technology, Agartala, Tripura, India.

In the seventh paper, Menbari and Jahanirad from University of Kurdistan, Sanandaj, Iran, provide an ingenious strategy for built-in self-test (BIST). Their test circuitry can be run either in a concurrent mode in parallel with the normal operation, or in an offline test mode.

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**Editor-in-Chief**

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