

Impact of Pass-Transistor Logic (PTL) on Power, Delay and Area

**Kalyana R Kantipudi
ECE Department
Auburn University**

**Low Power VLSI Design
Fall '05**

Abstract:

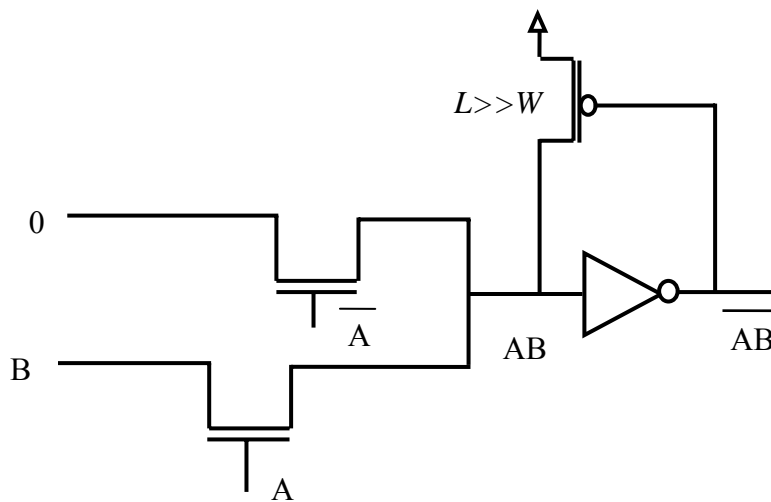
Power reduction is a serious concern now days. As the MOS devices are wide spread, there is high need for circuits which consume less power, mainly for portable devices which run on batteries, like Laptops and hand-held computers. The Pass-Transistor Logic (PTL) is a better way to implement circuits designed for low power applications.

Introduction:

The power consumption in a circuit can be decreased by reducing:

- Switching activity in the circuit
- Switching capacitance of each node
- Supply voltage
- Short-Circuit Current

Let's look at a PTL design:



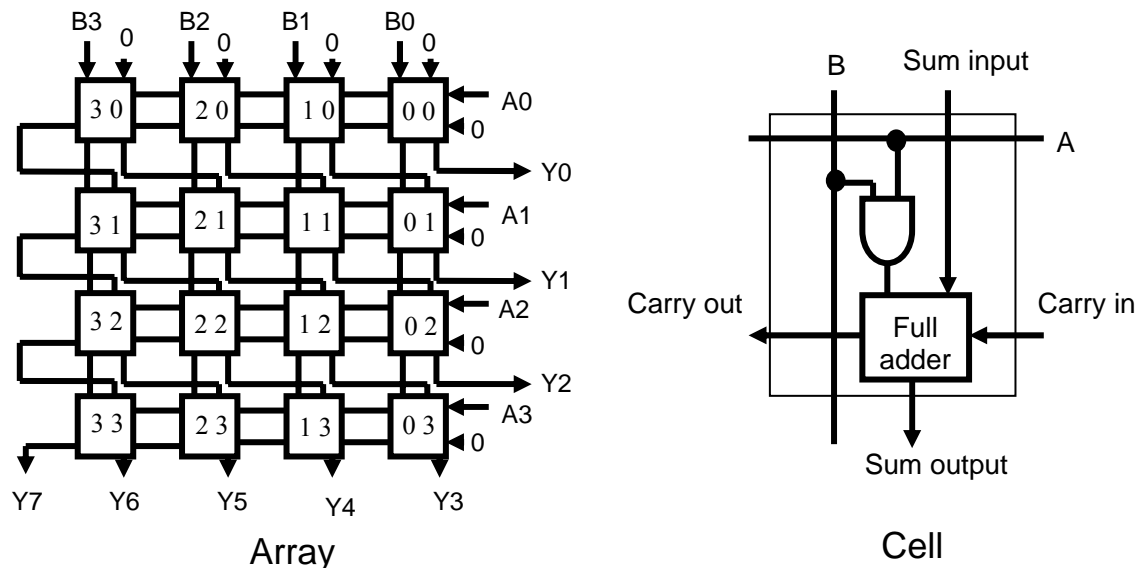
This kind of PTL design is called the Single-Rail Pass-Transistor Logic (also called LEAP). Here, a basic AND/NAND function is implemented. The PMOS transistor which is connected opposite to the output inverter is called a bleeder transistor, which is used to pull the weak '1' arriving at the input of the inverter.

Now, the advantage of PTL comes from the fact that it is best suitable to implement all the above power reduction techniques:

1. Switching activity in the circuit can be reduced by eliminating the glitches. This can be done by controlling the delays of each pass transistor (controlling the widths and lengths).

2. Switching capacitance of a node in the PTL will be less when compared to a node in the CMOS design. Due to the smaller size of the transistors in PTL implementation.
 - The lengths of the transistors should be as small as possible, because increased lengths result in more IR_{drop} across the transistor.
 - The widths of transistors also should be small. It's because the improvement seen in the switching of that transistor will be subdued by the delay caused in the input, which is driving that wider gate. This phenomenon can be observed in the presentation slides.
3. Like the CMOS technologies, the supply voltage can be reduced at the cost of some increase in delay of the circuit.
4. There are fewer ground connections (only at the inverters) means fewer V_{DD} to GND connections during switching. So theoretically PTL implementation should draw least amount of short circuit power.

The Present Project:^[1]



Steps followed to create the final 32x32 bit CMOS design:

1. A full adder is designed at the behavioral level in VHDL.
2. A multi_cell is implemented using the full adder and "and" gate.
3. The 32x32 bit multiplier is designed at the structural level using the 'multi_cell' in VHDL.
4. The generated 32x32 bit multiplier code is simulated in ModelSim to verify its functionality.

5. Then the 32x32 bit multiplier is synthesized using Leonardo for TSMC025 technology.
6. The synthesized model is imported into Design Architect.

The critical path given by Leonardo for my design is:

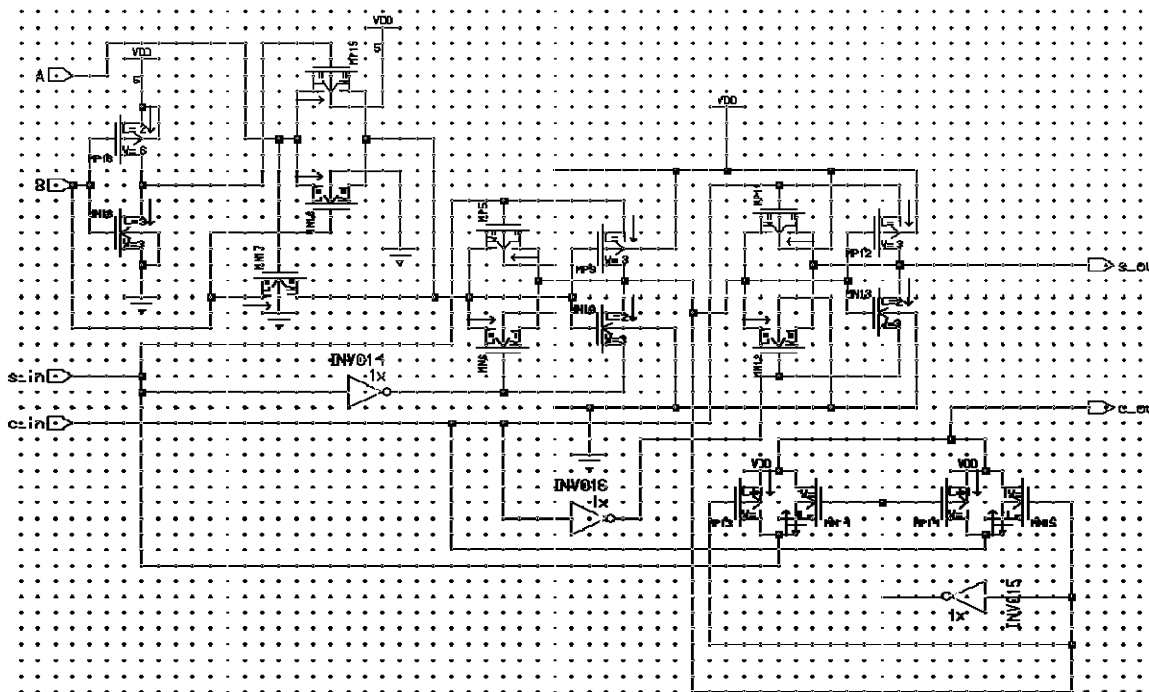
A0 or B0 → [0 0] → [1 0] → [2 0] → [3 0] → [2 1] → [1 2] → [0 3] → [1 3] → [2 3] → [3 3] → Y7

“Eldo” simulator which is a part of the Anacad&Mentor package is used for simulations at the transistor level.

Implementations:

There are basically 3 implementations I have manually designed transistor by transistor:

1. Normal PTL single rail design (--explained in the slides)
2. Transmission gate based design (see fig. below)
3. A new PTL design based on special XOR/XNOR gates (--explained in the slides)



All the implementations are working properly. Actually, I have implemented and simulated a full 4x4 multiplier using the above transmission gate based design. The above design is robust w.r.t loads (has good Delay Vs Load characteristics). The waveforms are looking robust like the CMOS based design with reasonable delays. But, the Eldo is having problems with this implementation (not reporting the static power correctly).

Power Consumption and Delay:

--Explained in slides.

Circuit Type	Static Power	Dynamic Power	Delay
CMOS	356.56pW	12.49μW	551ps
PTL	353.36pW	79.24μW	8.45ns
T _x gate	-	9.4μW	1.39ns
New PTL*	105.15pW	16.63μW	662ps

* Only 15 transistors are needed. The XOR design implemented in here will not produce a complete transition for 0, 0 inputs. It is considered that having smaller voltage swing will save dynamic power. (-- reference in slides)

Given below are the previously obtained results for a 0.35μm 4x4 multiplier based on the new PTL cell operating at 3.3V and 500 MHz. ^[2] (compared with other designs)

	Proposed	16-trans	Trans. Gate
Avg. Pwr. *10 ⁻³ W	0.851	1.798	2.746

Table 3. Simulation results for 4-bit multiplier using the 2 adder cells.

Area overhead:

--Explained in slides.

Considering for each cell, the area consumed by CMOS is at least 4 times the area consumed by the PTL design. So if we consider a 32x32 bit multiplier a much higher saving in area can be expected from the PTL design.

Lessons learnt:

As there are no particular cell libraries for PTL designs. I had to manually create my own designs. The mistake I have done is instead of creating a single logic gate and fully optimizing it; I aggressively designed the entire multi_cell and tried to optimize the widths and lengths of that complex cell.

So when ever we want to create a complex cell, first we should start with a basic gate, try to get the best optimized design and then go for the bigger one.

Reference:

[1] Dr. V D Agrawal's Project assignment.

[2] Fayed, A.A and Bayoumi, M.A., "A Low Power 10 Transistor Full Adder Cell for Embedded Architectures," in *Proc. IEEE Int/. Symp. Circuits and Systems*, vol. 4, pp. 226-229, Sydney, Australia, May 2001.

--Other references in my presentation slides